

VFAT2 : A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.

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Abstract

The architecture, key design parameters and results for a highly integrated front-end readout system fabricated as a single ASIC are presented. The chip (VFAT2) comprises complex analog and digital functions traditionally designed as separate components. VFAT2 contains very low noise 128 channel front-end amplification with programmable internal calibration, intelligent “fast OR” trigger building outputs, digital data tagging and storage, data formatting and data packet transmission with error protection. VFAT2 is designed to work in the demanding radiation environments posed by modern H.E.P. experiments and in particular the TOTEM experiment of the LHC.

Measured results are presented demonstrating full functionality and excellent analog performance despite intensive digital activity on the same piece of silicon.

I. INTRODUCTION

VFAT2 is a “trigger and tracking” front-end ASIC, designed primarily for the readout of sensors in the TOTEM [1] experiment of the LHC.

The VFAT2 chip (shown in Figure 1) has been designed in quarter micron CMOS technology and measures 9.43mm by 7.58mm. It has two main functions; the first (Trigger) is to provide programmable “fast OR” information based on the region of the sensor hit. This can be used for the creation of a trigger and in CMS it provides input to the first level trigger (LV1A). The second function (Tracking) is for providing precise spatial hit information for a given triggered event.

TOTEM itself comprises three operating regions each employing a different sensor technology to detect charge from traversing minimum ionising particles (MIPs). Silicon strips, Gas Electron Multipliers (GEM) and Cathode Strip Chambers (CSC) are the technologies used each having different electrical characteristics. VFAT2 will be used for low noise MIP discrimination for all 3 sensor technologies.

II. GENERAL ARCHITECTURE

Figure 2 shows the block diagram for VFAT2. It has 128 analog input channels each of which are equipped with a very low noise pre-amplifier and shaping stage plus comparator. A calibration unit allows delivery of controlled test pulses to any channel for calibration purposes. Signal discrimination on a programmable threshold provides binary “hit” information which passes through a synchronisation unit and then stored

within SRAMs until a trigger is received. The storage capacity enables trigger latencies of up to 6.4 μ s and the simultaneous storage of data for up to 128 triggered events. Dead time free operation with up to 100kHz Poisson distributed trigger rates is ensured. Time and event tags are added to the triggered data which are then formatted and read from the chip in the form of digitized data packets at 40 Mbps.

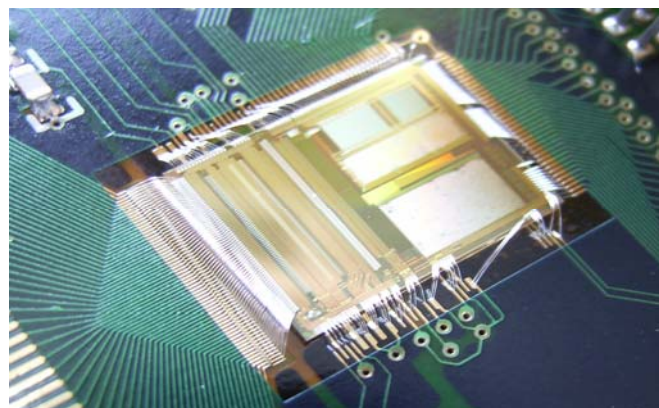


Figure 1 Photograph of VFAT2

VFAT2 has many programmable features which are controlled through an I²C slow control interface. Fast synchronous commands are applied via an encoded LVDS signal (T1) which is then decoded to 4 synchronous commands via an internal command decoder.

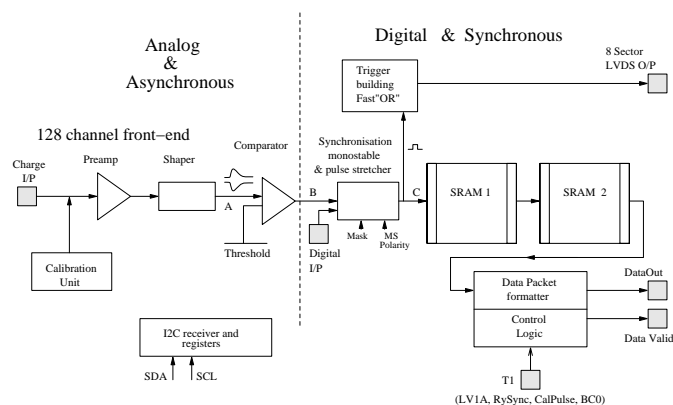


Figure 2 Block diagram of the VFAT2 signal flow.

III. ANALOG FRONT-END

A. Preamplifier, shaper and comparator

The front-end consists of a transimpedance preamplifier followed by a shaper with two stages of amplifier-integrator circuits and then a comparator. The schematic diagram for the front-end is shown in Figure 3.

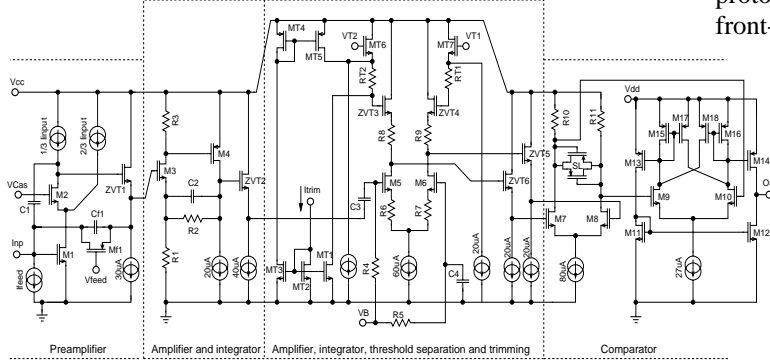


Figure 3 The VFAT2 front-end [2].

The pre-amp is a cascode configuration with an NMOS input transistor operating close to weak inversion. The gate capacitance of the input transistor is approximately 4pF. An active feedback loop provides signal discharge with a 13ns time constant for 0.8μA feedback current.

The shaping stage is composed of two amplifier and integrator stages. The shaper is tuned to give an overall 22ns peaking time. The second amplifier/integrator stage has a programmable dc level which acts as a threshold control for the comparator that follows. The threshold is controlled by two programmable voltages (VT1 & VT2) which provide a coarse threshold adjust to all channels. In addition there is a 5 bit Trim DAC for each channel. The Trim DAC can be used to finely adjust the threshold applied to each channel to remove any slight differences between channels due to fabrication statistical fluctuations. The TrimDACs can be used to apply a “constant threshold” in fC to all channels or to apply “constant signal clarity” i.e. a threshold adjusted to a constant separation of threshold to the noise floor.

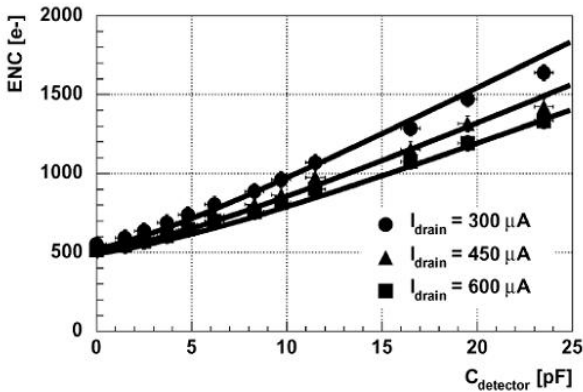


Figure 4 The ENC of the VFAT2 front-end [2].

The front-end dc bias can be adjusted to optimise the signal response for positive or negative input signals.

The variation of ENC with respect to capacitance of the front-end is shown in Figure 4. Series noise contributes around 50 e/pF ($M1_{id} = 450\mu A$) and 60 e/pF ($M1_{id} = 300\mu A$). For highly capacitive detectors a higher input device current ($M1_{id} = 600\mu A$) can reduce the noise slope to ~40 e/PF.

Full details of the front-end design and results of an initial prototype are given in [2]. The main characteristics of the front-end are summarized in Table 1 [2].

Shaper order	CR-(RC) ³
Gain	60 mV/fC
Peaking Time	22ns
Linearity	± 12 fC
Input Impedance	120 to 200 ohm (at the central frequency)
GBW	600 MHz
Parallel Noise	400 e rms
Noise Slope	40 - 60 e/pF
ENC	1500 e (for an input cap. Of 20pF)
Time Walk	12ns (for signal 1.2fC to 10fC with a 1fC threshold)
Power consumption	1.5mW
Ionising radiation tolerance	Measured to 10 Mrad of Xrays with no observable effects.

Table 1 Front-end characteristics

B. Calibration Unit

For calibration purposes VFAT2 contains an internal test pulse generator within the calibration unit shown in Figure 5. A controlled voltage step is generated and applied to a capacitor (C_{inj}). This, in turn applies a charge pulse to the input of a preamplifier. Each channel is equipped with a C_{inj} capacitor which when not in use is connected to ground. Connecting C_{inj} to the output node of the calibration unit (CalOut) selects that particular channel for calibration. All channels can be individually selected as can any number of channels simultaneously in any combination.

The amplitude of the voltage step applied is controlled by an 8 bit DAC (VCal). The step is generated by pre-charging two highly capacitive nodes within the calibration unit. One is charged with the value controlled by VCal and the other charged to a constant reference value. These nodes are known as V_{low} and V_{hi} respectively. The polarity of the step can also be selected and hence pre-charges CalOut to either V_{hi} (for a negative step) or V_{low} (for a positive step) as required. The step is generated by switching CalOut to the other pre-charged capacitive node inside the calibration circuit. The mechanism is that of charge transfer between two pre-charged nodes. Great care has been taken to optimise the transistors W/L used in complementary switches to transfer the charge in order to obtain low “on resistance” whilst maintaining low “charge injection” from the gate to the drain.

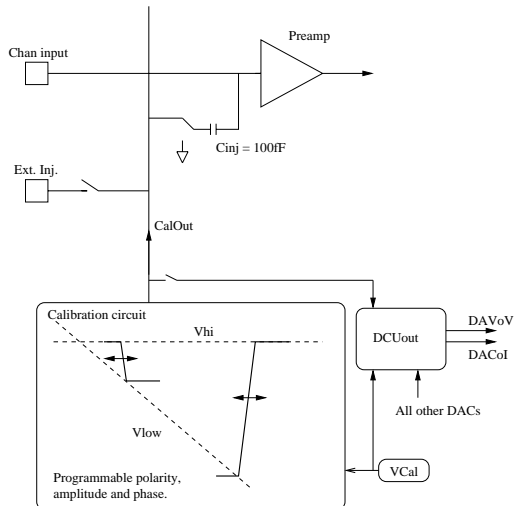


Figure 5 Internal test pulse generator for calibration.

The timing of the voltage step is controlled by the CalPulse signature on the T1 signal which is synchronous to the 40MHz master clock (MCLK). The phase is also possible to vary in steps of 45 degrees.

C. Biasing

The biasing of the analog part and control of VCal and thresholds is taken care of by 9 internal 8 bit current DACs of the form shown in Figure 6. The DAC design uses binary weighted current sources. All the DACs are themselves biased from a single bandgap reference which provides temperature stable operation.

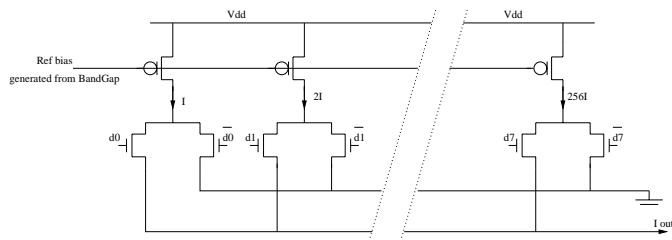


Figure 6 DAC design

The DACs can themselves be characterised and monitored by routing their individual current or voltage outputs to the outside world. This is particularly important for knowledge of the calibration pulse amplitude. One routes in turn the pre-charged values of Vhi and Vlow to the DACoV output. The amplitude delivered to the node CalOut is then the difference between the two values.

IV. DIGITAL SECTION

A. Synchronisation and monostable stage

Data leaving the comparator is asynchronous and has a pulse width proportional to the time over threshold. A clocked monostable has been designed to synchronise the digital signal and produce a controlled quantised signal length regardless of the time spent over threshold, shown in Figure 7.

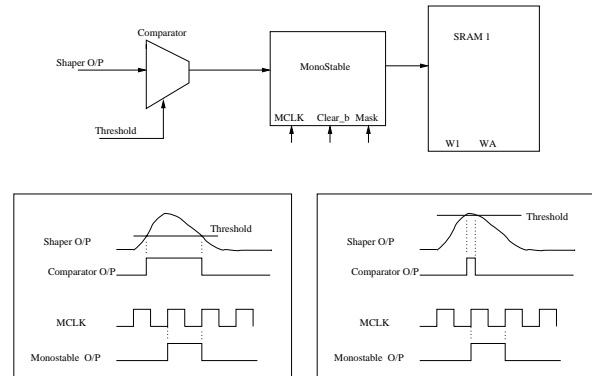


Figure 7 Clocked monostable

The monostable will produce a single synchronised pulse every time the comparator has signal over threshold. Since the front-end can support both negative and positive input signals, the polarity for the monostable is programmable. A positive pulse at its output represents a “hit” in either polarity.

The duration of the pulse at the output of the monostable is programmable from 1 to 8 clock periods.

It is at this stage that a “Mask” facility is introduced. All channels have the possibility of being masked individually which means that excessively noisy channels can be switched off.

VFAT2 also has the possibility to receive digital signal inputs and ignore the analog front-end. If this mode is used then digital inputs are bonded to pads located just before the clocked monostable.

B. Trigger building

VFAT2 has the possibility to provide “fast OR” signals that represent “hits” in the detector and hence can be used for trigger building. A “1” at the output of the monostable represents a “hit” in that detector channel. The 128 channels are then grouped in sectors and assigned to 8 LVDS outputs labelled S1 to S8. The assignment of sectors is programmable and explained in [3].

In addition a “hit” counter can be used for monitoring occupancy in the whole chip or for a selected sector.

C. Data storage and data formatting

Storage of data is done using two SRAM blocks (Figure 8). SRAM1 is filled with 128 channels of data at each clock cycle. The length of SRAM1 is 256 storage elements allowing 6.4μs of a 100% historical record. A trigger (LV1A) signal is received through the T1 line and decoded by the command decoder. Trigger latencies are permitted from 1 to 256 clock periods. On receiving a LV1A signal the data column corresponding to the trigger is transferred to SRAM2. At the same moment the values of counters “BCN” (12 bit Bunch crossing number) and “EN” (8 bit Event Number) are also transferred. SRAM2 hence is 20 bits wider than SRAM1 and has a length of 128 bits allowing simultaneous storage of 128 triggered events.

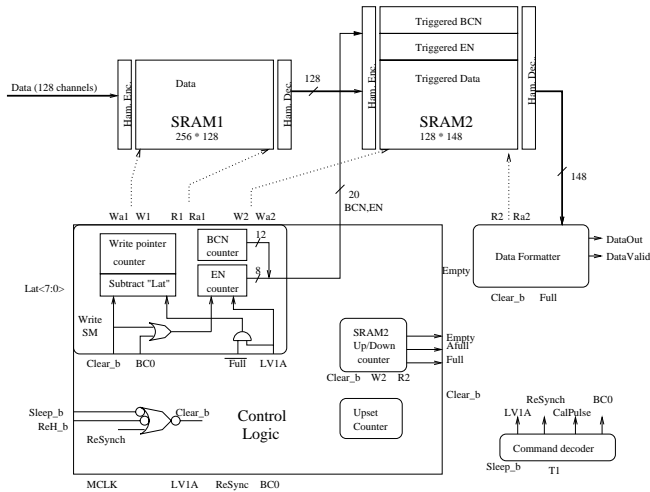


Figure 8 SRAMs, Control Logic and Data Formatter

The Control logic controls the write/read pointers for the memories. SRAM1 is written to in a continuous circular fashion overwriting previously written data. SRAM2 is controlled so that it behaves as a FIFO. Data for each LV1A is popped out of SRAM2 and formatted into data packets. The packet is then streamed out of VFAT2 at 40 Mbps. Figure 9 shows the data packet structure. Headers are included and also status flags. The packet finishes with a Cyclic Redundancy Check (CRC) to verify transmission integrity. An idle space of 2 clock periods separates successive data packets.

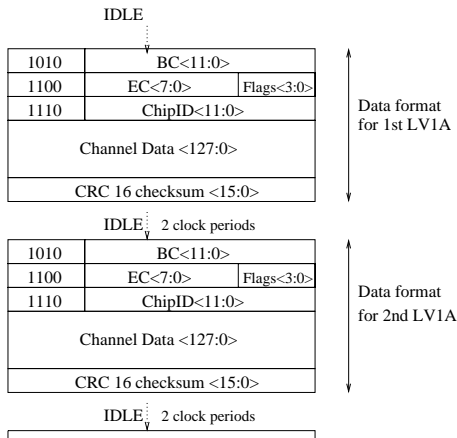


Figure 9 The data packet format

D. The I²C interface

VFAT2 has many programmable functions controlled through an I²C interface. These include: biasing of analog blocks, calibration unit control, front-end response polarity, channel masking, latency control, sector definitions, test mode settings including automatic self test of the digital memories. Chip status information including occupancy and SEU rates can be read via I²C. Reference [3] contains a complete guide to all the programmable functions and I²C register addresses.

In total, there are 152 internal programmable 8 bit registers. The I²C receiver design is asynchronous to avoid using a 40MHz sampling clock. Since the I²C is not active while taking data it is supplied from the analog power supply. Care has been taken to add low pass filters and glitch protection to the inputs of the I²C therefore reducing sensitivity to noise on the I²C bus.

The I²C uses standard 7-bit addressing where 3 bits are used for the chip address and 4 bits used for 16 principal register addresses. A further bank of 136 internal extended registers is made available by using principal registers 14 and 15 to point to the extended register addresses.

V. GENERAL DESIGN TECHNIQUES

VFAT2 combines low noise amplification and complex digital circuitry on the same piece of silicon. Various techniques have been employed to limit the distortion of the analog signal from charge transfer through the silicon substrate from the digital parts to the analog parts.

The chip is designed in a modular fashion. The different modules are Front-End, Monostable, Sector Logic, SRAMs plus Control Logic and I²C. Each module has its own power supply using as many power pads as possible. Also each module is surrounded by a guard ring full of substrate contacts. In the Monostable, Sector Logic and SRAM plus Control Logic modules, automatic place and route layout techniques have been employed. The library used for this has been specifically developed for resistance to radiation and to reduce injection of noise into the substrate. The later has been achieved by providing a separate return path for the switching current from the ground connection to the substrate.

Edgeless transistor structures have been extensively used throughout both for the full custom and semi custom parts of the design to reduce leakage effects due to ionising radiation.

Robustness to single event effects (SEE) has been built into the design too. Triplication and majority voting have been employed in the Sector Logic, Control Logic and I²C logic. The SRAMs have not been triplicated due to space restrictions however Hamming encoding has been employed to correct for single event upset errors.

VI. VFAT2 OPERATION

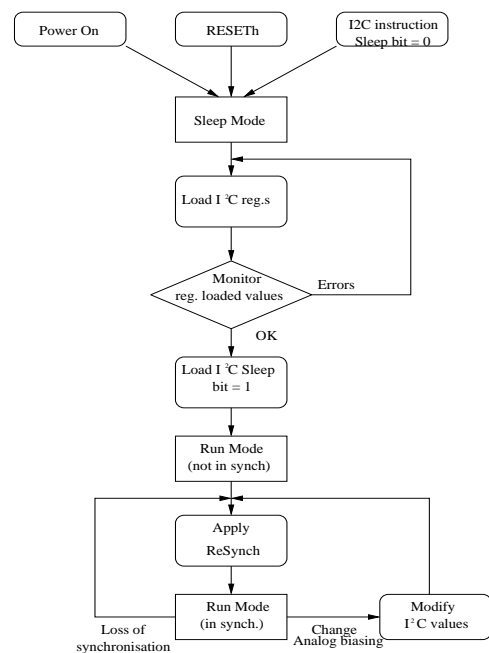


Figure 10 Operational flow chart

The operation flow is shown in Figure 10. On applying power to the chip VFAT2 performs an automatic power-on reset and goes directly into “Sleep mode”. Sleep Mode sets all DACs to default values providing stable but minimum power consuming conditions to the entire chip. In Sleep Mode only the I²C is active and can respond to commands. The internal registers can then be loaded with data. This data can be read back to check if loading was successful. The values loaded are not applied to the active circuits until VFAT2 is put into “Run Mode”. When VFAT2 is put into Run Mode, biases are applied to the analog circuits and digital circuits come out of a reset condition bringing the power consumption up to the normal level. Since the I²C is a non synchronous “slow” command VFAT2 still requires a synchronising signal. This is applied via a ReSync signal encoded within the T1 signal. VFAT2 is now in a synchronous Run mode and ready for taking data. Initial functional measurements showed all functions of VFAT2 to be fully operational.

VII. MEASURED RESULTS

Measurement of the calibration units test pulse generator reveal a charge delivery range of -2 fC to 18.5 fC with LSB = 0.08 fC and $\sigma(\text{LSB})$ from the straight line fit = 0.3fC.

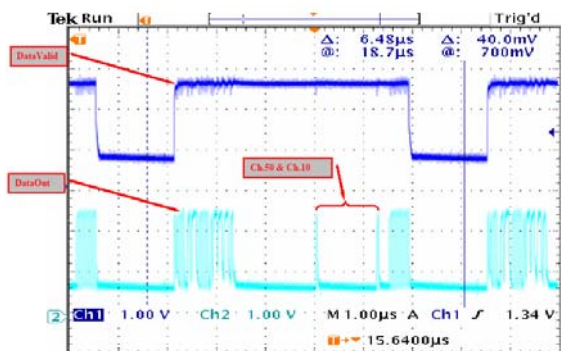


Figure 11 Oscilloscope view of a data packet output stream and the corresponding DataValid signal.

When triggered, Data packets appear on the DataOut output as shown in Figure 11 together with a DataValid signal which goes high for the duration of a Data Packet. The figure shows two “hit” channels, these channels received a charge pulse from the calibration unit.

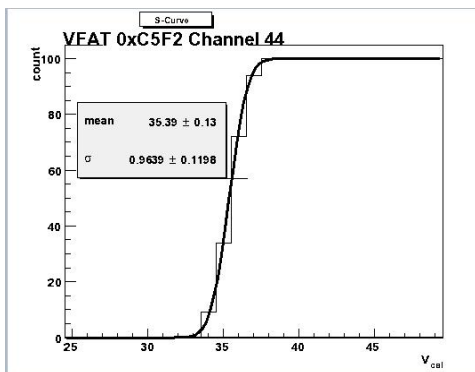


Figure 12 S-curve measurement. Number of “hits” against input signal amplitude (Vcal) on a single channel for a constant threshold.

Noise measurements have been made both with and without detector. Results from the analysis of S-curve measurements of the form shown in Figure 12 for the chip without a detector give the mean ENC = 589 e with $\sigma = 84$ e (for 128 channels). This was measured at a random threshold of 0.945 fC. The minimum threshold is 0.7 fC and maximum threshold 18.7 fC. The threshold spread across channels has been measured at 1.8% without trimming of DACs. The total power consumption is given in Table 2.

Power Consumption	Sleep Mode	Run mode (Nominal)	Run Mode (max. activity)
Analog	33 mW	378 mW	378 mW
Digital	135 mW	194 mW	237 mW
Total	168 mW	572 mW	615 mW

Table 2 Power consumption

VIII. SUMMARY

VFAT2 is a “trigger and tracking” front-end ASIC. It has 128 low noise input channels which after discrimination provide binary “hit” information for triggered events. The storage capacity enables trigger latencies of up to 6.4µs, simultaneous storage of data for <128 triggered events and enables continuous dead time free operation with up to 100kHz Poisson distributed trigger rates. Time and event tags are added to the triggered data which are then read from the chip in the form of digitized data packets at 40 Mbps.

A major design challenge was to integrate the multitude of digital functions without having a significant impact on the analog performance. Stringent design techniques to “deafen the listener” and “silence the talker” have been employed to all analog and digital modules.

Measurements from the chip show all modules to be 100% functionally correct. The shaper has a peaking time of 22ns. The expected front-end noise performance of approximately 400e + 50e/pF is maintained. The total power consumption is 572mW under normal operating conditions.

VFAT2 has successfully integrated complex analog and digital functions into a single ASIC without compromising noise performance.

IX. ACKNOWLEDGEMENTS

We would like to acknowledge the TOTEM collaboration and in particular the work of G. Antchev, J.Petaejaervi, V.Avati and E. Radicioni in helping obtain these results.

X. REFERENCES

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