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VFAT2 : A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.

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The architecture, key design parameters and results for a highly integrated front-end readout system fabricated as a single ASIC is presented. The chip (VFAT2) comprises complex analog and digital functions traditionally designed as separate components. VFAT2 contains very low noise 128 channel front-end amplification with programmable internal calibration, intelligent "fast OR"trigger building outputs, digital data tagging and storage, data formatting and data packet transmission with error protection. VFAT2 is designed to work in the demanding radiation environments posed by modern H.E.P. experiments and in particular the TOTEM experiment of the LHC.

Measured results are presented demonstrating full functionality and excellent analog performance despite intensive digital activity on the same piece of silicon.

Summary

VFAT2 is a "trigger and tracking"front-end ASIC, designed primarily for the readout of sensors in the TOTEM experiment of LHC.

The VFAT2 chip has been designed in quarter micron technology and has two basic functions. The first (Trigger) is to provide programmable "fast OR"information based on the region of the sensor hit. This can be used for the creation of a trigger and in CMS it provides input to the first level trigger (LV1A). The second function (Tracking) is for providing precise spatial hit information for a given triggered event.

TOTEM itself comprises three operating regions each employing a different sensor technology to detect charge from traversing minimum ionising particles (MIPs). Silicon strips, Gas Electron Multipliers (GEM) and Cathode Strip Chambers (CSC) are the technologies used each having different electrical characteristics. VFAT2 has been designed to provide the charge readout and low noise MIP discrimination for all 3 sensor technologies.

VFAT2 has 128 low noise input channels which after discrimination provide binary "hit"information which is stored until a trigger is received. The storage capacity enables trigger latencies of up to 6.4us (< 256 clock periods at 40 MHz), simultaneously store data for up to 128 triggered events and enable continuous dead time free operation with up to 100kHz Poisson distributed trigger rates. Time and event tags are added to the triggered data which are then read from the chip in the form of digitized data packets at 40 Mbps.

VFAT2 has many programmable functions controlled through an I2C interface. These include : internal biasing of analog blocks via 8 bit DACs, individual channel calibration via an internal test pulse with 8 bit programmable amplitude, calibration test pulse phase control, operate with positive or negative detector charge, 8 bit global threshold plus a 5 bit trim DAC threshold adjust on each channel, multiple possibilities for channel grouping for the "Fast OR"outputs, variable latency, various test modes plus an automatic self test of the digital memories. Chip status information including occupancy and SEU rates can be read via I2C.

For robustness against single event upsets (SEU), the digital parts of VFAT2 have been designed with hamming encoding for the SRAMs and triplication logic for the I2C interface and control logic. All analog circuitry employs layout techniques that reduce threshold voltage shifts under ionising radiation.

A major design challenge was to integrate the multitude of digital functions without having a significant impact on the analog performance. Stringent design techniques to "deafen the listener"and "silence the talker" have been employed to all analog and digital modules.

Measurements from the chip show all modules to be 100% functionally correct. The shaper has a peaking time of 22ns. The expected front-end noise performance of approximately 500e + 50e/pF is maintained. The total power consumption is 572mW.

VFAT2 has successfully integrated complex analog and digital functions into a single ASIC without compromising noise performance. This paves the way to future (post LHC) designs which will require further integration still.

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