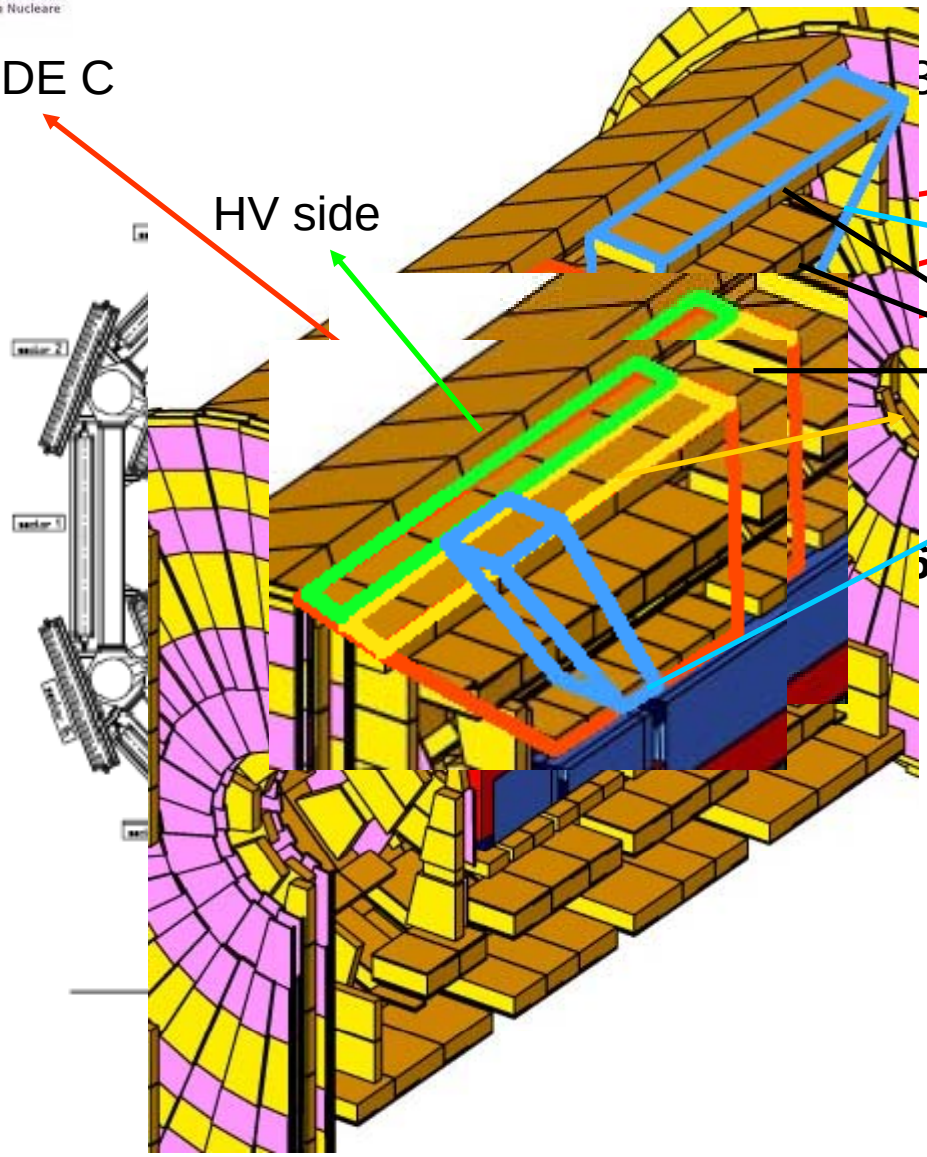
Sector Logic Board

The ATLAS Muon Trigger Sector Logic/RX Data Acquisition Board

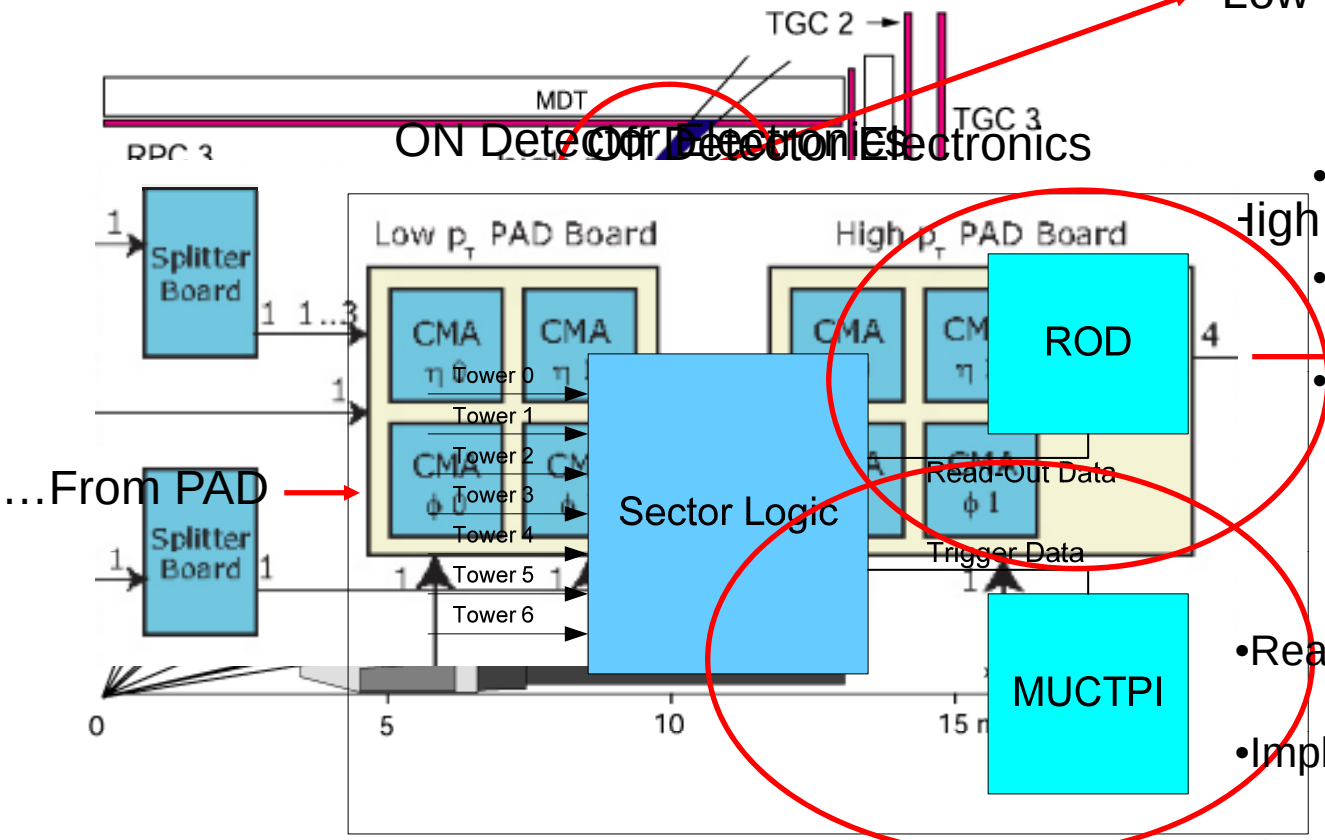
Author: Federico Spila

INFN Rome

1/13 LVL1 Muon Barrel Trigger



2/13 Lvl1 Trigger Electronics



Low Pt PAD BOX

ON Detector Electronics

•Read Read-Out Data

High Pt PAD BOX

•Implement Event Building

To Sector Logic …

•Send Output Data to ROD

…From PAD

•Read Trigger Data

•Implement Trigger algorithm

•Send Output Data to MUCTPI

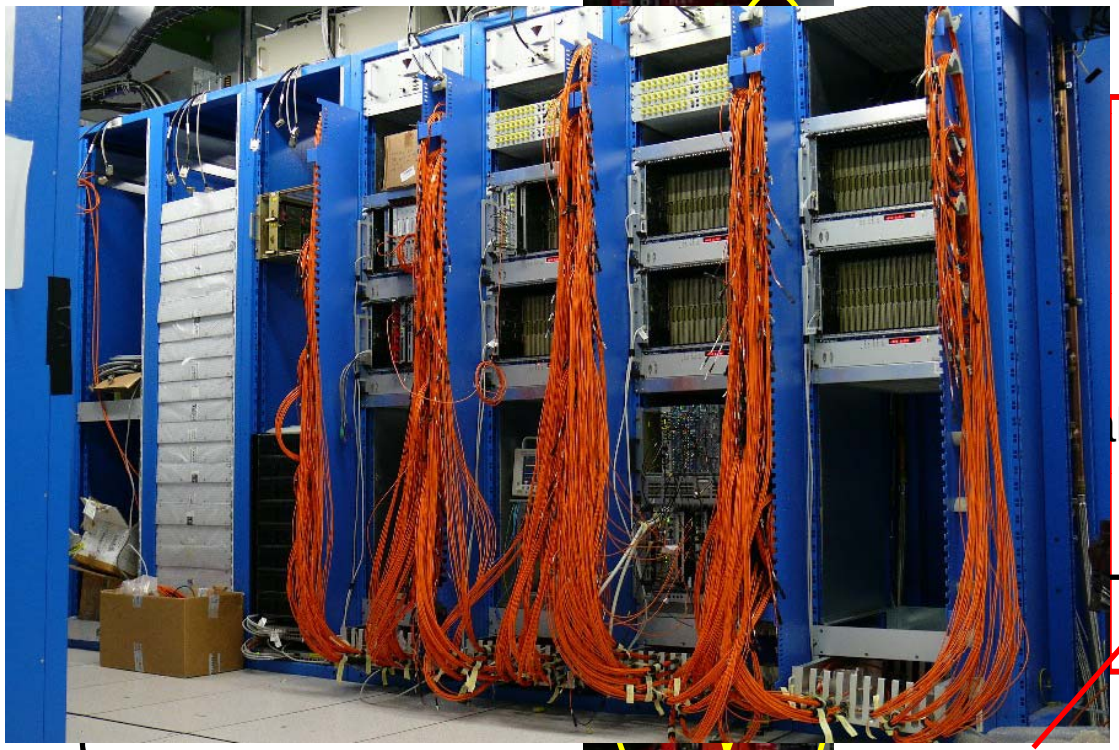
3/13 VME Crates

MUCTPI-Interface

Sector Logic

USA 15 Room 16 VME Crates

ead-Out Data: Backplane Connection



VME CRATE

Each takes data from
2 Geometrical Sectors

Each takes data from
2 Trigger Sectors

MUCTPI

l receivers

Central Trigger
Processor

In Total 64 Sector Logic
Boards

L1 Barrel Trigger

L1 End-Cap Trigger

External

VDS BUS

…To MUCTPI board

4/13 ROD-BUS

SL <-> ROD

Real ROD Block

- Sends Read-Out Data
- Receives TTC Signals

LAS Geometrical Sectors

2. ROD-BUS mounted on a VME Back-Panel
3. ROD
4. Sector Logic
   - Sends Trigger Data
5. MUCTPI-Interface
   - Receives Service Signals

ch ROD reads 2 Sector Logics

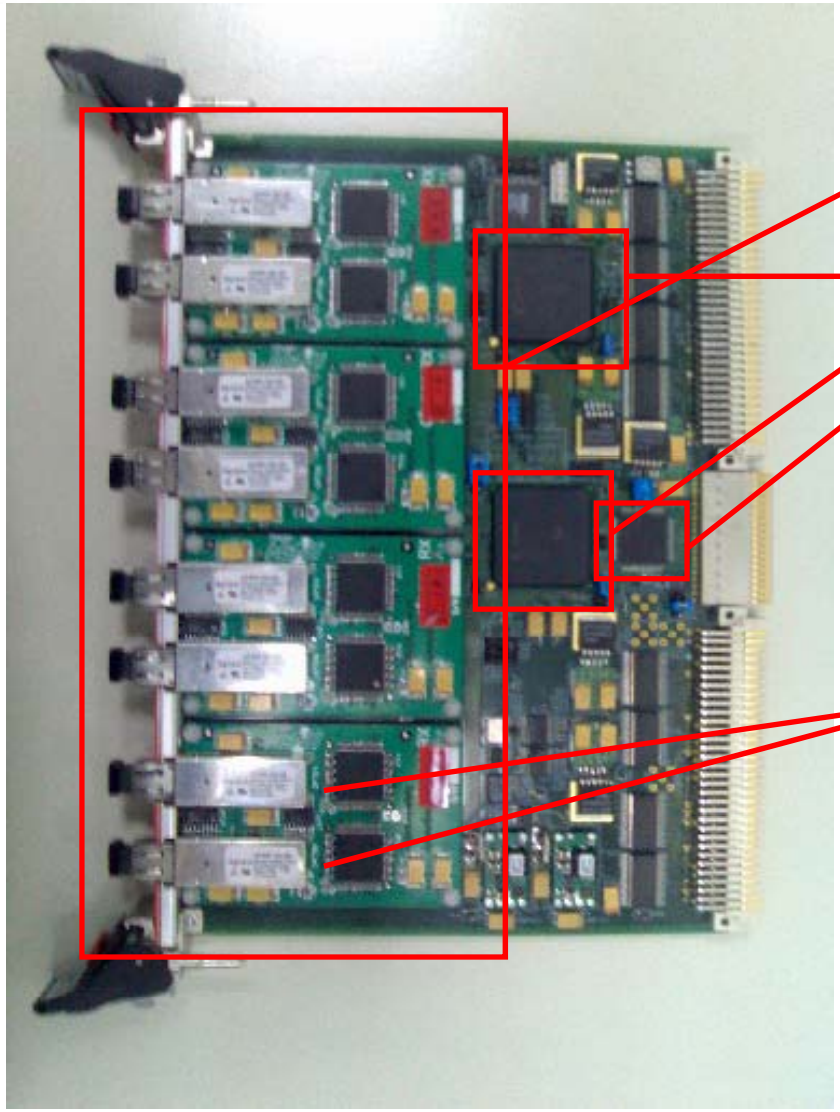
SL <-> MUCTPI-Interface

Sector Logic - ROD

Sector Logic - ROD

MUCTPI - Interface

5/13 Sector Logic Schema



4 G2Link RX Cards

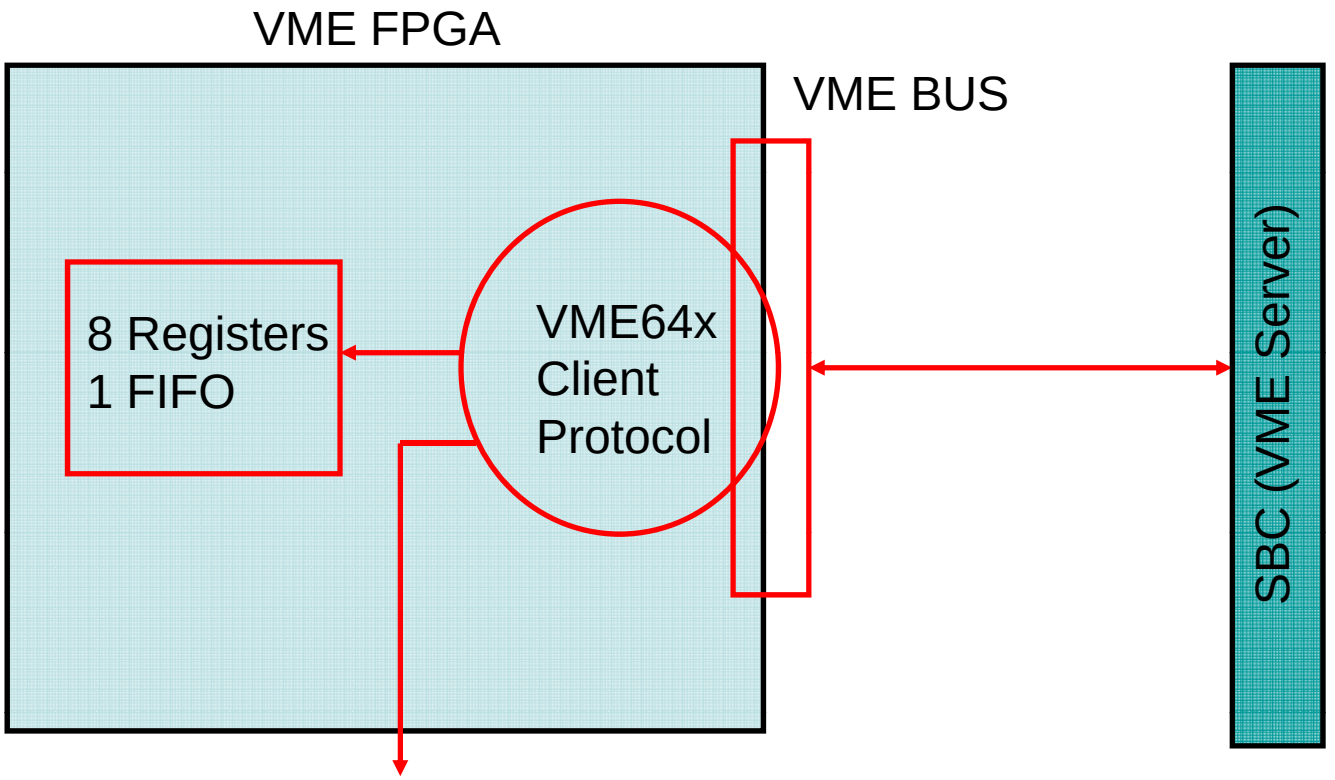
Xilinx Virtex2 XC2V 1000
Xilinx Virtex2.XC2V 2000
Serializer chip
VME Communication
JTAG
Other Services features

40 bit TTL input
->
8 bit LVDS output stream

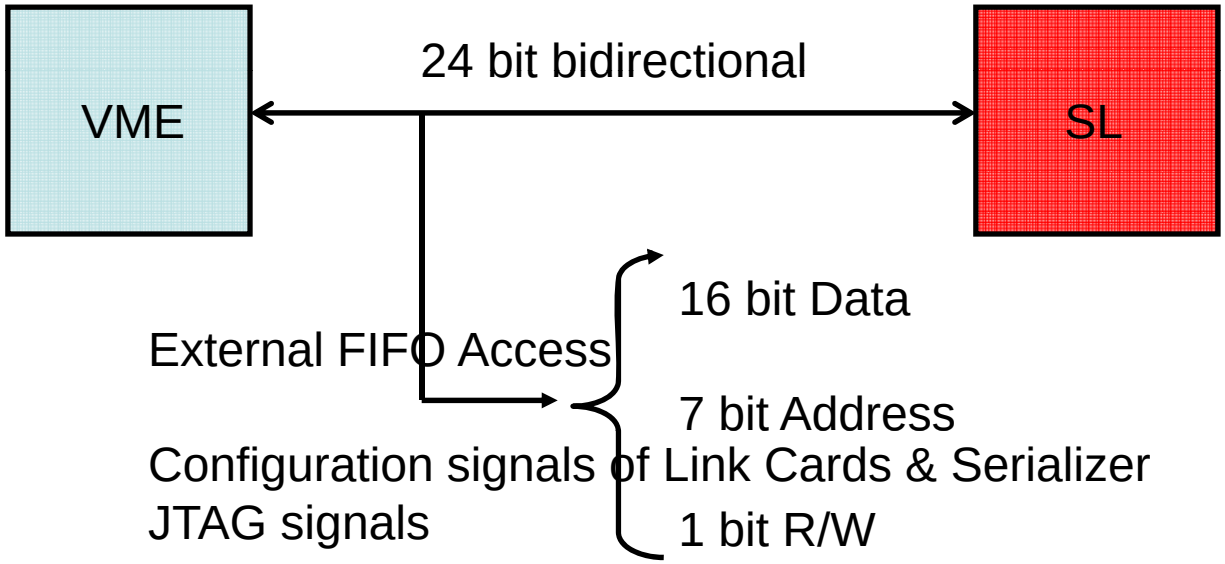
Each with 2 Optical link receivers
Speedrate 240 Mbyte/s

VME FPGA
SL FPGA

6/13 VME FPGA Firmware



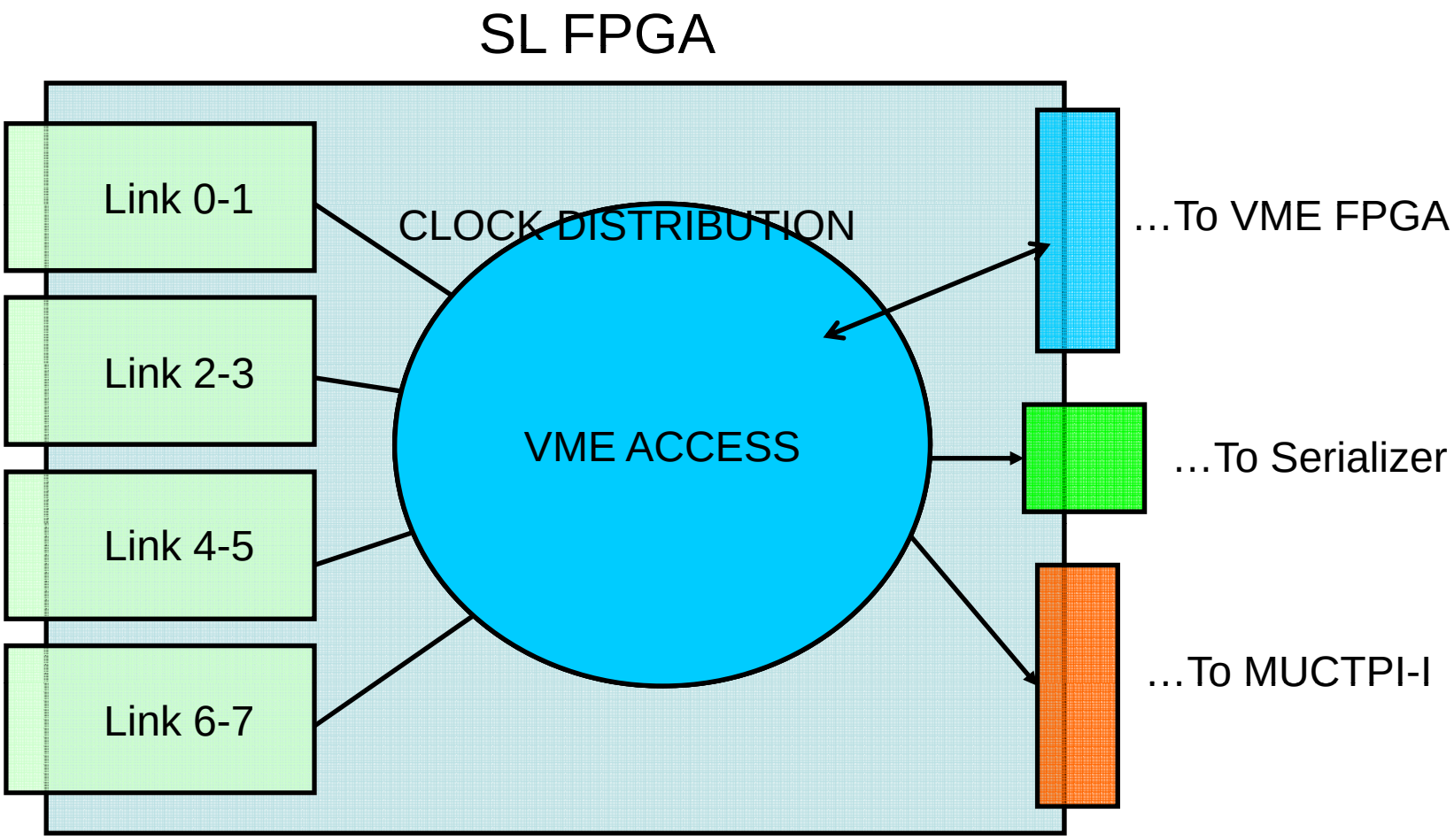
7/13 Master-Slave Protocol



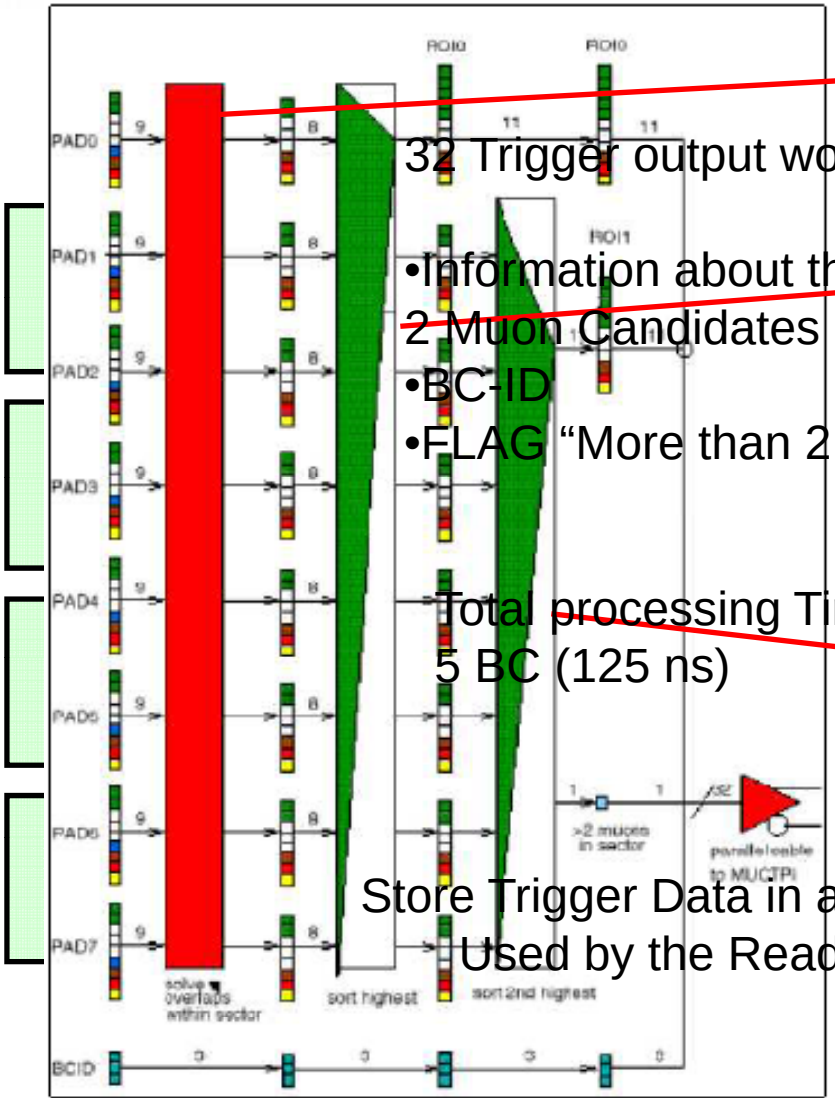
VME FPGA is the Master

Transmit first the low significant 2 bytes,
after the more significant 2 bytes

8/13 SL FPGA Firmware



9/13 Trigger Logic



lidate is detected

olves Trigger data

s

32 Trigger output word

- Information about the 2 Muon Candidates
- BC-ID
- FLAG "More than 2 candidates"

OGIC

Total processing Time:
5 BC (125 ns)

BC 1:
Solves the PAD Overlap

16 bit Trigger Word

BC 2:
Detects the first High Pt muon using a 8x7 Matrix comparator

- BC-ID
- Overlap
- Threshold
- ROI

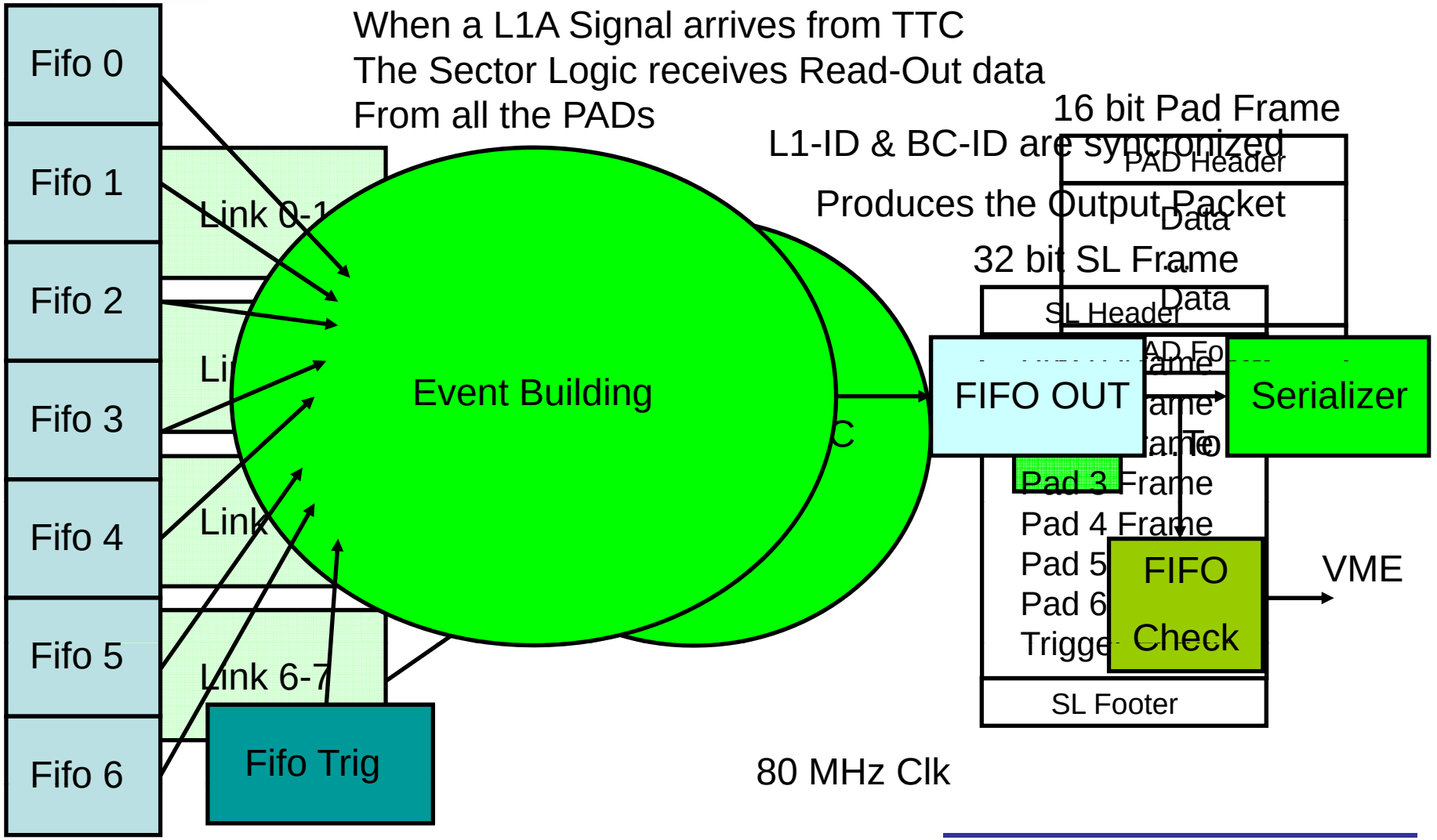
BC 3:
Detects the second High Pt muon using a 8x6 Matrix comparator

…To MUCTPI-I

Store Trigger Data in an internal FIFO
Used by the Read-Out Logic

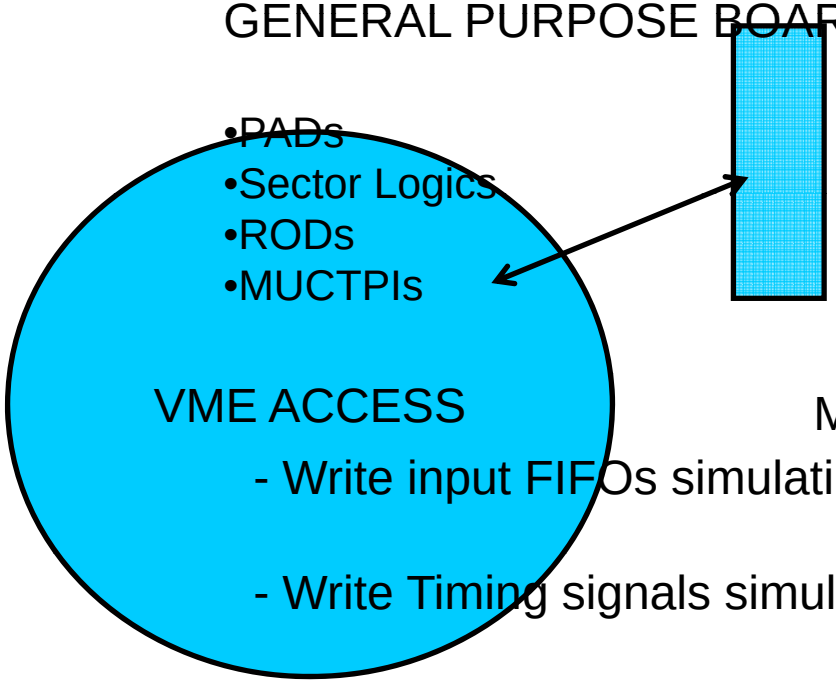
10/13 Read-Out Logic

When a L1A Signal arrives from TTC
The Sector Logic receives Read-Out data
From all the PADs



11/13 VME SL Logic

GENERAL PURPOSE BOARD for Testing

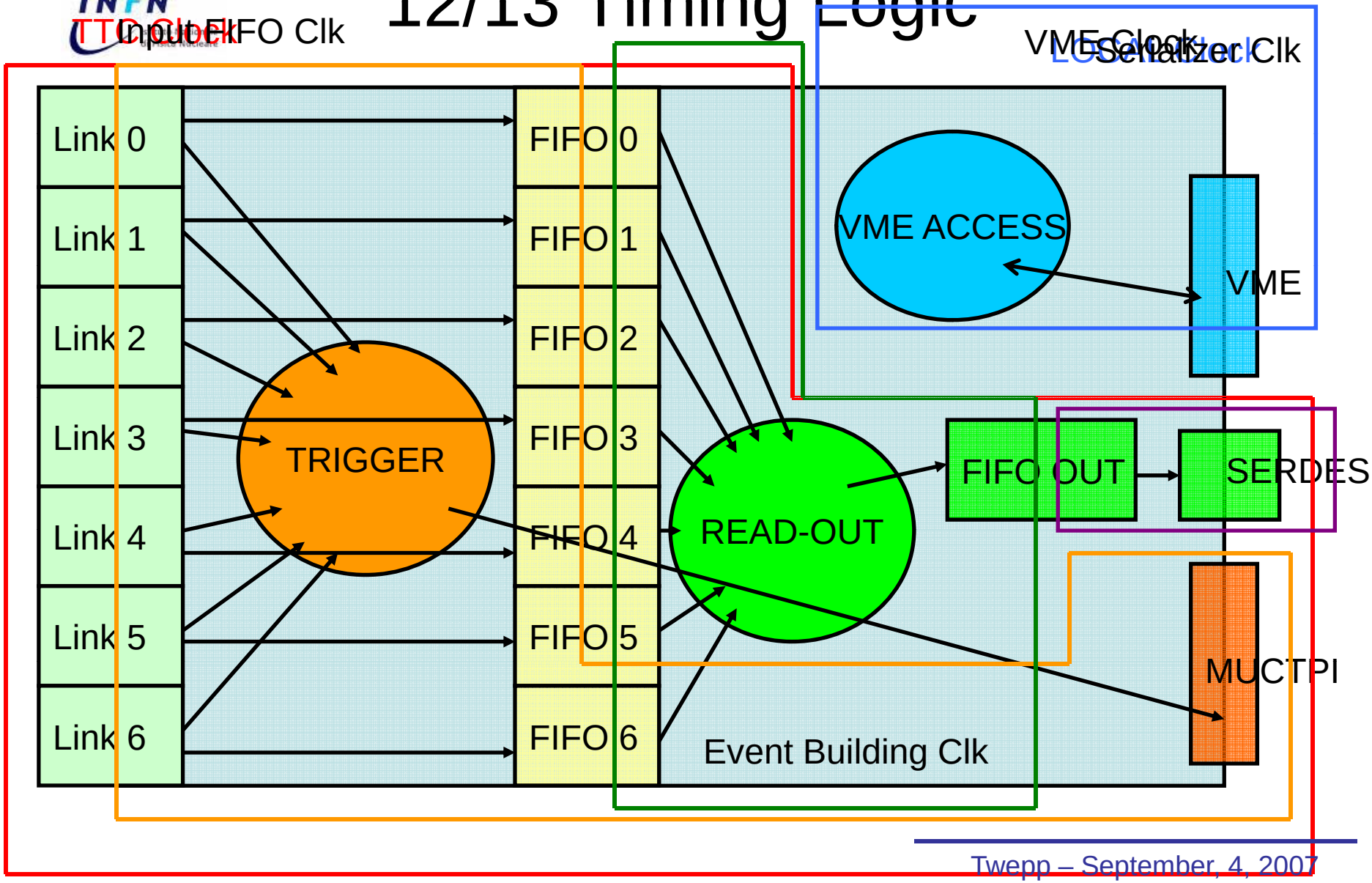


…To VME FPGA

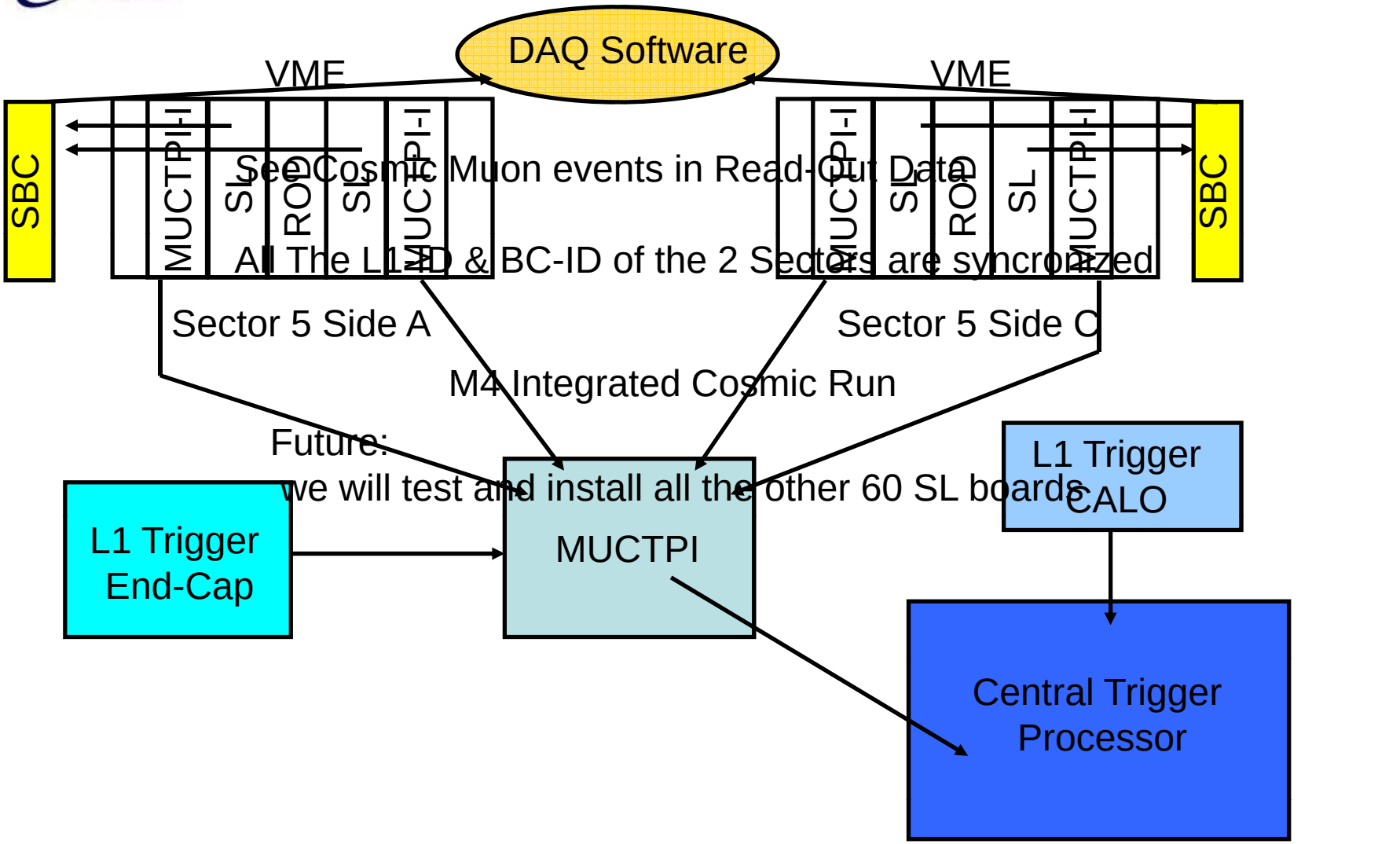
Master-Slave Custom Protocol

- Write input FIFOs simulating PADs
- Write Timing signals simulating the TTC
- Write the Output Data directly to ROD
- Write the Output Data directly to MUCTPI
- Mounting G2Link TX, we can emulate the PAD

12/13 Timing Logic



13/13 Conclusions & M4 RUN



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