Sector Logic Board

The ATLAS Muon Trigger Sector Logic/RX Data Acquisition Board

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1/13 LVL1 Muon Barrel Trigger

- 3 Planes of RPC Detectors
- Inner, Middle-pivot, Outer
- SIDE A, SIDE C, RO Side
- Each with 6 or 7 Chambers
- Trigger Tower
- 16 Sectors on the Azimuthal Plane
- 32 Geometrical Sectors
- 6 or 7 Trigger Towers
- 64 Trigger Sectors

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2/13 Lvl1 Trigger Electronics

- **ON Detector Electronics**
  - Read Read-Out Data
  - Implement Event Building
  - Send Output Data to ROD

- **High Pt PAD BOX**
  - To Sector Logic
  - Send Output Data to MUCTPI

- **Low Pt PAD BOX**
  - Read Trigger Data
  - Implement Trigger algorithm

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3/13 VME Crates

MUCTPI-Interface
USA 15 Room 16 VME Crates

Sector Logic
Head-Out Data: Backplane Connection

Each takes data from 2 Geometrical Sectors

Each takes data from 2 Trigger Sectors
Central Trigger Processor

In Total 64 Sector Logic Boards

L1 Barrel Trigger
L1 End-Cap Trigger

...To MUCTPI board

External Cables -> LVDS BUS

LVDS BUS...To MUCTPI board

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4/13 ROD-BUS

SL <-> ROD
Real ROD Block

• Sends Read-Out Data

SL <-> MUCTPI-Interface

• Sends Trigger Data
• Receives Service Signals

ROD BUS mounted on a VME Back-Panel

• Receives TTC Signals

LAS Geometrical Sectors

Each ROD reads 2 Sector Logics

2. Sector Logic
3. ROD
4. Sector Logic
5. MUCTPI-Interface

ROD BUS

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5/13 Sector Logic Schema

- 4 G2Link RX Cards
- Xilinx Virtex2 XC2V 1000
- Xilinx Virtex2 XC2V 2000
- Serializer chip
- VME Communication
- JTAG
- Other Sector logic features
- 8 bit LVDS output stream
- Each with 2 Optical link receivers
- Speedrate 240 Mbyte/s
- VME FPGA
- SL FPGA

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6/13 VME FPGA Firmware

VME FPGA

VME BUS

SBC (VME Server)

SL FPGA

8 Registers
1 FIFO

VME64x Client Protocol

Custom Master-Slave Protocol

All Registers & FIFOs
32 bit length
7 bit Address

44 Registers
12 FIFOs

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7/13 Master-Slave Protocol

VME FPGA is the Master

Transmit first the low significant 2 bytes, after the more significant 2 bytes
8/13 SL FPGA Firmware

SL FPGA

- Link 0-1
- Link 2-3
- Link 4-5
- Link 6-7

CLOCK DISTRIBUTION

VME ACCESS

...To VME FPGA

...To Serializer

...To MUCTPI-I
9/13 Trigger Logic

When a MUON candidate is detected:
- **BC 1:** Solves the PAD Overlap
  - 16 bit Trigger Word
  - Link 0-1

The Sector Logic receives Trigger data from 1 or more PADs:
- BC 2:
  - 32 Trigger output word
  - Information about the 2 Muon Candidates
  - BC-ID
  - Threshold
  - ROI
  - Link 0-1

Detects the first High Pt muon using an 8x7 Matrix comparator:
- **BC 3:**
  - Detects the second High Pt muon using an 8x6 Matrix comparator
  - Total processing Time: 5 BC (125 ns)

Store Trigger Data in an internal FIFO:
- Used by the Read-Out Logic
- ...To MUCTPI-I

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10/13 Read-Out Logic

When a L1A Signal arrives from TTC
The Sector Logic receives Read-Out data
From all the PADs

Fifo 0
Fifo 1
Fifo 2
Fifo 3
Fifo 4
Fifo 5
Fifo 6

Link 0-1
Link 2-3
Link 4-5
Link 6-7
Fifo Trig

Event Building

L1-ID & BC-ID are synchronized
Produces the Output Packet

16 bit Pad Frame
32 bit SL Frame

Pad Header
SL Header
AD Frame
AD Frame
AD Frame
AD Frame
Trigger Frame
Trigger Frame
Trigger Frame
Trigger Frame

PAD Footer
Pad 0 Frame
Pad 1 Frame
Pad 2 Frame
Pad 3 Frame
Pad 4 Frame
Pad 5 Frame
Pad 6 Frame
Trigger Frame

FIFO OUT
Serializer

80 MHz Clk

Fifo Check
VME

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11/13 VME SL Logic

GENERAL PURPOSE BOARD for Testing
- PADs
- Sector Logics
- RODs
- MUCTPIs

VME ACCESS
- Write input FIFOs simulating PADs
- Write Timing signals simulating the TTC
- Write the Output Data directly to ROD
- Write the Output Data directly to MUCTPI
- Mounting G2Link TX, we can emulate the PAD

...To VME FPGA

Master-Slave Custom Protocol
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12/13 Timing Logic

- Timing Logic
- FIFO 0
- Link 0
- TTC Clock
- LOCAL Clock
- Input FIFO Clk
- VME ClockSerializer Clk
- VME ACCESS
- FIFO 1
- Link 1
- FIFO 2
- Link 2
- FIFO 3
- Link 3
- TRIGGER
- FIFO 4
- Link 4
- READ-OUT
- FIFO 5
- Link 5
- FIFO OUT
- Link 6
- Event Building Clk
- FIFO OUT
- SERDES
- MUCTPI
- VME
- Twepp – September, 4, 2007
13/13 Conclusions & M4 RUN

See Cosmic Muon events in Read-Out Data

All The L1-ID & BC-ID of the 2 Sectors are synchronized

Sector 5 Side A

Sector 5 Side C

Future:
we will test and install all the other 60 SL boards.

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THE END