Contribution ID: 65 Type: Oral

The ATLAS Barrel Level-1 Muon Trigger Sector-Logic/Rx off-detector trigger and acquisition board

Tuesday, 4 September 2007 12:35 (25 minutes)

The ATLAS experiment uses a system of three concentric Resistive Plate Chambers (RPC) detector layers for the level-1 muon trigger in the air-core barrel toroid region. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The on-detector electronics that provides the trigger and detector readout functionalities collects input signals coming from the RPC front-end.

Trigger and readout data from on-detector electronics are sent via optical fibres to the off-detector electronics. Six or seven optical fibres from one of the 64 trigger sectors go to one VME Sector-Logic/RX module, that latter elaborates the collected trigger and readout data, and sends readout and trigger data respectively to the Read-Out Driver modules and to the Central Level-1 Trigger.

We present the functionality and the implementation of the VME Sector-Logic/RX module, and results from the first cosmic ray run data collected using this module.

Summary

The ATLAS experiment uses a system of three concentric Resistive Plate Chambers detectors layers for the level-1

muon trigger in the air-core barrel toroid region. The trigger classifies muons within different programmable transverse momentum ranges, and tags the identified tracks with the corresponding bunch crossing number. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road.

which defines the transverse momentum cut.

The full experiment is divided in 64 trigger sector. One sector side is composed by three planes of RPC detectors (inner, middle-pivot and outer), each plane being composed normally of six or seven adjacent RPC detectors. Δ

trigger tower is composed by three half RPC detectors (inner, pivot and outer) belonging to the same trigger sector, so that there are six or seven trigger towers per trigger sector.

For every Trigger Tower, trigger and readout data, coming from on-detector electronics, are sent via optical fibres

to the off-detector part of the trigger. Six or seven optical fibres (one per Tower), coming from one trigger sector

go to one VME Sector-Logic/RX module (from now "Sector Logic"), which elaborates the collected trigger and readout data, and sends readout and trigger data respectively to the Read-out Driver (ROD) module and to the Muon-Central Trigger Processor Interface (MUCTPI) module.

Sector Logic modules are mounted on VME Crates in USA 15, far form the detector. There are 16 VME Crates, each with 4 Sector Logic (for a total of 64 Sector Login, one per ATLAS Trigger Sector).

Data communication from SL to others modules are made using the ROD-BUS (a custom VME Backpanel that enables adjacent slot in the same VME crate to share a custom data-bus.

Every Crate has two "5-slot ROD-BUS", on which modules are mounted in this order: 1 Muctpi Interface module:

1 SL module; 1 ROD module; 1 SL module; 1 Muctpi Interface module.

Muctpi Interface is a module that receives trigger data from SL and drives a parallel LVDS bus to reach the MUCTPI module mounted in USA 15 at a 10m distance.

Every SL receives data from 8 Optical link from the Trigger Towers elaborates, and send data to 1 Muctpi Interface on 1 side and one ROD on the other side:

• 8-bit trigger data per link are processed in a pipe-line 3 clock periods long, that produce a 32 bit word with information about the 2 highest pT muon candidate, and the Bunch Crossing value.

Trigger data so generated are sent to MUCTPII Interface.

• Up to 8 16-bit word wide read-out "Pad Fragment", are temporary stored using internal FIFOs, and are processed to generate the 32 bit "SL Fragment" (that contains all the Pad fragments of the same Trigger event). SL Fragments are sent to ROD Module via a Serializer chip, which provides LVDS data transmission at 1280

Mbps speed-rate.

The Sector Logic processor core is based on two Xilinx FPGA, one dedicated to VME Communications and to other

services (JTAG, I2C, etc...). The other FPGA is dedicated to the trigger and read-out logic.

The first Sector Logic modules are mounted in USA 15 together with some ROD and MUCTPI modules, and will be

used to collect data of the first ATLAS Cosmic Ray Run. The result of this run will be presented.

Primary author: Dr SPILA, Federico (INFN, Sezione di Roma I)

Co-authors: Dr ALOISIO, Alberto (INFN, Sezione di napoli); Dr SALAMON, Andrea (INFN, Sezione di Roma II); Dr PETROLO, Emilio (INFN, Sezione di Roma I); Mr GENNARI, Ettore (INFN, Sezione di Roma I); Dr PASTORE, Francesca (INFN, Sezione di Roma I); Dr VARI, Riccardo (INFN, Sezione di Roma I); Dr VENEZIANO, Stefano (INFN, Sezione di Roma I)

Presenter: Dr SPILA, Federico (INFN, Sezione di Roma I)

Session Classification: Parallel session B1 - Trigger 1 Atlas