A Trigger/Timing Logic Unit for ILC Test Beams

Introduction

The Trigger/Timing Logic Unit (TLU) is designed to act as a interface between a prototype detector and the beam-trigger at a test beam: It is a **"NIM crate replacement with extras".** The TLU was developed as part of the LCFI and EUDET programmes.

Functionality:

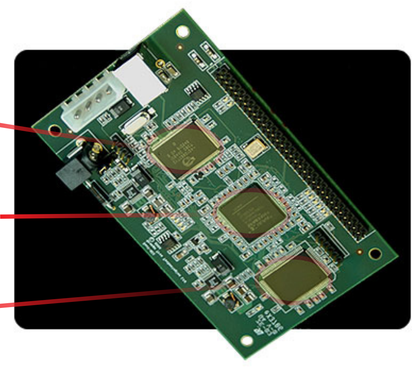
- Accept input from beam triggers and relay to one or more devices under test (DUT).
- Inhibits triggers when one or more DUT busy.
- Records a 64-bit time-stamp for each trigger issued so that a DUT which needs a trigger can be mixed with a "triggerless" DUT that identifies data with a timestamp rather than a trigger number.

Design Aims:

- Place as few burdens on user as possible.
- Provide maximum flexibility while remaining simple to use.
- Low cost.

Implementation

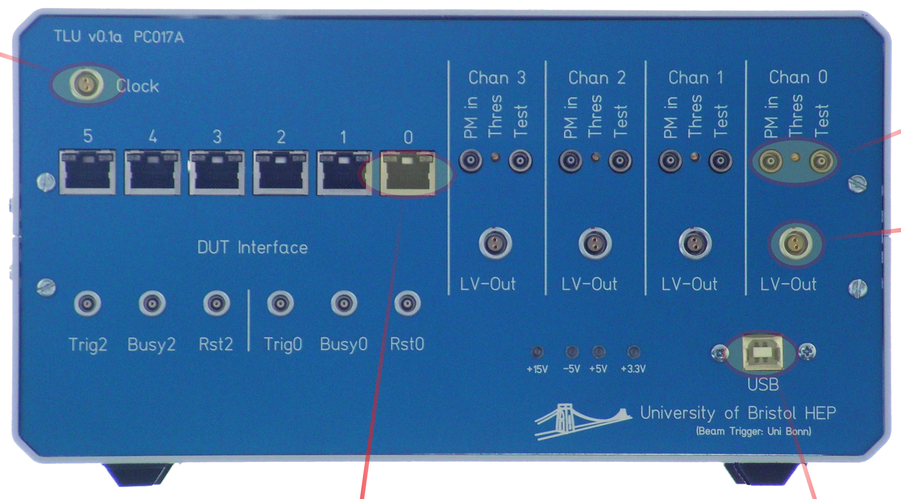
- Uses "COTS" FPGA prototyping module (ZestSC1 from Orange Tree). Reduces hardware design time. Example firmware available to reduce firmware develpment time.
- Cypress "EZ-USB FX2LP" CY7C68013 microcontroller used for FPGA configuration and USB 2.0 interface to host.
- Based around Xilinx Spartan 3 device (xc3s1000ft256).
- 8MByte low-latency (ZBT) SRAM available to store timestamps.



- Firmware for FPGA written in VHDL. Simple enough to be synthesized by freely downloadable "Webpack" tool.
- Even in small quantities, the total cost of a TLU is relatively small (~ €1500).

Clock

- Can either use internal 48MHz crystal clock for timestamp counter or external clock.
- Clock source selectable under software control.
- Differential LVDS or LVPECL signal levels.
- Instead of recieving an external clock the TLU can be configured to transmit the internal clock from the clock connector.



Trigger Input

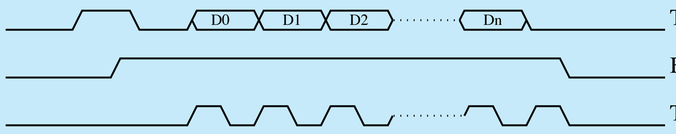
- Simple threshold discriminator allows photomultiplier, NIM and LVTTL input levels to be recieved.
- Low voltage output for powered PMT bases. (15V by default, but eaily changable to other voltages)
- The four inputs can be used in any combination of "and" , "or" , "veto" logic.

Interface to DUT

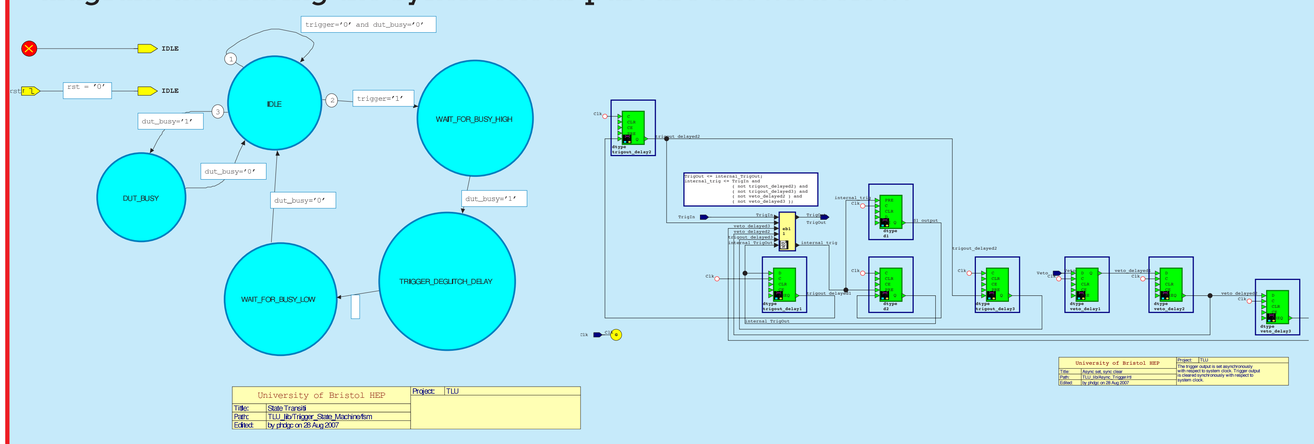
The device under test (DUT) is interfaced to the TLU using four LVDS level signals:

- Trigger (from TLU)
- Busy (from DUT)
- Clock (from DUT)
- Reset (from TLU)

Two handshake modes: simple trigger/busy handshake or a mode where the DUT reads out the trigger number from the TLU. These modes are dynamically selectable by the DUT. The trigger readout mode is illustrated below:



In order to have fixed latency between the incoming trigger and the trigger sent to the DUT, whilst avoiding potential race conditions, the trigger is set asynchronously and cleared synchronously with respect to the system clock. A block diagram of the logic used for the asynchronous part of the trigger, together with the state-transition diagram describing the synchronous part are shown below:



Host Interface

- EZ-USB provides USB 2.0 interface.
- Two access methods: 8-bit registered and 16-bit block transfer.
- Register access is used for setup and control.
- Block transfer is used to read block of timestamps. Transfer rates of ~ 30MByte/s measured)

Future Directions?

- Configure FPGA from internal memory (allowing stand-alone operation).
- Add alphanumeric display and switches for configuation via front panel (needed for stand-alone operation).
- Use clock doubling and double edged clocking to improve timestamp resolution. Can be reduced to 2.5ns with no hardware changes, currently 20ns.
- Could implement a TLU with different hardware (e.g. CAEN V1495) but same physical interface to DUT (four LVDS signals) and same address map

References

EUDET: Detector R&D Towards the ILC, http://www.eudet.org
LCFI: Linear Collider Flavour Identification, http://hepwww.rl.ac.uk/lcfi
TLU: Trigger/Timing Logic Unit, http://www.eudet.org/zms/content/e62/e144/e190/eudet-memo-2007-02.pdf
ZestSC1: FPGA USB Board, http://www.orangetreetech.com/fpga_board_zestsc1.html
EZ-USB: CY7C68013A FX2LP USB Microcontroller, http://www.cypress.com
Xilinx: Spartan 3 FPGA, http://www.xilinx.com/spartan3

David Cussans, TWEPP, Prague, 3-7 Sept, 2007