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A Trigger/Timing Logic Unit for ILC Test-beams

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Summary

Introduction:

ILC not a triggered experiment, but during detector development it may be useful to operate in a triggered mode. A Trigger/Tagging Logic Unit (TLU) is described which allows triggered operation, with option of smooth transition to triggerless, data-driven mode. The TLU is being developed as part of the EUDET programme to develop test-beam infrastructure for ILC detector development.

At detectors with a pipe-lined trigger, for example the LHC and HERA experiments, the front-end links operate at a multiple of bx-clock to minimize latency for the first-level hardware trigger. Because the ILC detectors will not be triggered locking the link clock frequency need not be a multiple of the ILC bunch-crossing clock, allowing the use of COTs data-link technology. However, in data-driven operation a clock and control signals must still be distributed to the detectors to enable the data to be time-stamped where it modes from pipelined, fixed latency, to buffered data-driven.

Aims:

Because the ILC detectors will operate in a data-driven, triggerless mode any triggered test-beam operation for development of detectors should be as simple as possible - since it is not a “stepping stone” to the eventual system.

Simple and low cost enough to be widely distributed. Ideally, each group developing detectors should be able to have at least on TLU. It is hoped to place few *demands* on user whilst being as flexible as possible.

Description:

The TLU will be able to operate in two modes. Firstly a “classic” trigger/busy triggered mode with hand-shake. Secondly as a “Tagging” logic unit providing the time-stamp information needed for a data-driven system.

In the triggered mode, the TLU and each device has four signals connecting them: Trigger/Busy/Reset/DUT-Clock. Once a trigger has been sent from the TLU to a device and a busy signal sent from the device to the TLU the device can optionally clock out trigger information from the TLU on the trigger line.

In “tagging” (data driven) mode mode a separate low-jitter clock tree fans out a system-level clock to all test-beam devices. The TLU receives the system clock and produces a manchester encoded serial data stream which is fanned out to all system devices together with the system clock. The simple encoding, at the bit-rate equal to the system clock, allows the serial data to be decoded in an

FPGA without the aid of an external clock recover unit. The serial data stream carries spill-on/spill-off (bunch train present) information and the spill(bunch-train) number.The TLU also keeps a record of time-stamps for incoming triggers.

Implementation:

Number of units is likely to be relatively low and the life-span is modest (˜ 5 years). This suggests the use of a COTS FPGA module coupled to a custom motherboard and using off-the-shelf USB interface firmware and software drivers rather than totally custom hardware and firmware/software. Cypress EZ-USB microcontroller with USB interface used to interface beween Xilinx Spartan xc3s1000 FPFGA and USB2.0.

Interface to the test-beam device under-test is via RJ45 connectors with LVDS levels. There are six DUT interfaces. Four 50-Ohm terminated coaxial connectors accept NIM,TTL or photo-muliplier level pulses and receive a trigger for each particle passing through the test-beam. The arrival of each trigger is time-stamped. In triggered mode the arrival of a trigger will cause a trigger to be issued to active DUTs, unless the DUT have indicated that they are busy.

The FPGA is configured via the USB interface. A memory-mapped interface is used for set up via the host interface and block transfer is used to transfer time-stamps from the TLU to the host computer.

Status:

An implemention of the TLU suitable for triggered mode already exists and is due to be used in test-beam this year. The low-jitter clock distribution system needed for operation in “tagging” mode has not yet been constructed.

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