Development of SEU-robust, radiation-tolerant and industry-compatible programmable logic components

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Outline

- Motivation and objectives
- TID hardening
- SEU hardening
- PLD design description
- FPGA design description
- Experimental results for SEU-robust structures

Motivation

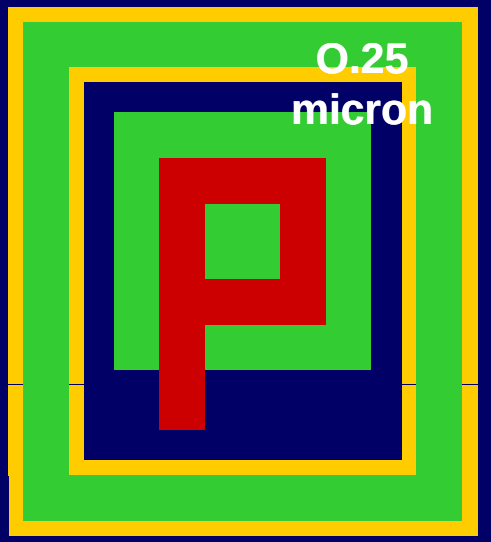
- High-Energy Physics would benefit from the availability of radiation-hard programmable logic
  - FPGAs
    - Fast design development
    - Flexibility (changing requirements, failure recovery, …)
  - PLDs
    - Glue logic, simple state machines
    - Hard fixes in the late stages of a project
- Commercial devices do not attain LHC radiation levels
  - >30 Mrad total dose
  - SEUs from intense flux of hadrons
    - ~10^{15} hadrons/cm^2 in 10 years LHC

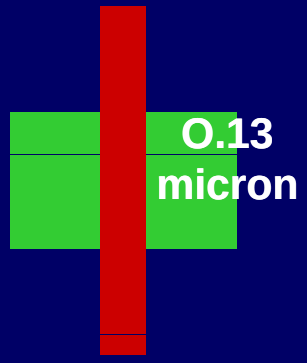
Objectives

- Programmable logic components
  - TID-tolerant to experiment upgrades inner tracker levels
  - Built-in SEU hardness
    - Configuration bank and user registers…
    - …protected at circuit level against SEUs
    - User can avoid utilization of SEU hardening techniques at HDL level and/or reconfiguration techniques for program restoration
- FPGA
  - compatible with an existing device, ~25k gates, 256 I/Os
  - in 0.13µm CMOS
- PLD
  - compatible with 16LV8 device, 10 inputs, 8 bidirectional
  - in 0.25µm CMOS

Total Ionizing Dose hardening

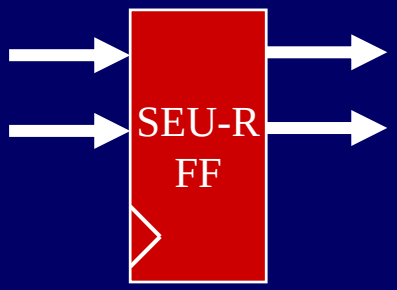
- Design practices for TID hardening
  - 0.25µm CMOS technology
    - Enclosed Layout Transistors
    - Guard-rings
  - 0.13µm CMOS technology
    - Intrinsically TID-hard
      - Faccio and Cervelli, "*Radiation-induced edge effects in deep submicron CMOS transistors*", IEEE Transactions on Nuclear Science, vol. 52, December 2005
    - Wide linear transistors (W>0.30µm)





Single-Event Upset hardening

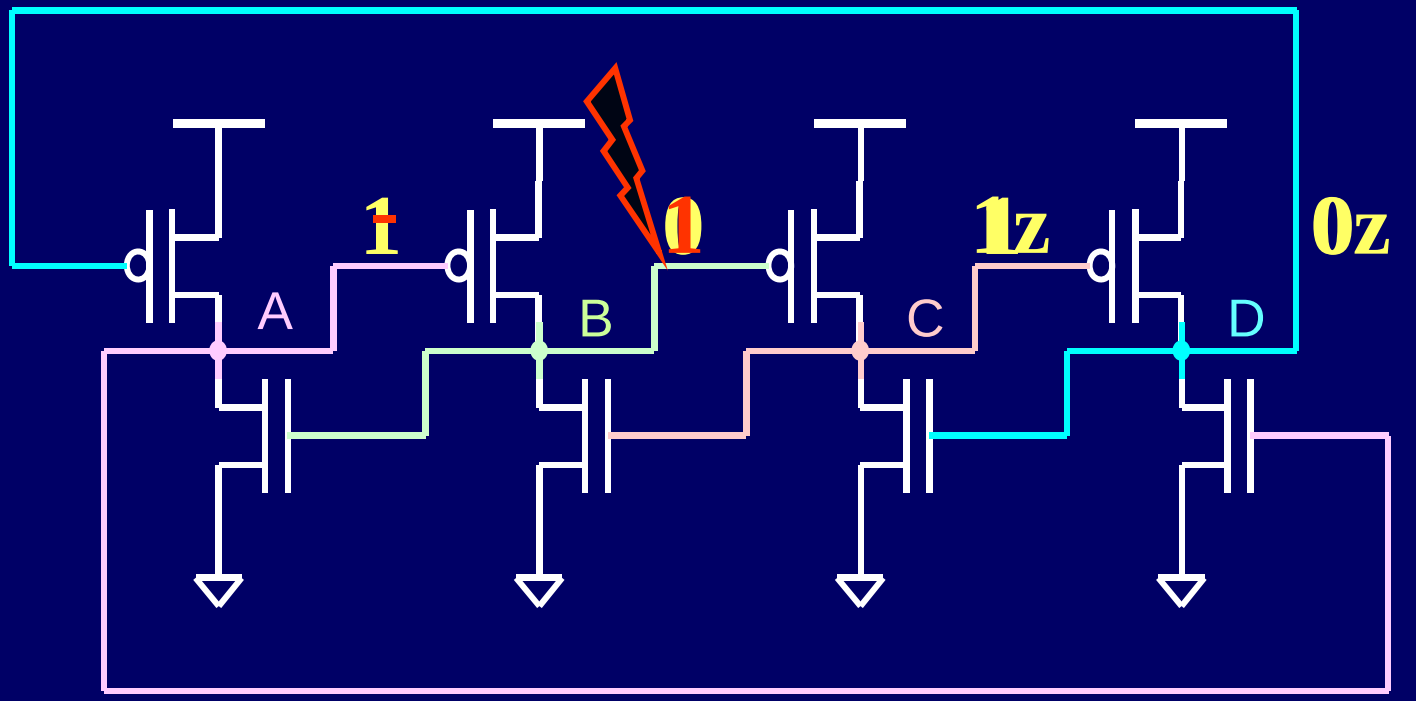
- Circuit level SEU protection
  - SEU-robust register
    - used for configuration storage
    - …and user data
  - Based on Dual-Interlocked Cell (DICE)



- Protection against Single-Event Transients (SETs)
  - Which occur in combinatorial logic
  - Duplication

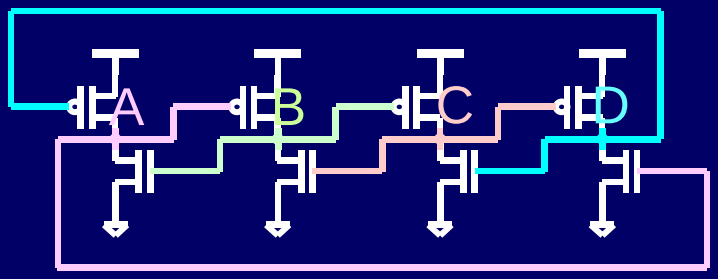
Dual-Interlocked Cell (DICE)

- 4 memory nodes
- Each memory node is correlated to 2 other memory nodes
  - Interlock
- Symmetric cell
  - Each node is equivalent to the others
- 2 stable states
  - (1,0,1,0)
  - (0,1,0,1)
- pMOS propagate right only low values
- nMOS propagate left only high values



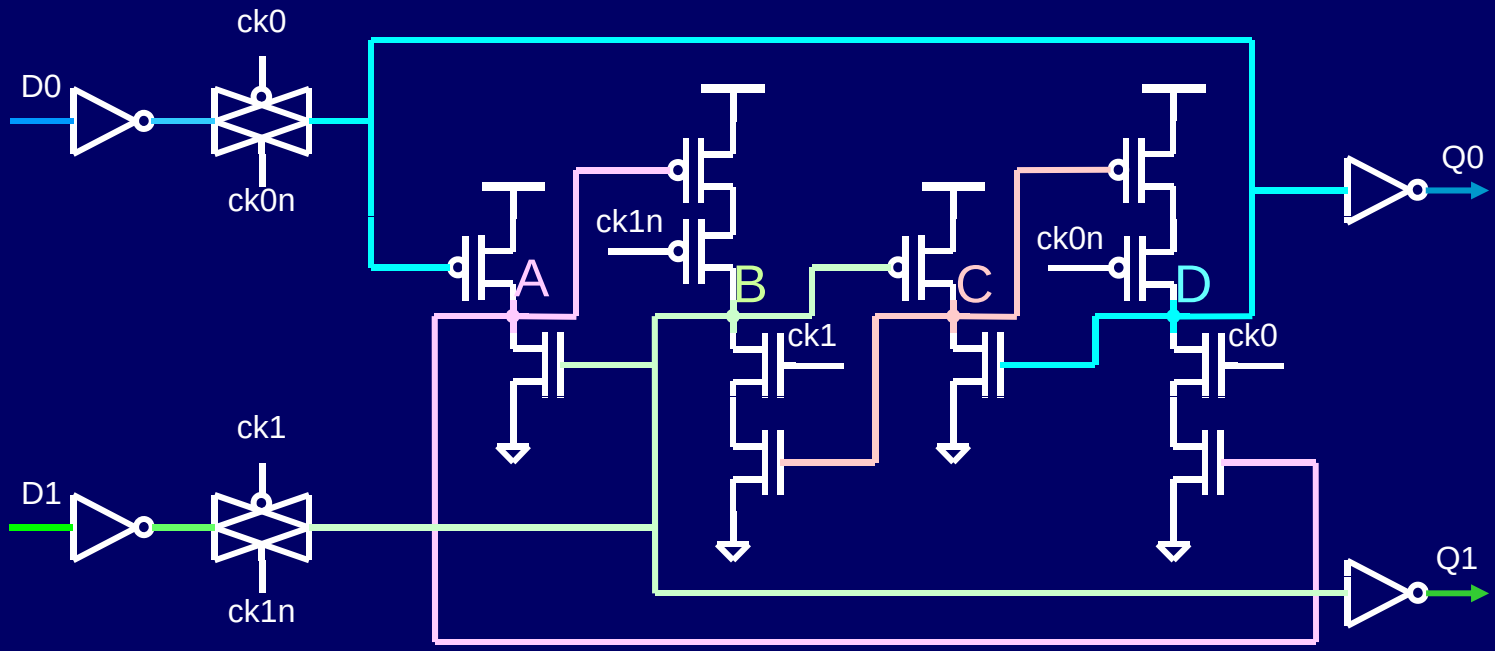
- Intrinsically immune to single-node particle hits
- Vulnerable to multiple-node particle hits

SEU-robust latch



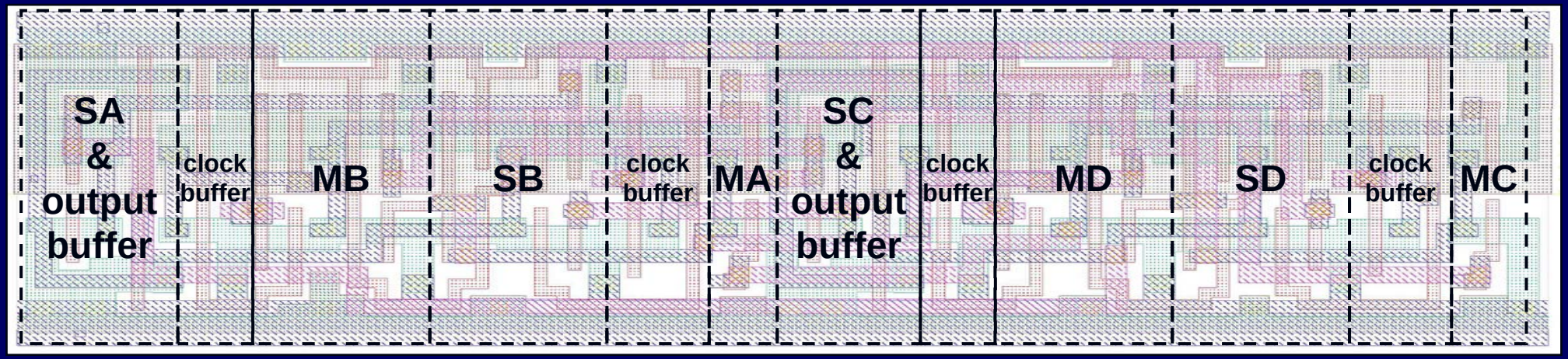
…add clock driven transmission gates to access memory nodes…

- Fully 2× redundant
  - 2 inputs
  - 2 outputs
  - 2 clock buffers
  - Normally they have the same logic levels

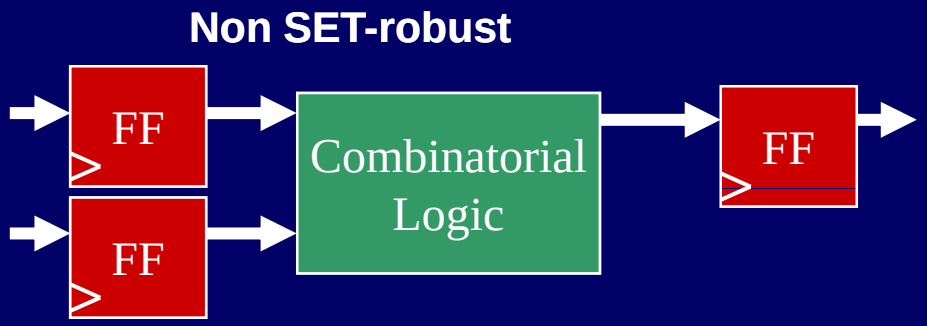


Register layout for SEU robustness

- SEU-register is composed by a master latch and a slave latch
  - Master nodes: MA, MB, MC, MD
  - Slave nodes: SA, SB, SC, SD
- Latch is vulnerable to multiple-node particle hits on correlated nodes
- The nodes of the two latches are interleaved in order to increase the distance between correlated nodes
  - Less probability of multiple-node particle hit

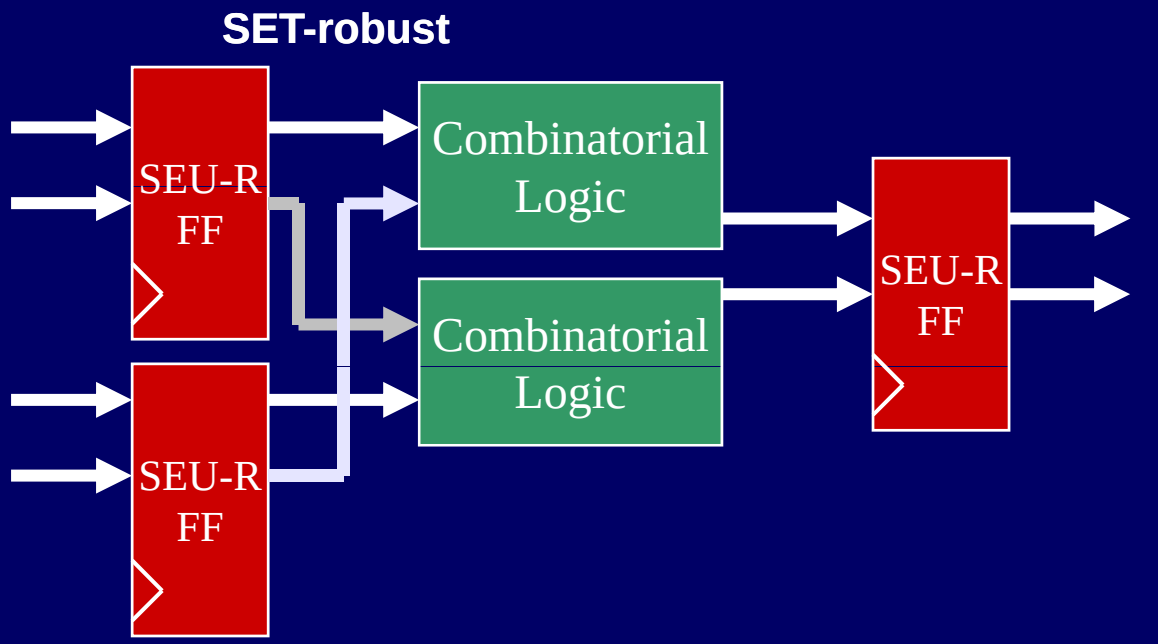


SET protection: duplicated logic



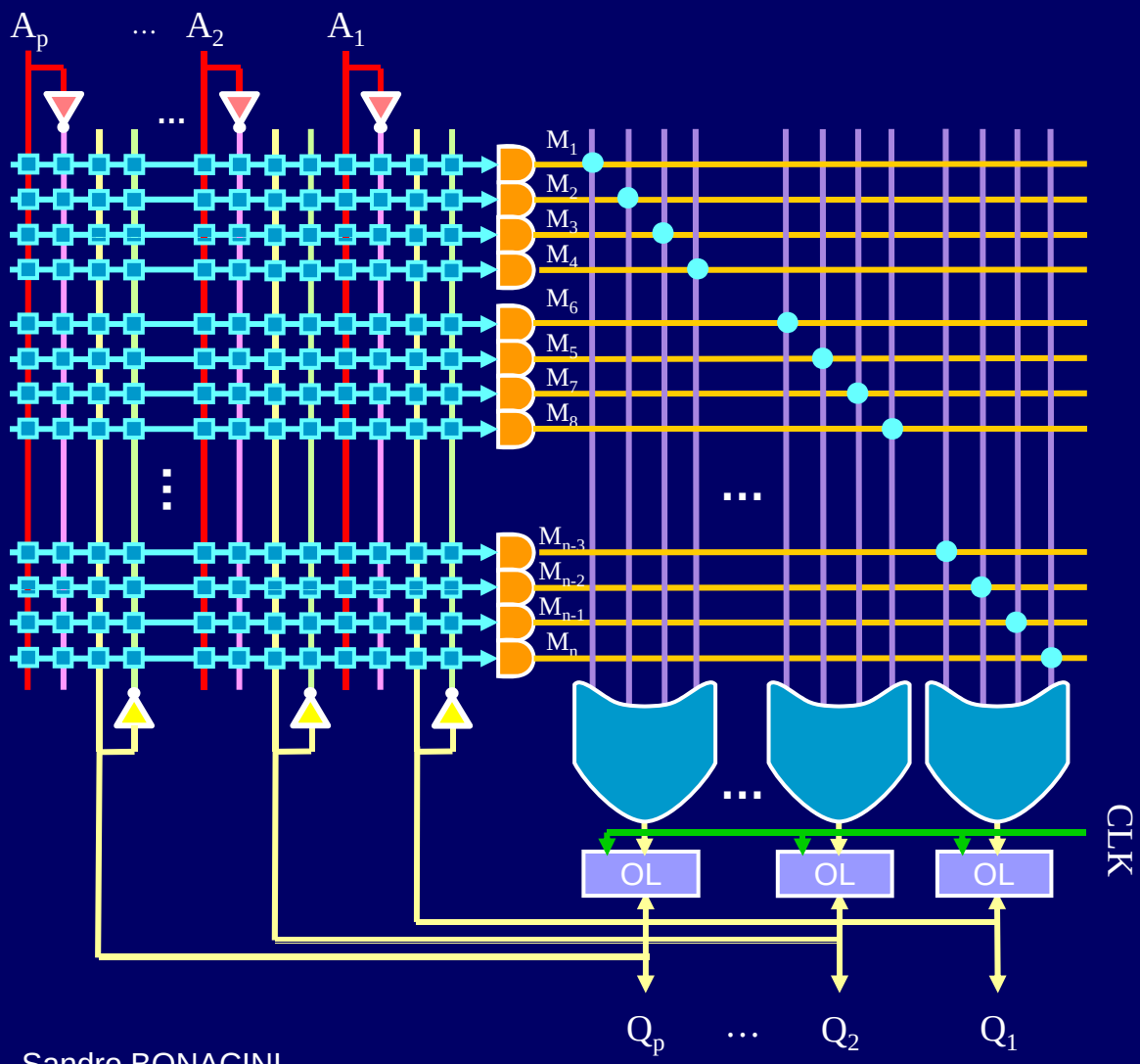
- Protection against Single-Event Transients (SETs)
  - Which occur in combinatorial logic and propagate to the flip-flops

- Duplicate combinatorial logic
- Use SEU-robust FF
  - SEU-robust FF has 2 inputs and 2 outputs
  - Can tolerate an SEU on one of the two inputs.
  - Duplicate data path alleviates the problem of latching erroneous states



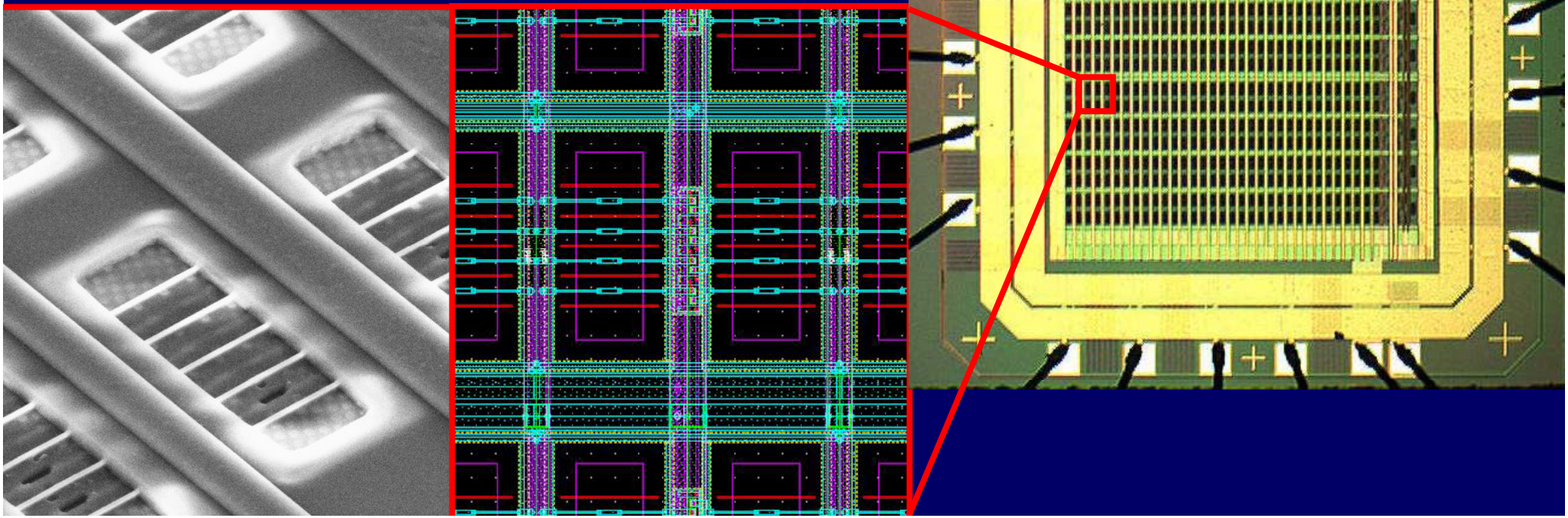
Radiation-tolerant PLD

- Compatible with 16LV8 commercial device
- Fuse based
  - Laser programmable
- 10 inputs, 8 programmable input/outputs
- Configurable AND matrix generates minterms
  - 32 vertical operand lines
  - 64 horizontal minterm lines
- Fixed OR matrix sums minterms
  - 8 minterms per output
- Outputs can be registered or not
- PLD can generate 8 functions of 8 minterms of 8 inputs
- Outputs are fed back to AND matrix for generation of more complex functions



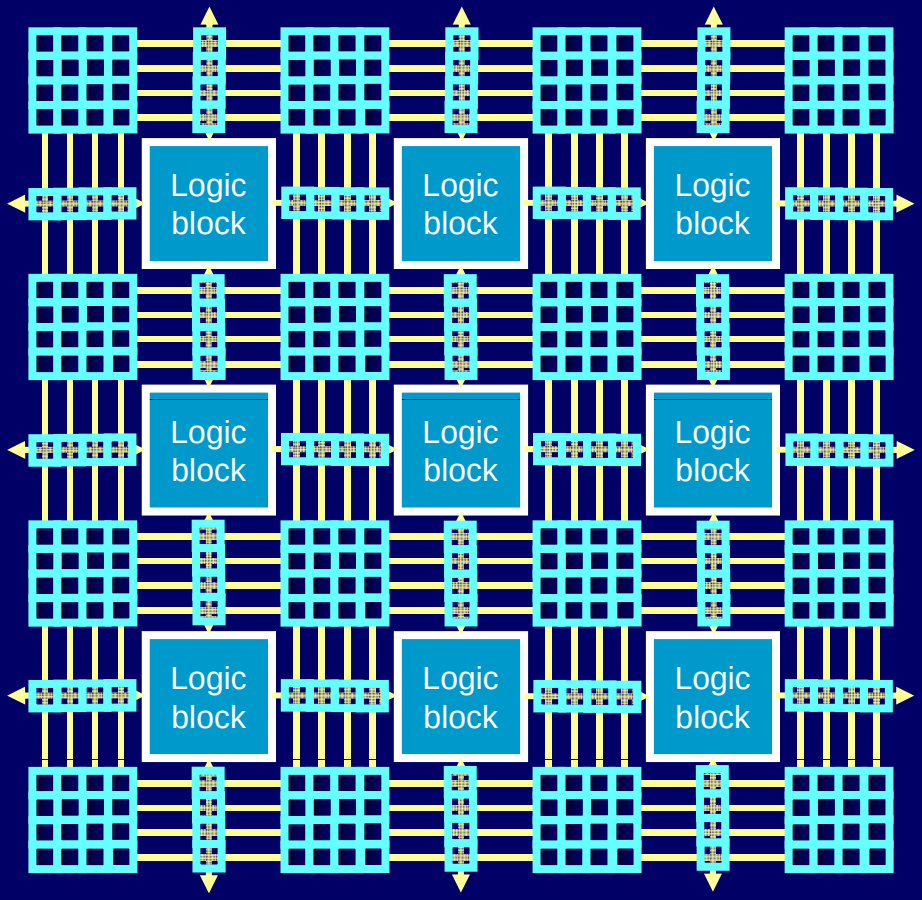
Fuses & PLD chip layout

- Fuses consist in a 7×1 μm^2 metal line (aluminum)
  - Laser programmable
  - 2080 programming fuses
  - Occupy 70% of core area
- Chip size is 2×2 mm^2

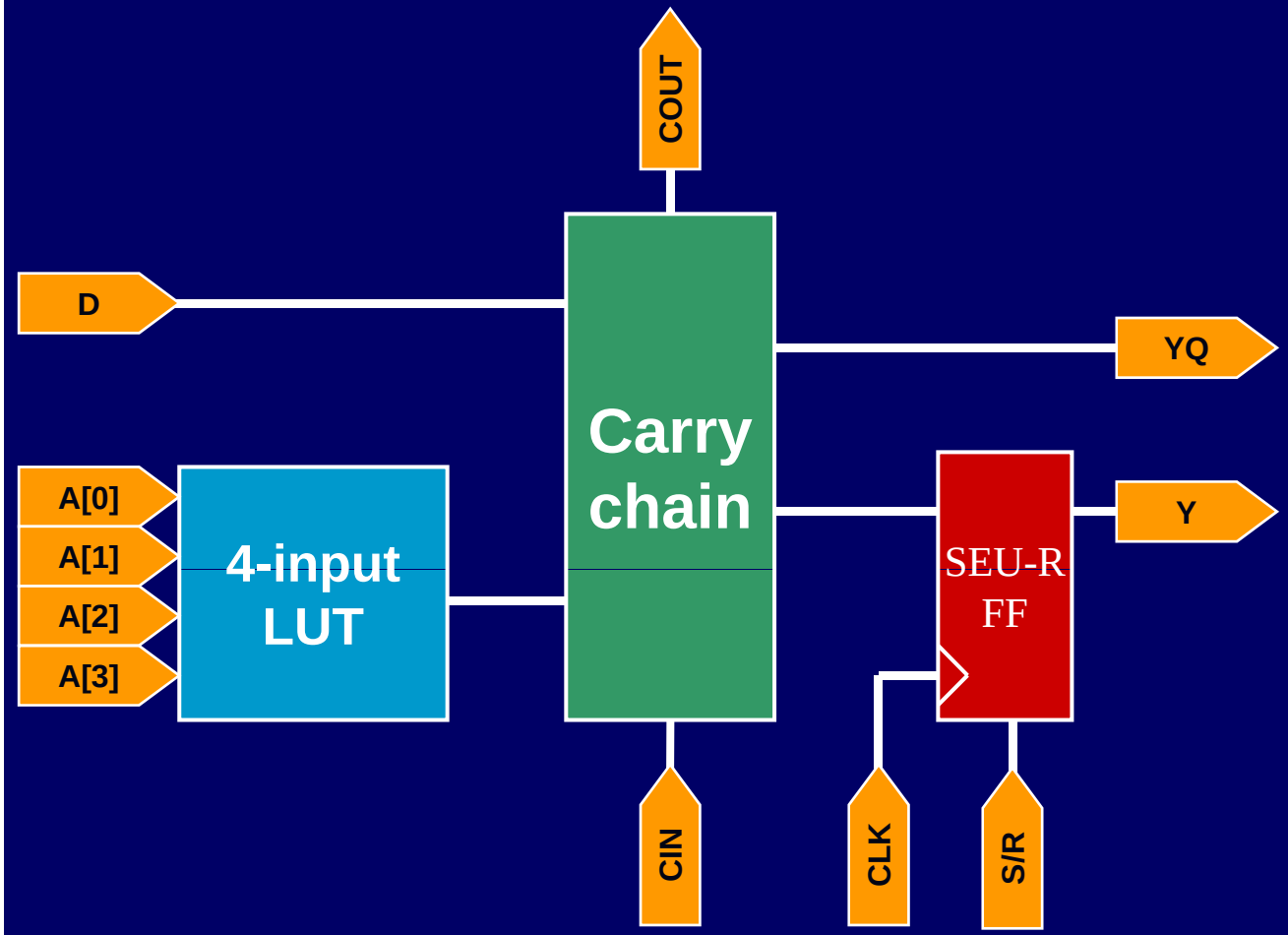


Radiation-tolerant FPGA

- Typical FPGA architecture
  - Array of 32×32 Logic Blocks (LBs)
  - Configurable routing
- SRAM based
  - Reprogrammable
- 256 I/Os
- Compatible with an existing commercial device
  - Same design tools can be reused
    - Synthesis, Place & Route



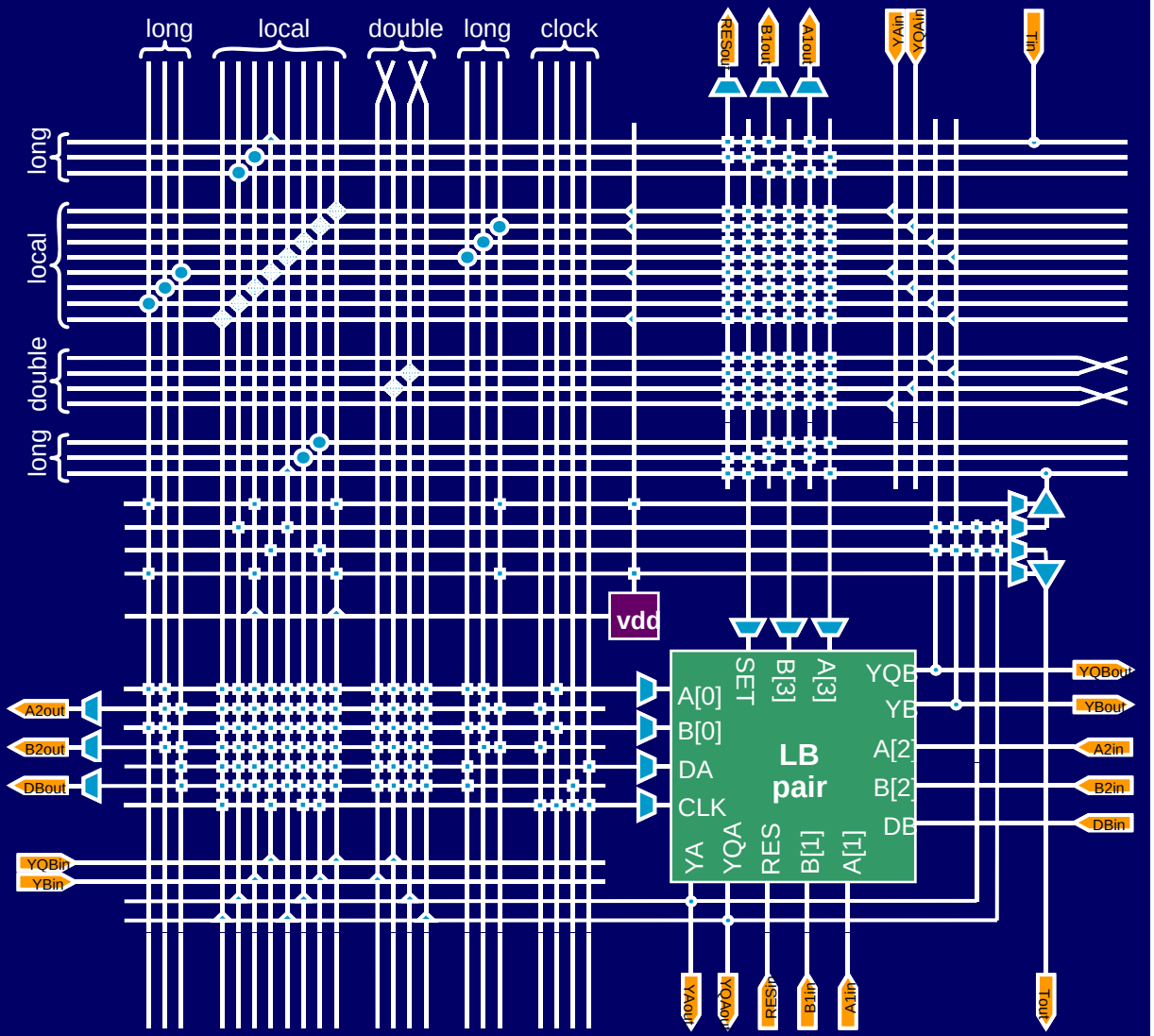
Logic Block



- 4-input-1-output Look-Up Table (LUT)
  - implements any boolean function of 4 variables
  - holds its truth table in 16 configuration registers
  - can also be used as a 16×1-bit RAM block
- 31 configuration bits per LB are present and are organized in a shift-register structure

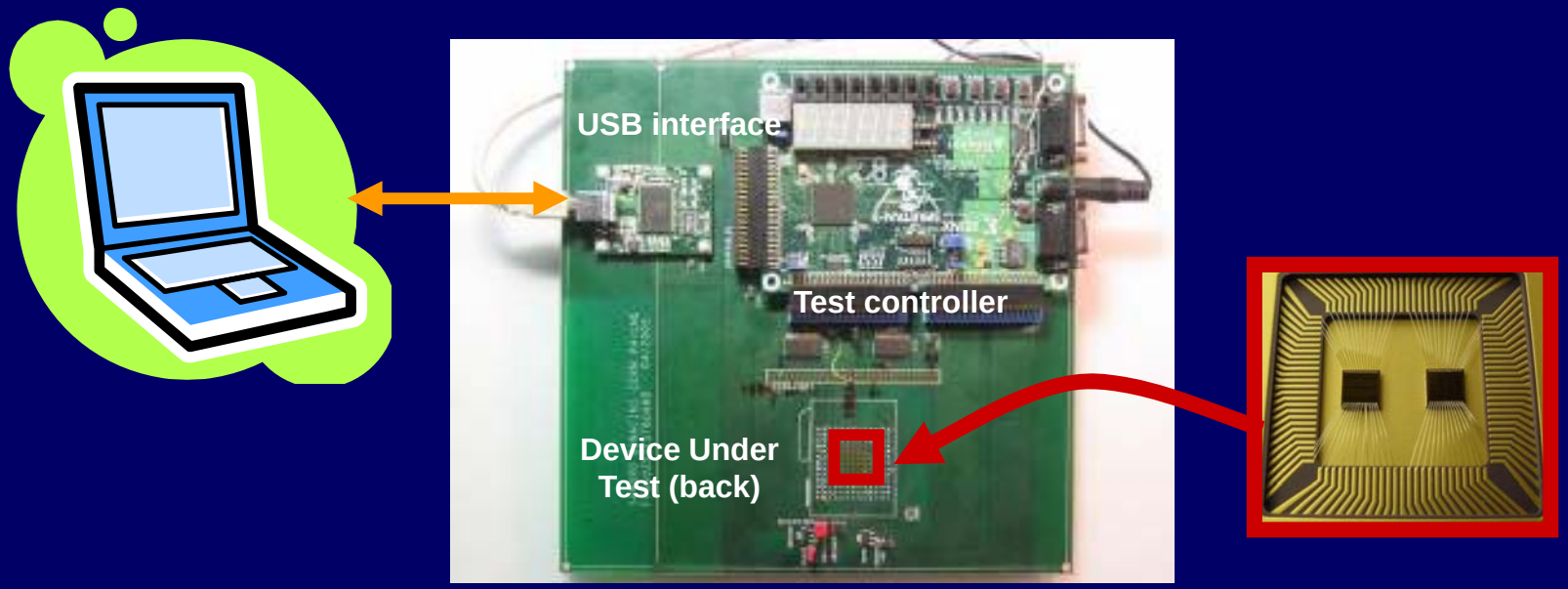
Programmable interconnections

- 18 wires per direction
  - 6 long lines
  - 12 short-distance lines
  - 8 direct neighbor connections
- Connections implemented with
  - tristate buffers
  - transmission gates
  - multiplexers
- 256 configuration registers in total

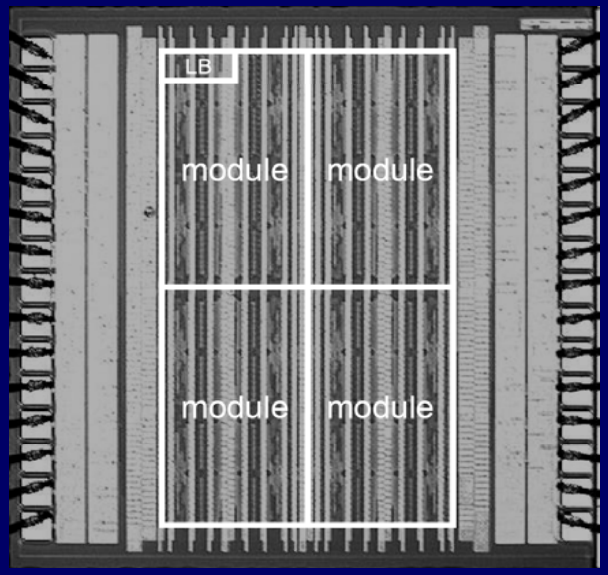


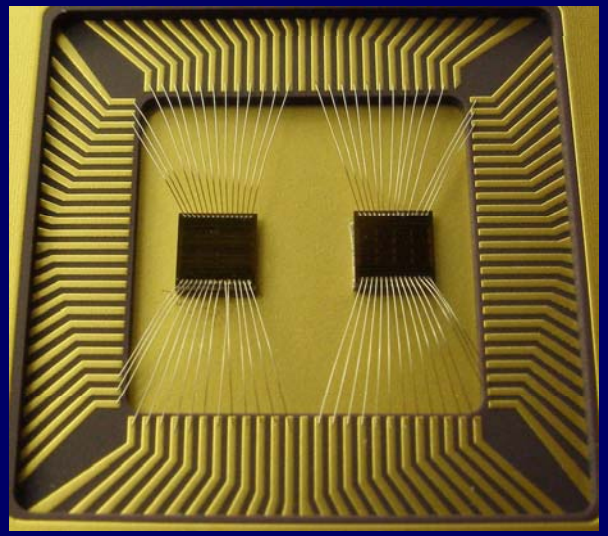
Heavy-ion beam tests on SEU-robust register

- Two test chips were fabricated
  - 0.25µm CMOS
    - 2×2 mm^2, 1024 SEU-robust registers
  - 0.13µm CMOS
    - 1×2 mm^2, 9216 SEU-robust registers, 4096 standard library registers
- Static shift-register test
  - Stream in configuration
  - Beam start/stop
  - Retrieve configuration & compare
- Dynamic shift-register test
  - Continuous configuration load, retrieve & compare while configuration clock is running and beam is on



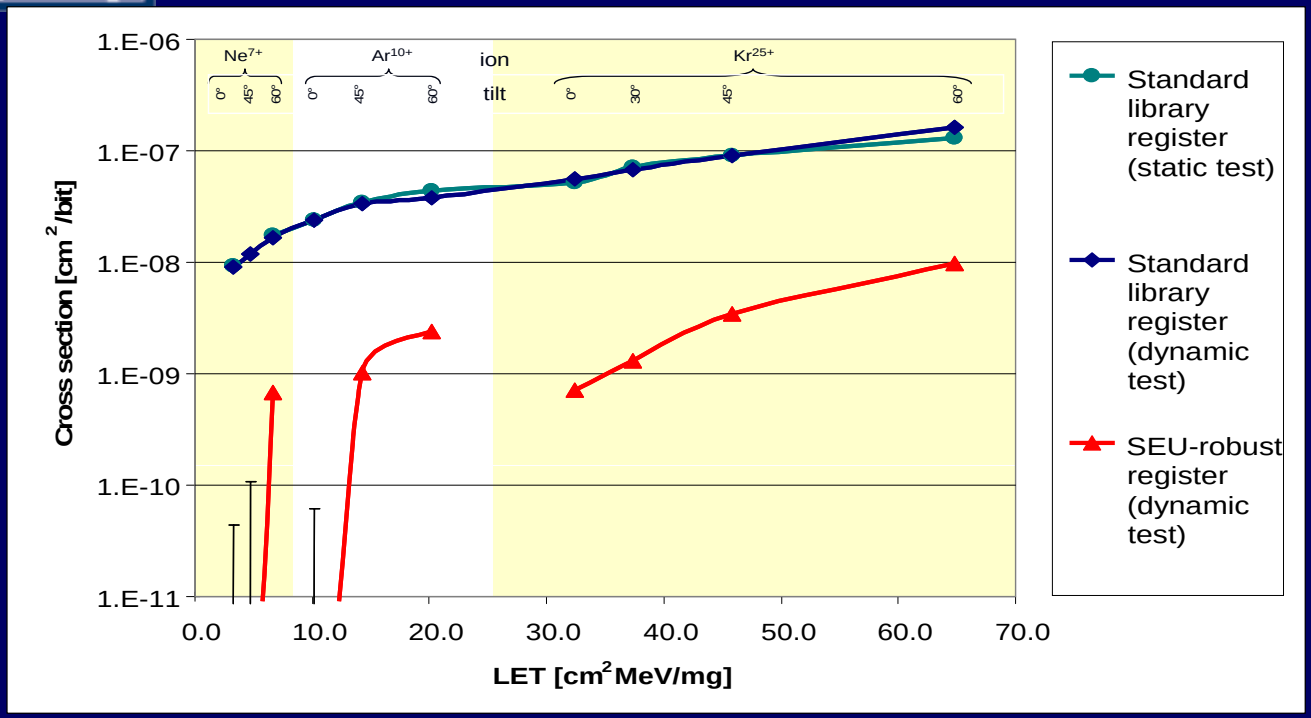
Test chip in 0.25µm CMOS

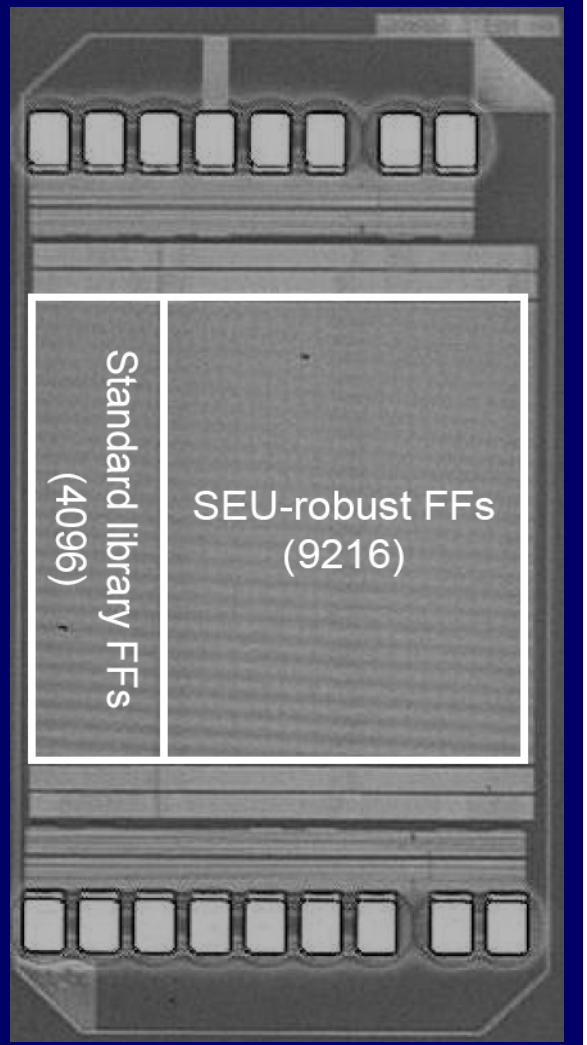




- Heavy-ion beam testing
  - Strong SEU robustness of the register cell up to an LET of 79.6 cm^2MeV/mg
    - no errors observed in either static and dynamic test modes
  - At an LET of 112 cm^2MeV/mg and only in the dynamic test mode, the register cell showed SEU sensitivity, with SEU cross-section of $6.2 \cdot 10^{-10}\ cm^2/bit$
  - LHC environment: up to 17 cm^2MeV/mg

Test chip in 0.13µm CMOS





- 0.13µm CMOS
  - Good static mode robustness
    - no errors up to 45.8 cm^2MeV/mg
  - In dynamic mode register shows sensitivity
    - strongly dependent on angle of incidence of the beam
  - Suitable as configuration register
  - Not suitable as user register

Conclusions

- Our approach demonstrated the feasibility of the SEU-tolerant radiation-hard PLD and FPGA
  - PLD chip was fabricated
  - The LB of the FPGA design was finalized, work is on going to complete the FPGA with interconnection infrastructure
- An SEU-robust register structure was designed and tested in two CMOS technologies
  - Results obtained in the 0.25 μm technology demonstrate good robustness of the circuit up to 79.6 cm^2MeV/mg
  - The 0.13 μm circuit showed good robustness in the static tests but appeared to be sensitive in the dynamic tests
    - Additional work is necessary for the FPGA user register