Development of SEU-robust, radiation-tolerant and industry-compatible programmable logic components

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Abstract

Most of the microelectronics components developed for the first generation of LHC experiments have been defined and designed with very precise experiment specific goals and are hardly adaptable to other applications. In an effort to cover the needs for generic programmable components, often needed in the real world, an industry-compatible Programmable Logic Device (PLD) and an industry-compatible Field-Programmable Gate Array (FPGA) are now under development. This effort is targeted to small volume applications or to the cases where small programmable functions are required to fix a system application. The PLD is a fuse-based, 10-input, 8-I/O general architecture device compatible with a popular commercial part, in 0.25 μm CMOS. The FPGA under development is instead a 32×32 logic block array, equivalent to $\approx$ 25k gates, in 0.13 μm CMOS. SEU-robust registers are employed for configuration registers as well as for user data flip-flops.

I. Introduction

The progress in microelectronic technologies applied to programmable logic circuits has allowed to decrease the costs and the development time of digital electronics in the industrial sector as well as in the space and avionics sector. The use of such devices is also appealing for High Energy Physics (HEP) detectors placed in the vicinity of high-luminosity particle accelerators such as the Large Hadron Collider (LHC). The harsh radiation environment present in these detectors makes Commercial Off-The-Shelf (COTS) components unsuitable for the application and requires the design of custom-designed circuits.

The most advanced programmable circuits are Field-Programmable Gate Arrays (FPGAs), which consist of a memory storage bank and a set of logic circuits whose behavior is configured by the content of the memory bank. FPGAs exploit different techniques for the storage of the configuration information. Most commonly SRAMs, FLASH memories and antifuses are used. While the first two let the user program the device many times, the latter is One-Time Programmable (OTP). The SRAM-based FPGAs are inherently flexible to meet multiple requirements and offer significant cost and schedule advantages. They can be reconfigured after the commissioning of the systems to correct errors or to improve performance. SRAM-based FPGAs can be implemented in standard CMOS processes while FLASH-based FPGAs require special FLASH processes.

Many studies [1] have been done on the radiation effects on commercial FPGAs, proving them to be often sensitive to both Total-Ionizing Dose (TID) and Single-Event Upsets (SEUs). SEUs in FPGAs can occur in the user logic and, in the case of SRAM-based devices, also in the configuration storage. When the latter is corrupted by a particle hit, the user logic can end up being modified, therefore the functionality can be affected and compromised. This latter effect is often referred to as Single-Event Functional Interrupt (SEFI) [2]. SEFIs can also occur when the configuration control state machine of the FPGA enters into an erroneous state.

The FPGAs are critically sensitive to SEUs due to the large amount of memory elements located in these structures. These devices must be strongly protected to avoid errors during run time. There are two main techniques to mitigate the SEU radiation effects; by high level logic description or by cell level architectural design. Special constructs in the high level logic description involve introduction of redundancy in the user logic. These techniques reduce drastically the available circuitry resources of the FPGA and require complex reconfiguration schemes to avoid corruption of the configuration data [3]. Contrary to this approach, the objective of this work is the development of programmable circuits where SEU insensitivity is built-in at the storage cell level, not requiring the user to exploit any special technique for SEU protection.

Programmable Logic Devices (PLDs) are small components which can implement logic functions equivalent to ≈ 50 gates. Although PLDs are considered nowadays surpassed by FPGAs, they are still favourable in some applications implementing simple state machines, glue logic circuitry and providing fixes for system design bugs at the late stages of a project. PLDs also suffer from TID. PLDs are in general OTP devices and they are not affected from SEUs in the configuration storage, but the user data can still be corrupted and therefore need to be protected.

This work focuses on the design of an SRAM-based FPGA and a fuse-based PLD that are SEU-robust, radiation-tolerant, industry-compatible devices.

II. Radiation hardening techniques

This section describes the measures taken during the design for the programmable logic circuits to resist radiation. These are divided into TID tolerance and SEU robustness techniques.

A. TID tolerance

Special layout techniques for CMOS technologies were proven to be effective against TID up to the HEP experiments

requirements [4] and a standard cell library in 0.25 μm CMOS was designed and qualified [5]. The same layout techniques were employed during the design of the 0.25 μm test chip.

The 0.13 μm CMOS technology used does not require special transistor layouts in order to be TID-tolerant, as suggested by the results in [6]. The only minor layout constraint imposed by TID is to avoid the use of minimum width devices. In this work, all the devices have width bigger than 0.3 μm which is almost double of the minimum size.

B. SEU hardening techniques

The key point in the realization of SEU tolerant programmable circuits is the development of an SEU-robust register which can be used to store the user data as well as the configuration data in the case of an FPGA. In this work, protection of the stored information is achieved by using special circuit techniques in the implementation of the register cell rather than system techniques like Error Correction Coding (ECC), Triple Module Redundancy (TMR) or data scrubbing.

The SEU-robust register is made of two identical cascaded latches, the first being the master, and the second being the slave. The two latches are a modified version of the Dual Interlocked Cell (DICE), introduced in [7]. It is evident that since the DICE latch has a single local clock buffer, this marks a weak spot for SEU tolerance: if the clock buffer is upset, the operation of the entire cell is compromised. This upset mechanism is expected to become more pronounced in advanced technologies with smaller feature sizes. In order to alleviate this upset mechanism, our SEU-robust latch features two independent terminals for the input, output and clock signals, driven by separate signal buffers. The SEU-robust latch is presented in Fig. 1.

Under normal operating conditions, the two redundant copies of the inputs are identical. When a particle hits one of the two input buffers, the transient upset will affect only one of the four memory nodes in the latch, which is intrinsically immune to this mode of upset.

It follows that the combinatorial part of the logic can be protected from Single-Event Transients (SET) [8] by duplicating it. In this work, duplication is extensively used to harden the entire logic circuitry.

Because of its circuit topology the latch is intrinsically insensitive to single-node particle hits on its network. Nevertheless, the latch is vulnerable if a particle hits multiple correlated nodes, an event also referred to as multiple-node charge collection. To reduce the probability of this mode of failure we employed a special layout topology which takes care of increasing the distance of the sensitive correlated nodes.

The solution adopted in our work consists in interleaving the nodes of the two latches composing the register, since they are independent. Fig. 2 depicts the layout of the SEU-robust register.

C. Test procedures and results

To assess the performance of the SEU-robust register and compute its effectiveness with respect to the feature size of CMOS technologies we designed and fabricated two test chips on respectively CMOS 0.25 μm and 0.13 μm technologies.

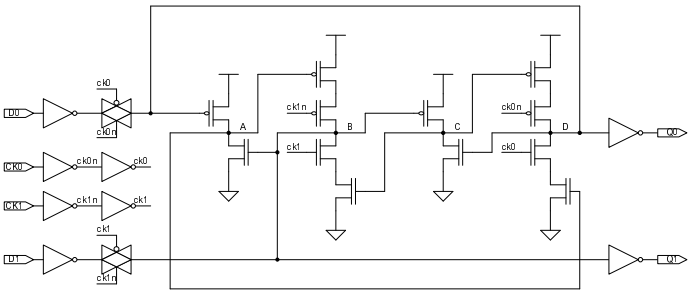

Figure 1: Fully 2×-redundant SEU-robust latch implemented in this work. The latch has 2 inputs, 2 outputs and 2 local clock buffers. A register is made of two cascaded latches (a master and a slave).

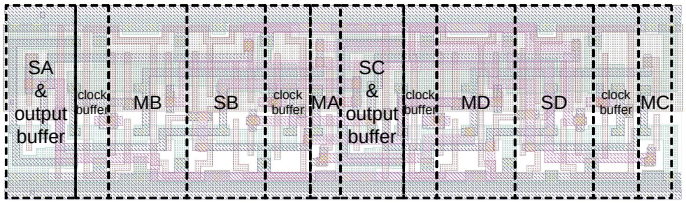

Figure 2: Layout view of the SEU-robust register in its 0.13 μm technology version. The figure is divided into the areas which affect the corresponding nodes in the network. The master latch nodes are MA, MB, MC, MD, while the slave latch nodes are SA, SB, SC, SD. By interleaving the master and the slave components the distance among nodes belonging to the same latch is maximized.

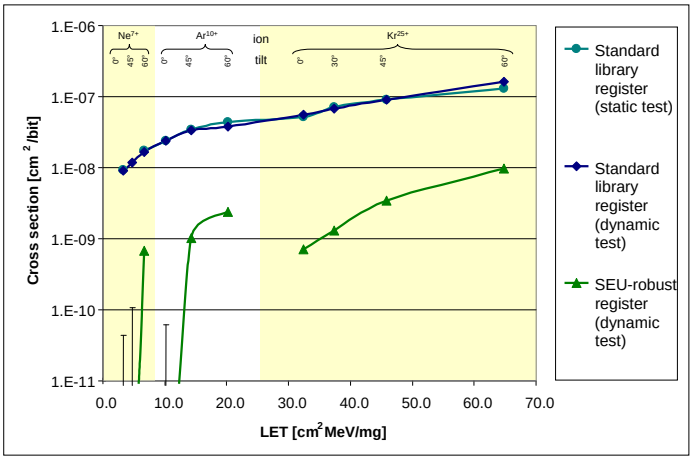

Figure 3: Results of the heavy-ion beam test on the 0.13 μm technology SEU-robust register. Only the dynamic test showed sensitivity, while no errors were observed for the static test. Error bars representing the upper bound cross section given with 95% confidence level are present where no errors were observed in the dynamic test.

Table 1: Comparison between the two tested versions of the SEU-robust register. Units are in μm and fF.

Technology feature size	0.25	0.13
Cell size	68×11	14.5×3.6
Min. distance between memory nodes	10.0	2.4
Number of metal levels used	2	3
Enclosed layout transistors	yes	no
Minimum device width	3.23	0.30
Typical inverter input capacitance	25	1

The SEU-robust registers were implemented in the form of shift-registers to facilitate SEU characterization. The two test chips had the same circuitry and differ only in sizes and ratios due to the different layout rules.

Table 1 summarizes the differences between the two chips. The chips were tested under a heavy-ion beam. Two kinds of tests were performed: a static test and a dynamic test.

The static test consists in (a) loading a bit stream in the Device Under Test (DUT) while the beam is off, (b) exposing the DUT to the beam for a specific fluence and (c) comparing the output bit stream of the DUT with the original.

The dynamic test consists instead in continuously writing a bit stream in the DUT while it is exposed to the beam and continuously comparing the output with the original.

The registers fabricated in the 0.25 μm technology showed a strong robustness [9], proving to be insensitive up to an LET of 79.6 cm^{2}MeV/mg. No upsets were observed in all static tests, while the dynamic tests showed a small sensitivity at an LET of 112 cm^{2}MeV/mg.

The 0.13 μm cells showed to be less robust than their 0.25 μm counterpart. The cell demonstrated strong robustness in the static tests, for no errors were observed up to 45.8 cm^{2}MeV/mg, while showed sensitivity in the dynamic tests. The test results are depicted in Fig. 3. A standard library shift-register present on the same test chip was irradiated for comparison. The plots were obtained with three different ions and several tilt angles: Ne^{7+} was used for LETs below 10 cm^{2}MeV/mg at 0°, 45° and 60° tilt; Ar^{10+} was used for LETs between 10 and 20 cm^{2}MeV/mg, at 0°, 45° and 60° tilt; Kr^{25+} was used above 20 cm^{2}MeV/mg at 0°, 30°, 45° and 60° tilt. The cross section in the dynamic tests is strongly dependent on the angle of incidence of the beam, which suggests the increased importance of multiple node charge collection phenomenon.

Hence, from the test results it is evident that the 0.25 μm register is suitable as a user register for the PLD circuit, while the 0.13 μm register is suitable as configuration register for the FPGA circuit but not as user register. A harder cell has to be designed for this latter purpose.

SET tolerance can be attained feeding the SEU-robust registers with two redundant copies of the same logic value, which can be obtained for instance from two identical combinatorial logic blocks. This technique is referred as duplication. A possible alternative is temporal redundancy, which consists in creating a copy of the logic value with a delay element.

III. PLD DESIGN STRUCTURE

PLDs consist of two sets of logic cells organized in two stages, namely an AND stage and an OR stage. The AND stage performs its operation on the inputs of the PLD creating minterm products that are then summed by the second stage. In a PLD the AND stage is configurable thus the user can decide which inputs of the PLD participate to each AND, customizing in this way the minterms. The OR stage is hard-wired and not configurable. Fig. 4 shows a typical PLD architecture.

A configurable Output Logic (OL) block containing a register is present at the output of each OR stage. The output of each OL is fed back to the AND array and can be used to form more complex logic.

The PLD of this work has 8 outputs, 8 minterms per output and 8 inputs, therefore the AND array has 2048 programming bits and the PLD can realize 8 logic functions of 8 minterms formed by the 8 inputs and the 8 outputs.

Each OL output is connected to a bidirectional pad. In fact, in this PLD implementation, each pad connected to the OL blocks can be configured to be input, output or bidirectional, according to the user needs. Overall, the PLD chip has 10 input pads and 8 bidirectional pads. Two of the inputs are special, since they can be assigned to be the clock and the output enable depending on the configuration, and they are fed to all the OLs for this purpouse. The PLD is fully compatible with a commercially available component.

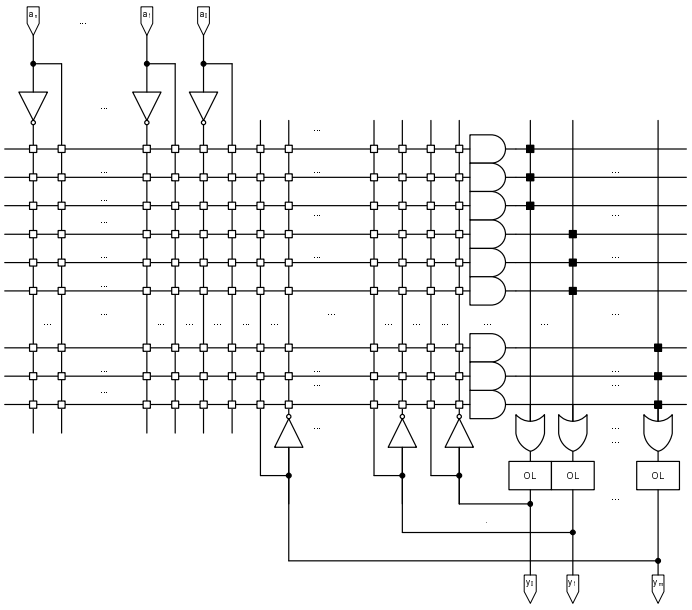

Figure 4: Typical PLD architecture composed of a configurable AND stage, a fixed OR stage and a set of registers. The empty squares indicate the programmable participation to the AND stage, while the filled squares indicate the fixed participation to the OR stage.

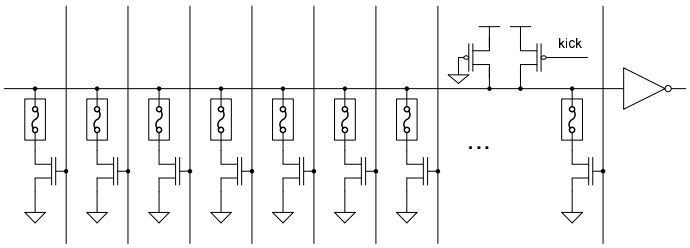

Figure 5: Horizontal line with fused pull-downs and primary and secondary pull-up forming an AND.

A. AND array

The AND array consists in 64 horizontal lines which form the output minterms and 32 vertical lines which bring the inputs from the 8 input pads and from the 8 OL feedbacks in their positive and negated form.

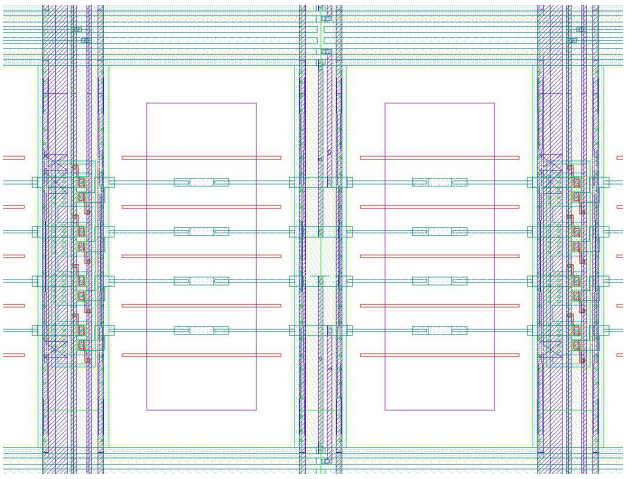

Figure 6: Layout of the fuses in the AND matrix. Each fuse is attached on one side to a short segment which connects it to an horizontal line running on the top or on the bottom. A transistor is placed on the other side of each fuse, acting as a pull-down. The gates are connected in vertical lines.

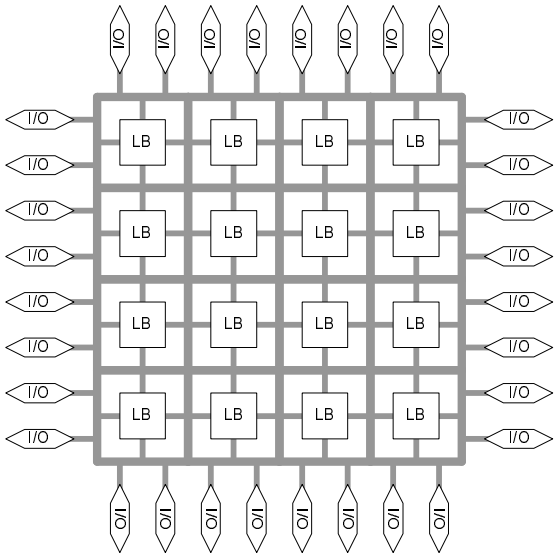

Figure 7: Typical FPGA architecture composed of programmable Logic Blocks (LBs), Input/Output (I/O) elements and a configurable routing mesh.

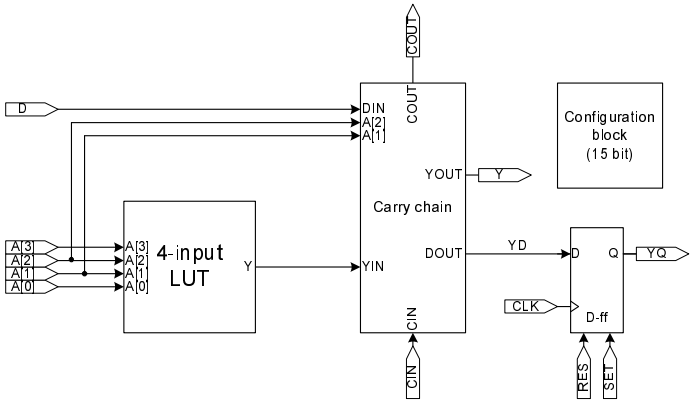

Figure 8: Simplified schematic of the Logic Block. A 4-input-1-output LUT generates a user-configured function. A carry chain is provided for an efficient implementation of adders. An user register the output of the combinatorial part of the LB.

A fuse and a transistor are placed at each intersection, and act as the pull-down for the horizontal line connected (see Fig. 5). Hence, each horizontal line behaves as a wired NOR. Two pull-up transistors are connected in the middle of each horizontal line.

The delay of the wired AND is directly related to the strength of the pull-up and pull-down drivers. For this reason, each horizontal line has two pull-up transistors, a weak primary pull-up and a strong secondary pull-up. The former acts as a keeper with low power consumption, while the latter is activated only when the inputs of the logic change in order to quickly bring the horizontal line to its settling value.

The horizontal lines have a high capacitance which should be enough to resist SETs coming from particles with an LET below ≈ 25 cm^{2}MeV/mg, which is more than sufficient in the foreseen application. Each horizontal line feeds two inverters which generate two redundant copies of the same wired AND value for the LB.

The fuses available in the technology are laser-programmable. Each fuse is composed by a 7×1 μm^2 metal rectangle enclosed in an opening in the passivation. Due to layout rules, the area utilization of a group of 4 fuses is about 32×56 μm^2.

B. Logic blocks

Each LB accepts 8 minterms coming from the AND matrix and is connected to an I/O pad plus a second alternate input pad. The behavior of each LB depends on 4 configuration bits which decide whether the LB uses the primary pad or the alternate pad and whether it uses it as input, output or I/O. The LBs are fully duplicated for protection from SETs.

C. Chip layout

The chip size is 2×2 mm^2, while the core size is approximately 950×1150 μm^2.

IV. FPGA DESIGN STRUCTURE

The basic element for logic implementation inside an FPGA is a programmable LB that allows the user to implement various logic functions. An LB is usually composed of a configurable combinatorial block which drives a user register. In an FPGA many LBs are interconnected through a two-dimensional mesh of wires with switching elements at wire crossings to configure the routing, like in Fig. 7.

Our target design is an FPGA composed of an array of 32×32 LBs for an equivalent of $\approx$ 25k gates. The FPGA is fully compatible with an existing commercial component. The FPGA has 256 configurable I/Os which can be configured as registered or non-registered.

A. Logic Block

The LB in the present work resembles a typical FPGA logic block. It is composed of a 4-input-1-output Look-Up Table (LUT) together with a carry-chain infrastructure and a user reg-

ister. The diagram of the LB is depicted in Fig. 8.

The LUT can implement any boolean function of 4 variables and holds its truth table in 16 configuration registers. An internal multiplexer driven by the LUT inputs selects the output bit among the 16 stored values, generating the function. The LUT can also be used as a 16×1-bit RAM block.

A special purpose carry-chain logic block eases the implementation of adders, minimizing the number of necessary LBs. Without this structure, the number of LBs used for a n-bit adder would be $2n$, since there are 2 outputs per bit, while with this architecture only n LBs are employed.

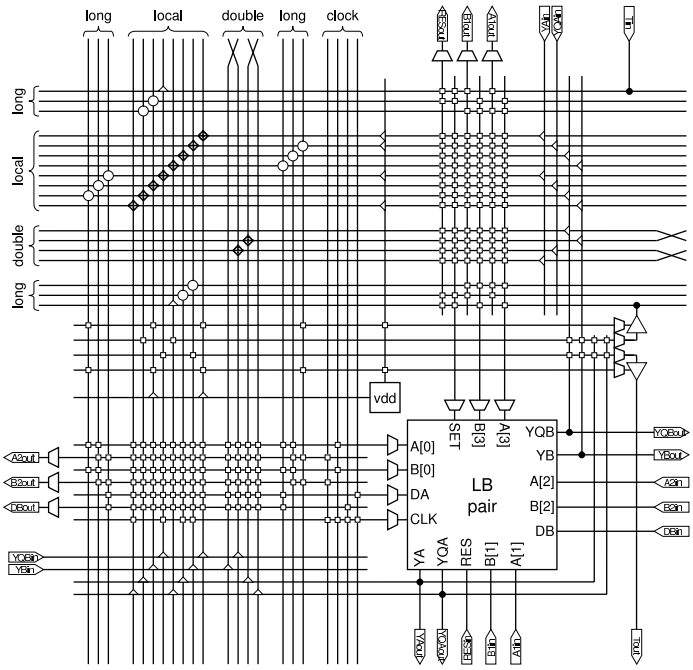

Figure 9: Periodical structure for the interconnectivity. The block is replicated in 2 dimensions in order to create a large array. Carry-chain connections between LBs are not shown.

The user register receives the output of the combinatorial part of the LB. An unregistered output is also provided. The user register has asynchronous set and reset signals.

A total of 31 configuration bits per LB are present and are organized in a shift-register structure for configuration loading.

B. Switch matrix architecture

The FPGA interconnectivity is a balanced combination of local connections, which bring signals between neighbouring or close cells, and long connections, which bring signals between distant places on the chip. A pair of LBs together with its adjacent routing forms a tile, which is the basic structure repeated in two dimensions to form an array.

In order to let the user implement a non-congested routing the number of horizontal and vertical wires is about the same of the total LB pair I/Os which have to be connected. In this design the number of wires is 18 per direction, respectively 6 long lines and 12 short-distance lines. In addition, adjacent tiles share a number of direct connections. Fig. 9 depicts the wiring architecture designed. The inputs of each LB pair are physically divided among the four sides of the block in order to distribute their load. Four dedicated clock tree lines are available as a global network coming from a dedicated pad.

The several wires present in a tile are connected one to the other with tristate buffers, transmission gates or multiplexers, depending on the length of the lines and their purpose.

V. Conclusions

The results obtained in the beam tests were promising and demonstrate the feasibility of the design of SEU-tolerant radiation-hardened programmable logic circuits. The PLD was fabricated and it is soon going to be tested.

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