Contribution ID: **15** Type: **Oral**

Development of SEU-robust, radiation-tolerant and industry-compatible programmable logic components

Wednesday, 5 September 2007 16:20 (25 minutes)

Most of the microelectronics components developed for the first generation in LHC experiments have been defined and designed with very precise experiment specific goals and are hardly adaptable to other applications. In an effort to cover the needs for generic programmable components often needed in the real world, an industry-compatible Programmable Logic Device (PLD) and an industry-compatible Field-Programmable Gate Array (FPGA) are now under development. This effort is targeted to small volume applications or to the cases where small programmable functions are required to fix a system application. The PLD is a fuse-based, 10-input, 8-I/O general architecture device compatible with a popular commercial part. The FPGA under development is instead a 32×32 logic block array, equivalent to ˜25k gates, in 0.13 micron CMOS. SEU-robust registers are employed for configuration registers as well as for user data flip-flops. Test results for both chips will be presented.

Summary

The harsh radiation environment present in the vicinity of high-intensity-beam particle accelerators, necessary for High Energy Physics (HEP) experiments like the LHC, requires so far the utilization of custom-designed Application-Specific Integrated Circuits (ASICs), and forbids instead the exploitation of standard commercial programmable logic components. Future experiment and upgrades would benefit from the flexibility of programmable logic covering the need for small volume applications or where simple logic functions are necessary. Within this perspective, two industry-compatible radiation-tolerant devices are under development, respectively a Programmable Logic Device (PLD) and a Field-Programmable Gate Array (FPGA), targeting two different types of applications. Studies performed on the radiation effects on most commercial programmable logic parts have proved them to be often sensitive to both Total-Ionizing Dose (TID) and Single-Event Upsets (SEUs). SEUs can occur in the user logic and, in case of SRAM-based devices, also in the configuration registers. When such a register is corrupted, the user logic can end up being modified, therefore the functionality can be affected and compromised.

This work focuses on the development of programmable logic designed to be SEU-robust and TID-tolerant. Our final aim is the creation of an FPGA and a PLD where SEU insensitivity is built-in, thus not requiring the user to exploit special technique for SEU protection.

SEU-hardening circuit and layout techniques were employed for the design of a robust register based on the Dual-Interlocked Cell (DICE). The sensitivity of the SEU-robust register topology was assessed on a test chip fabricated in a 0.25 micron technology. The circuit proved to be insensitive up to an LET of 79.6 cm2MeV/mg showing minimal sensitivity at higher LETs. The structure of the register will be described in this paper.

The SEU register was exploited also for the development of a fuse-based PLD. The configuration fuses are intrinsically hard to SEUs while the user logic is protected by the SEU-hardened structure. The PLD is a 10-input 8-I/O general architecture device compatible with most commercial parts. The PLD structure will be described.

The target FPGA device is an SRAM-based 32×32 logic block matrix which uses

the SEU-robust register for both configuration and user data in order to attain maximum reprogrammability together with SEU hardness. The FPGA could be used as a stand-alone chip or as an IP-core. The FPGA fabric under development will be described.
Both devices can easily be programmed using the same development tools available for the corresponding commercial parts and adapted to our specific implementation by a simple post-processing tool. Device programming considerations will be discussed.

Primary author: Mr BONACINI, Sandro (INPG, CERN)

Co-authors: Dr MARCHIORO, Alessandro (CERN); Dr FACCIO, Federico (CERN); Dr KLOUKINAS, Kostas (CERN)

Presenters: Dr KLOUKINAS, Kostas (CERN); Mr BONACINI, Sandro (INPG, CERN)

Session Classification: Parallel session B6 - ASICs 3 future