

ALICE Silicon Pixel Detector (SPD) system

Alexander Kluge

CERN-PH

TWEPP 2007

CERN, Sept 3 - 7, 2007

Overview

- **ALICE SPD**

- Detector and Specification



- **Components**

- On detector
- Off detector



- **Pixel trigger**

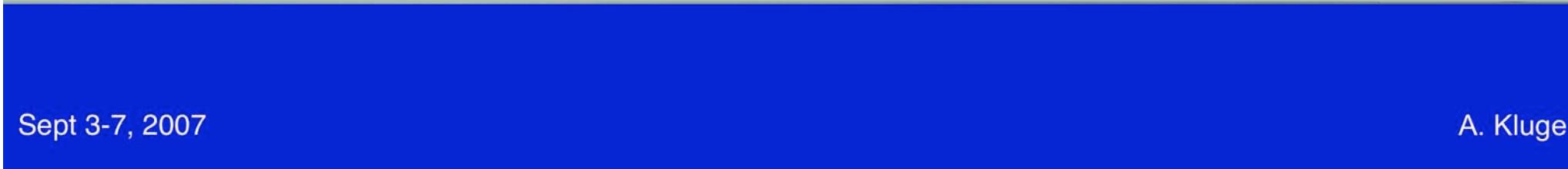
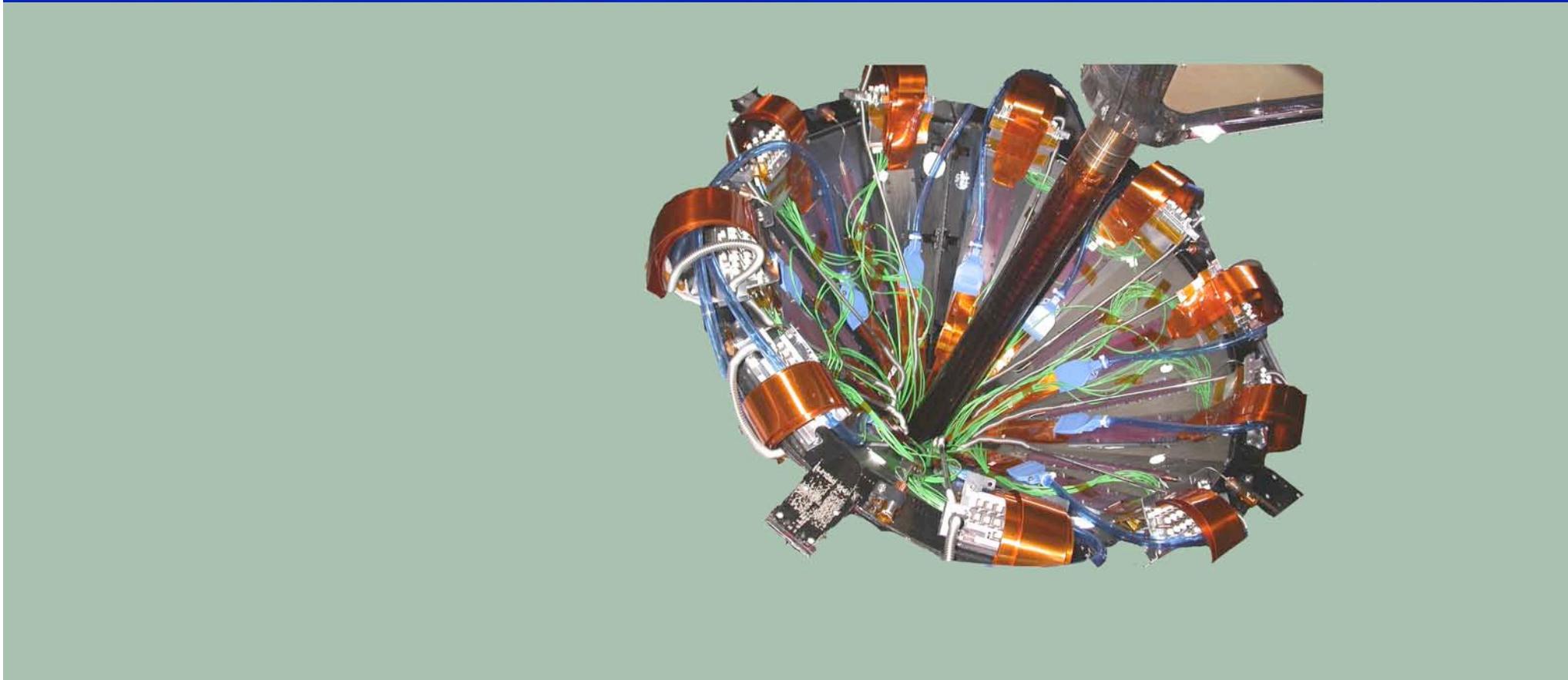
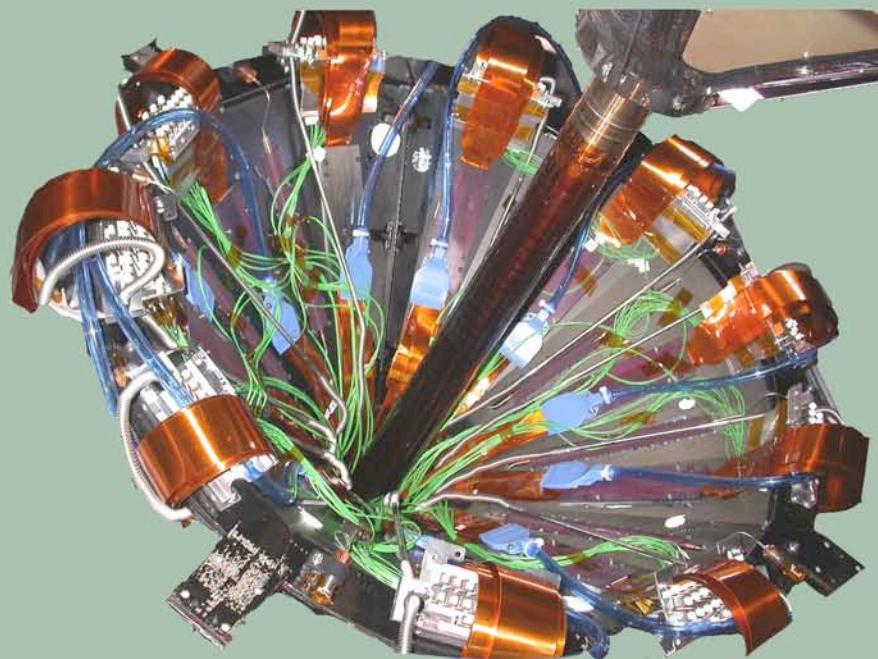


- **Status of**

- Installation
- Commissioning



- **Conclusion**



Sept 3-7, 2007

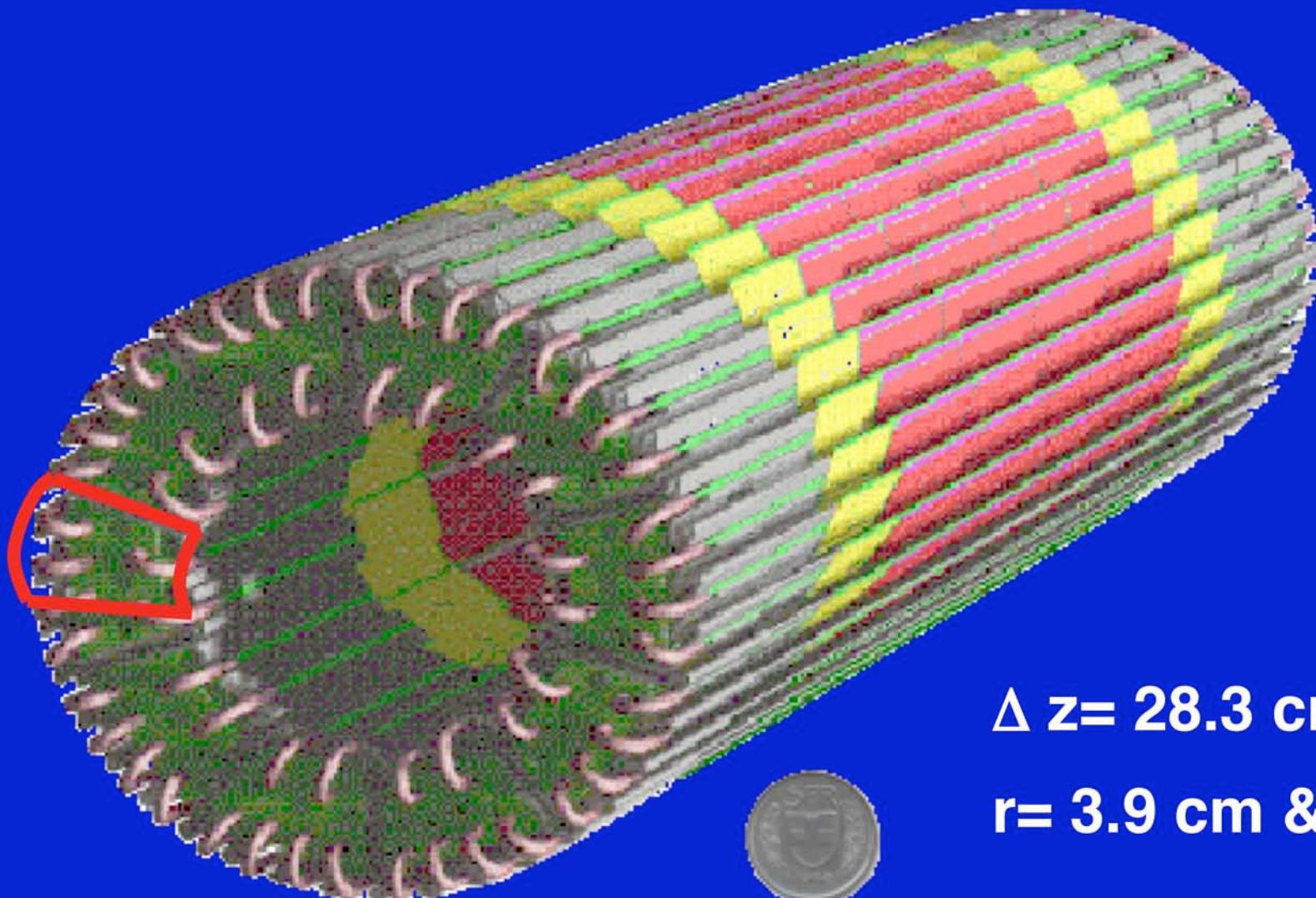
A. Kluge



Sept 3-7, 2007

A. Kluge

The SPD Detector



The SPD half stave

physical size = 250 mm x 15 mm x 2 mm

material budget = 1% $X_0 \rightarrow$ no copper

120 pieces

1 sensor

beam pipe dist. 4 mm

1 sensor

10 readout chips



Sept 3-7, 2007

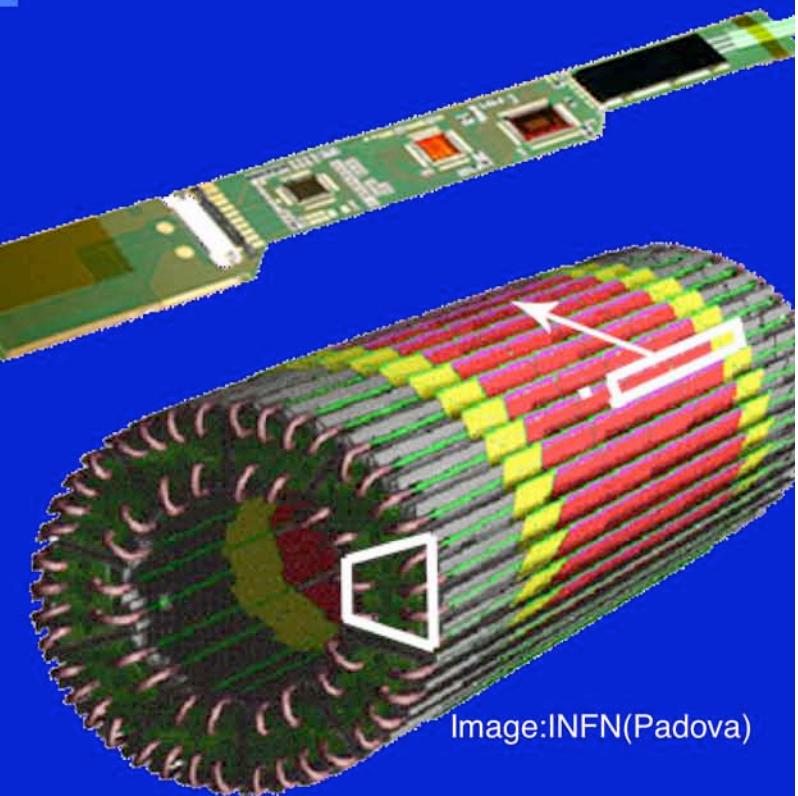


Image:INFN(Padova)

A. Kluge

System parameters

System Parameters

- ~ 10 million channels in 1200 pixel chips
- 120 detector modules - half staves
- 10 sectors
- Two trigger levels (6 μ s,100 μ s): ~1 GB/s raw data
- Readout time: 260 μ s
- Radiation: 250 krad
- neutron flux: $3 \times 10^{11} \text{cm}^{-2}$ (10y)
- Material budget: 1% X_0 per layer
- Power dissipation: 1kW (cooling C_4F_{10})
- Operation temperature: 24 °C

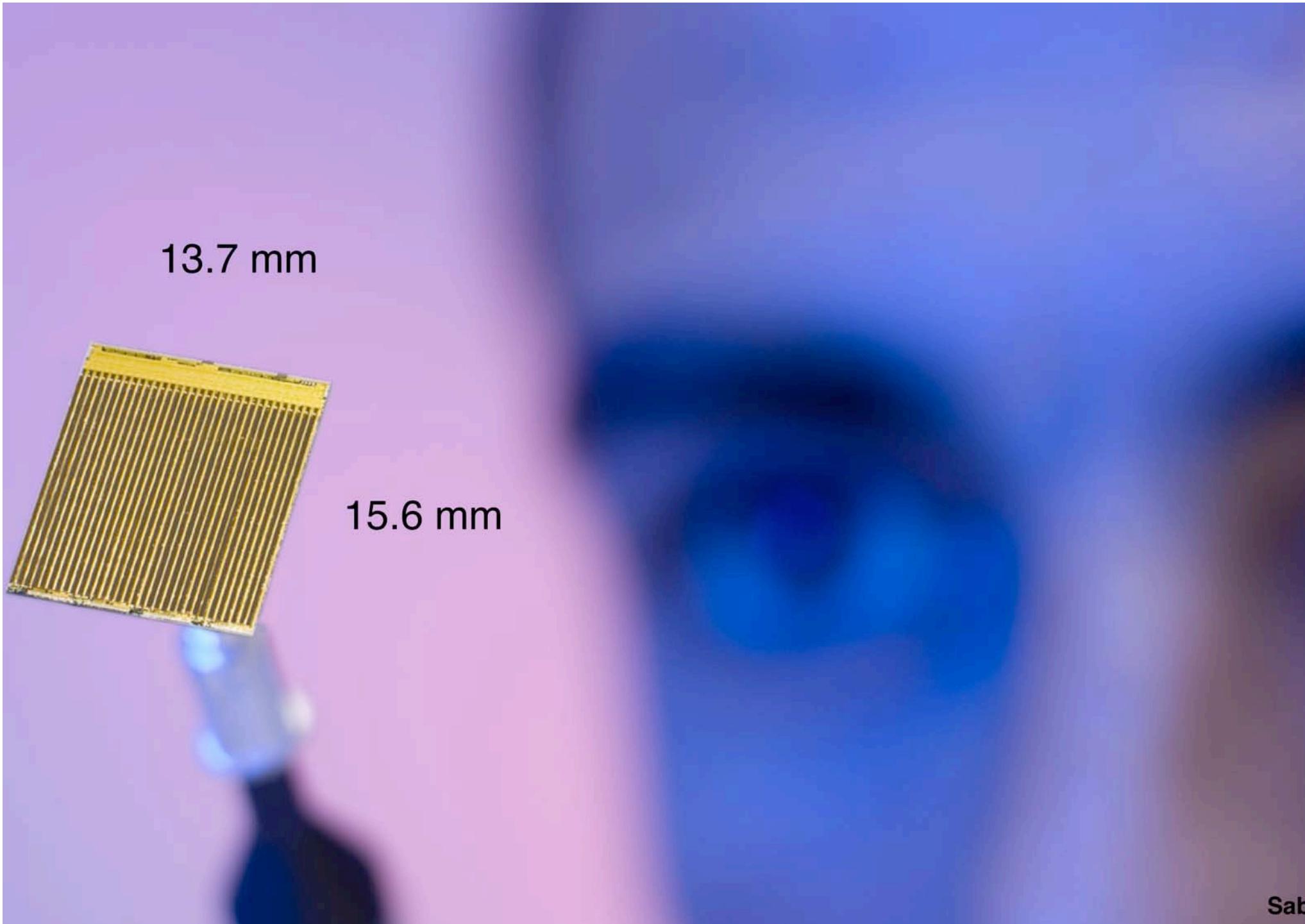
On-detector components

On detector electronics elements

- Pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)

On detector electronics elements

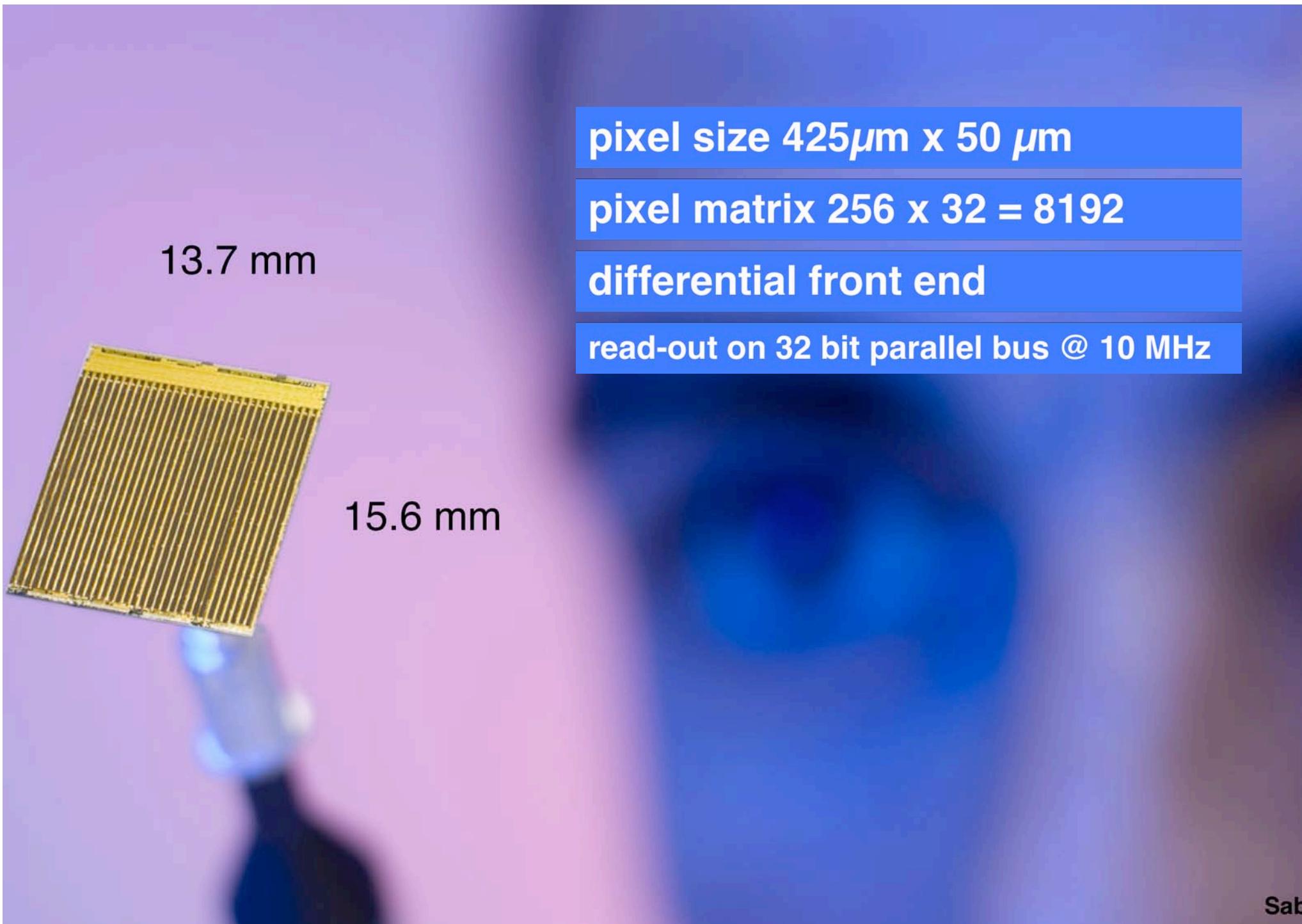
- Pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)



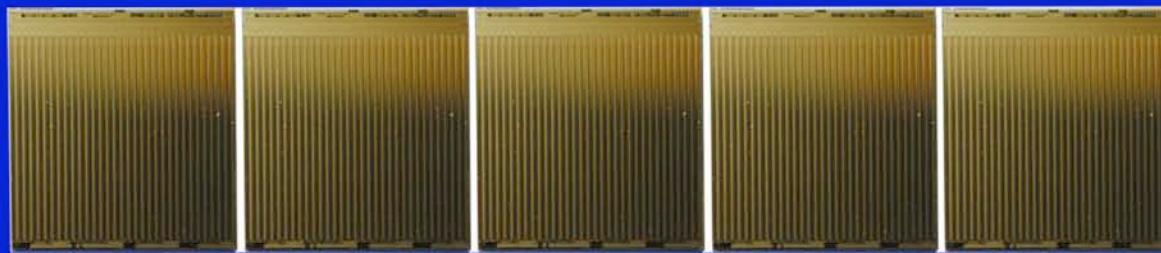
13.7 mm

15.6 mm

Sab



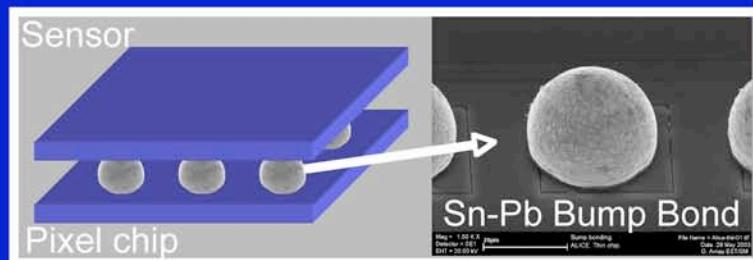
Sensor & pixel chips



5 readout chips/sensor
0.25 μ m CMOS
13.68 mm x 15.58 mm
thinned to 150 μ m



p-in-n silicon sensor
72.72 mm x 13.92 mm
200 μ m thin



40960 bump bonds
 \sim 25 μ m diameter
Stand-off:
 \sim 12 μ m (Pb-Sn)

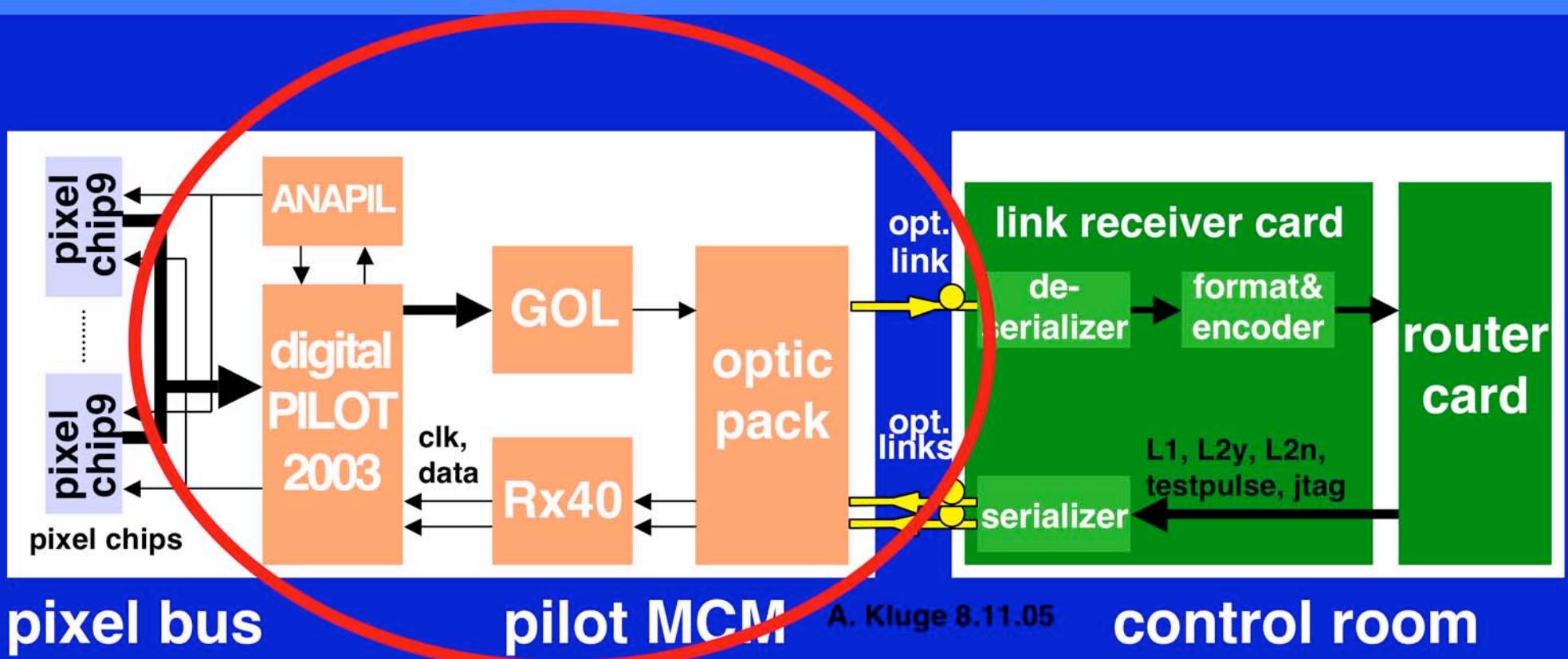


Sab

On detector electronics elements

- The pixel chip & sensors
- Read-out Multi chip module + ASICs
- Al Multi-layer kapton cables (Bus)

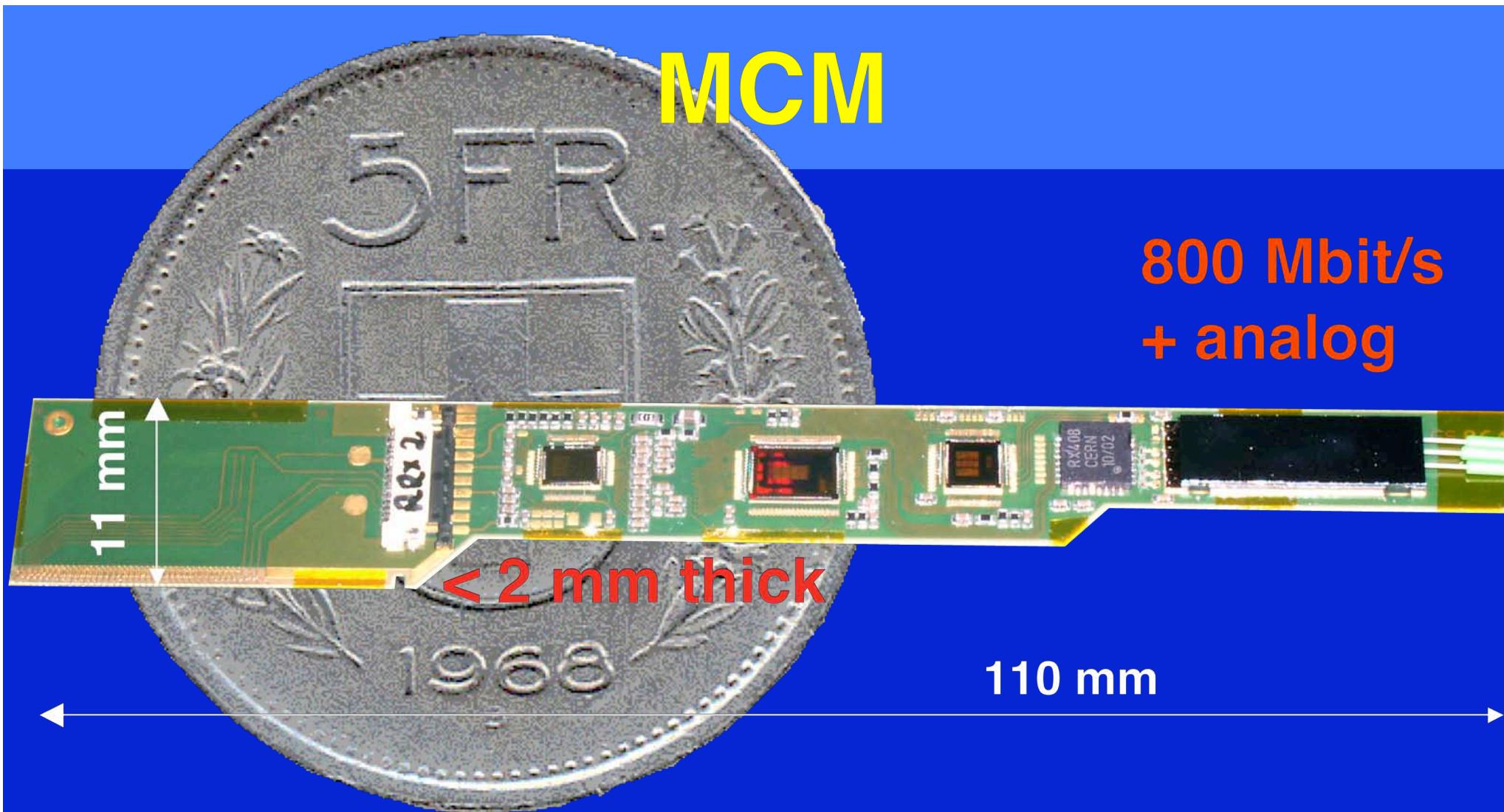
Pixel read out system



MCM

800 Mbit/s
+ analog





MCM

800 Mbit/s
+ analog

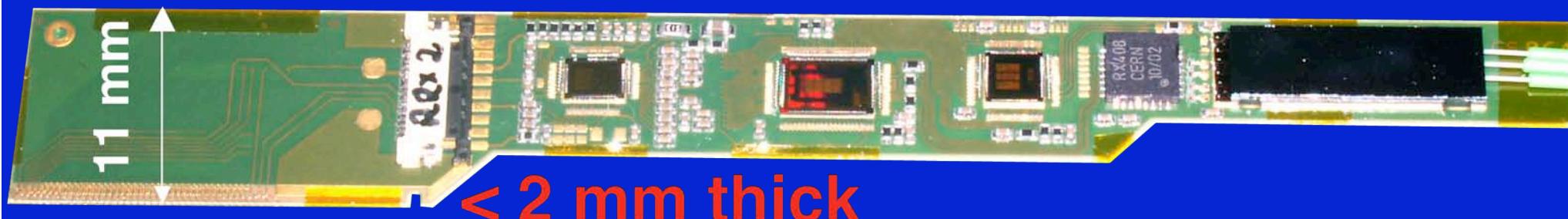


MCM

No Copper connections

No data processing, no memory

**800 Mbit/s
+ analog**



Analog (10mV) + digital (800Mbit/s)

Dense, comp. placement, routing

Fragile: thin, no packages

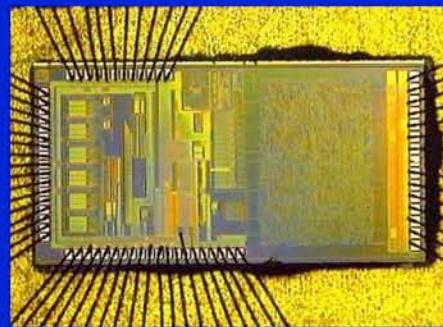
Small quantity

Small: limited reworking

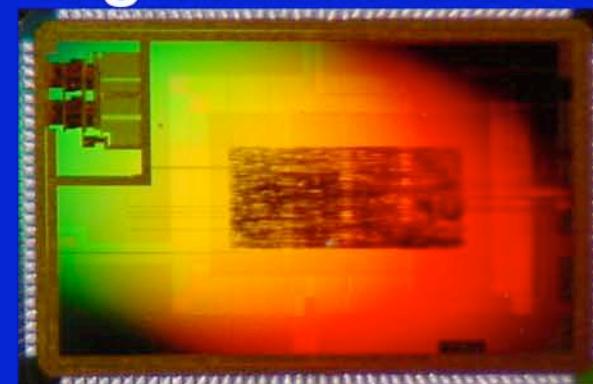
A. Kluge

Pilot MCM ASICs

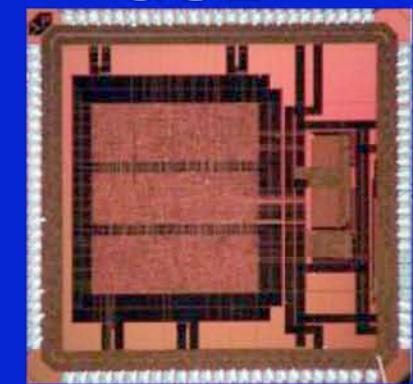
ANAPIL3



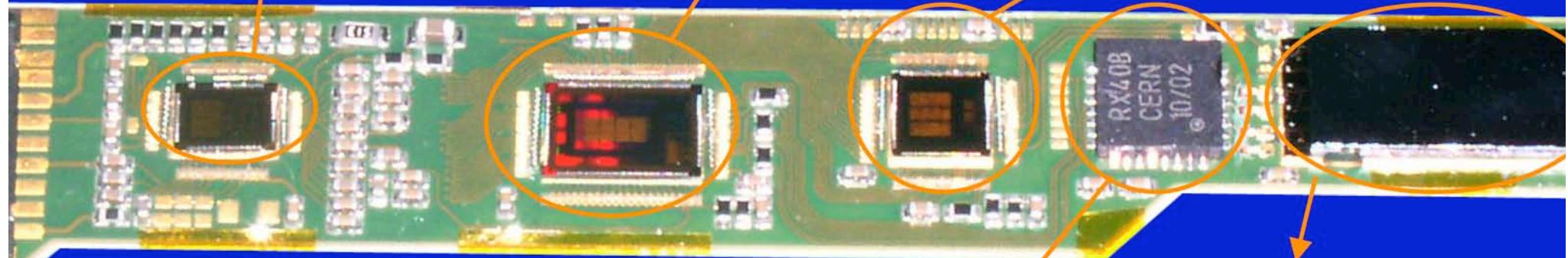
Digital Pilot 2003



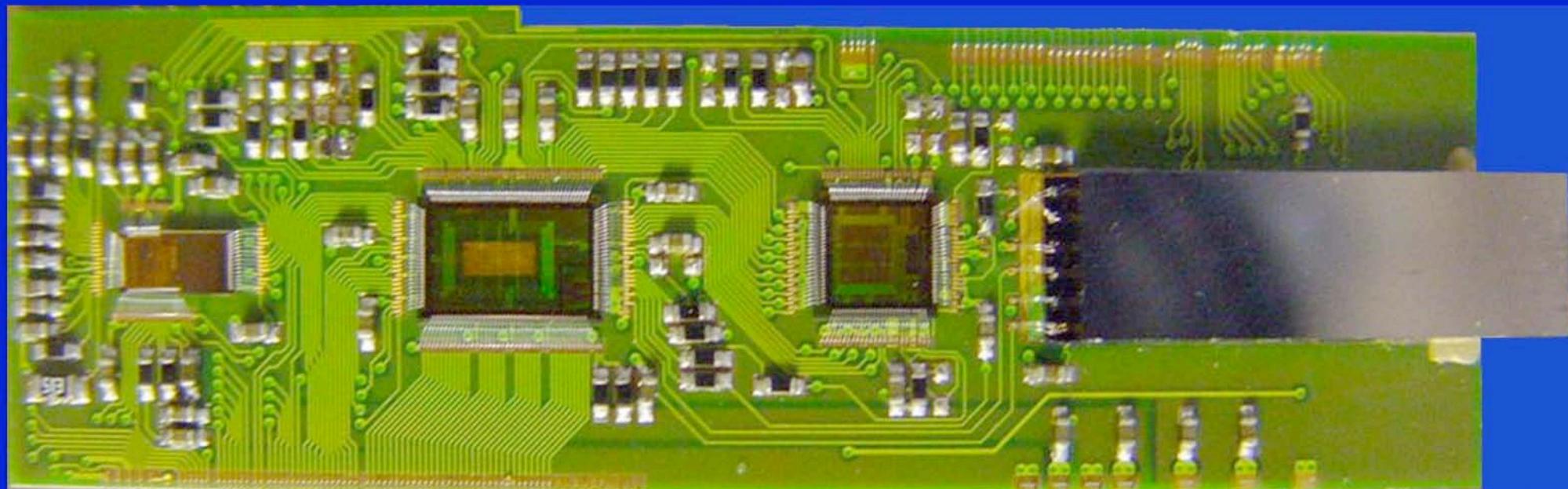
GOL



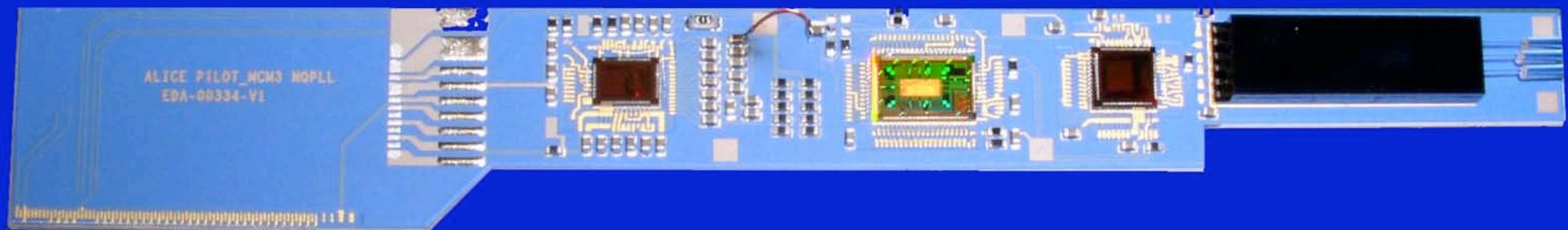
PILOT MCM



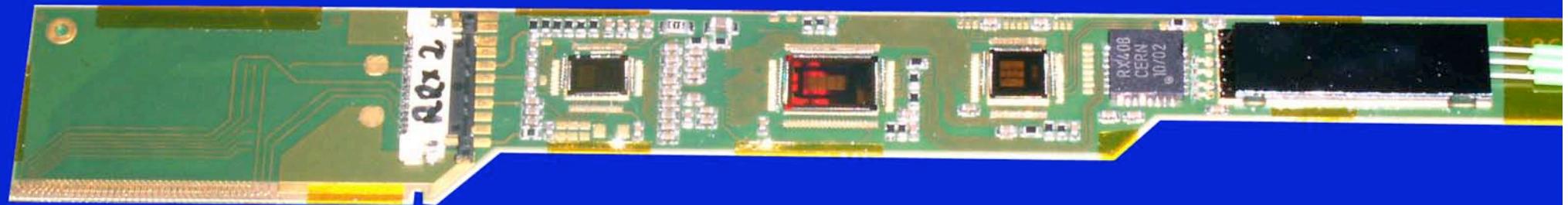
Pilot MCM ASICs



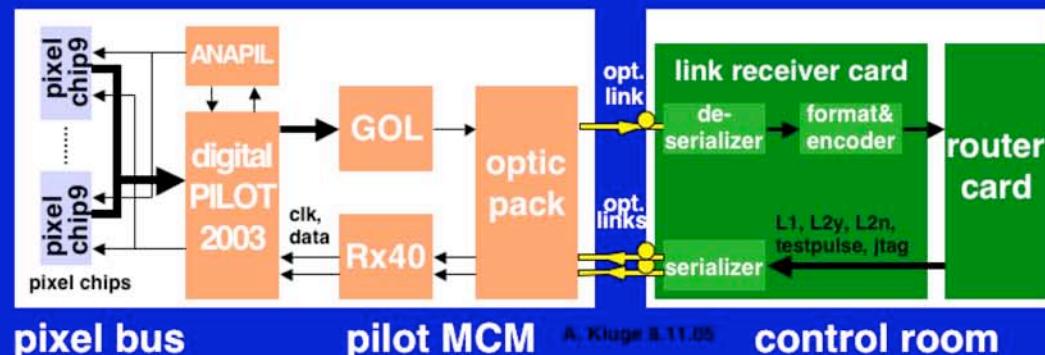
Pilot MCM ASICs



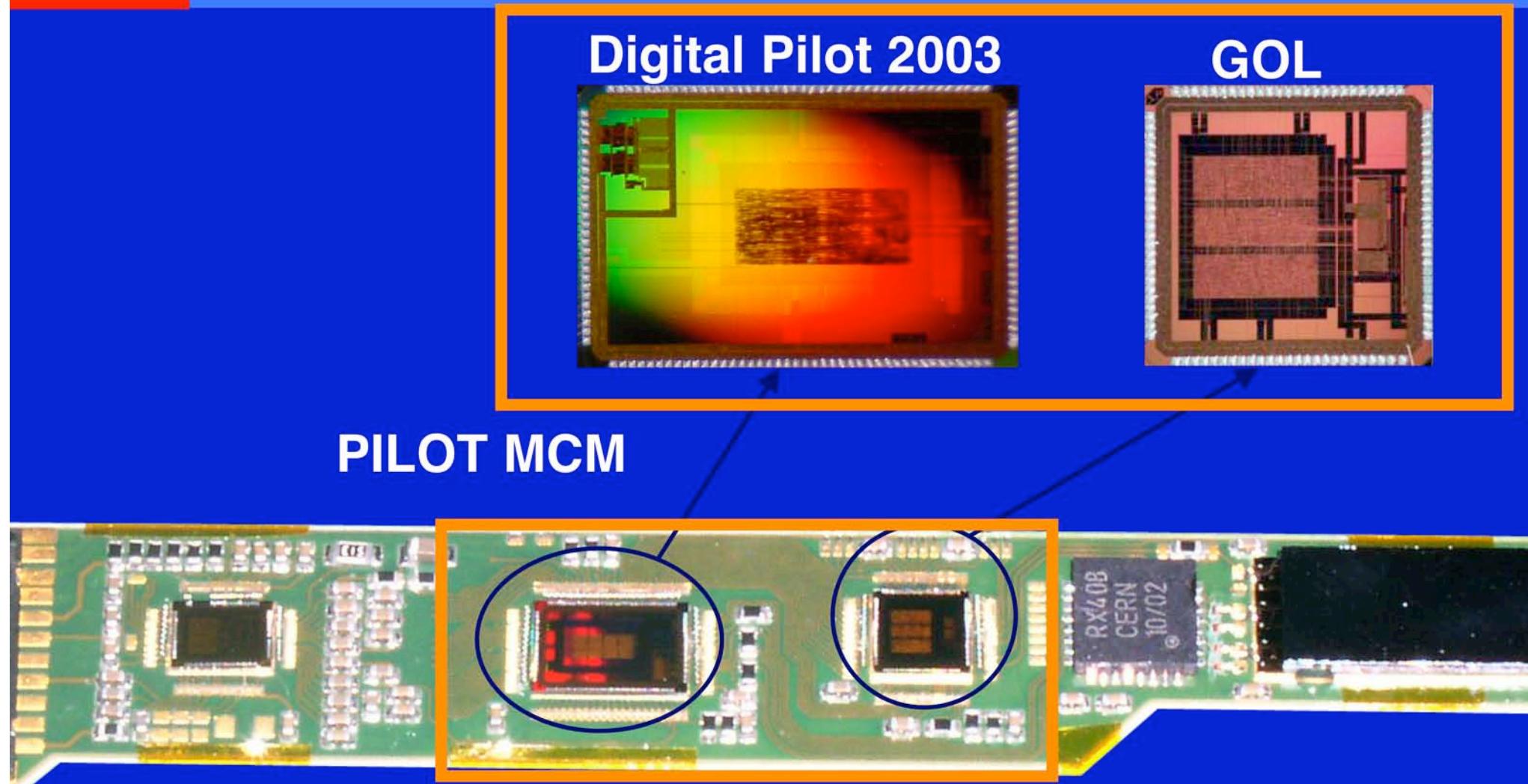
MCM



Complexity due to connectivity, limited space, number of signals (bus width, analog bias) and late integration design.



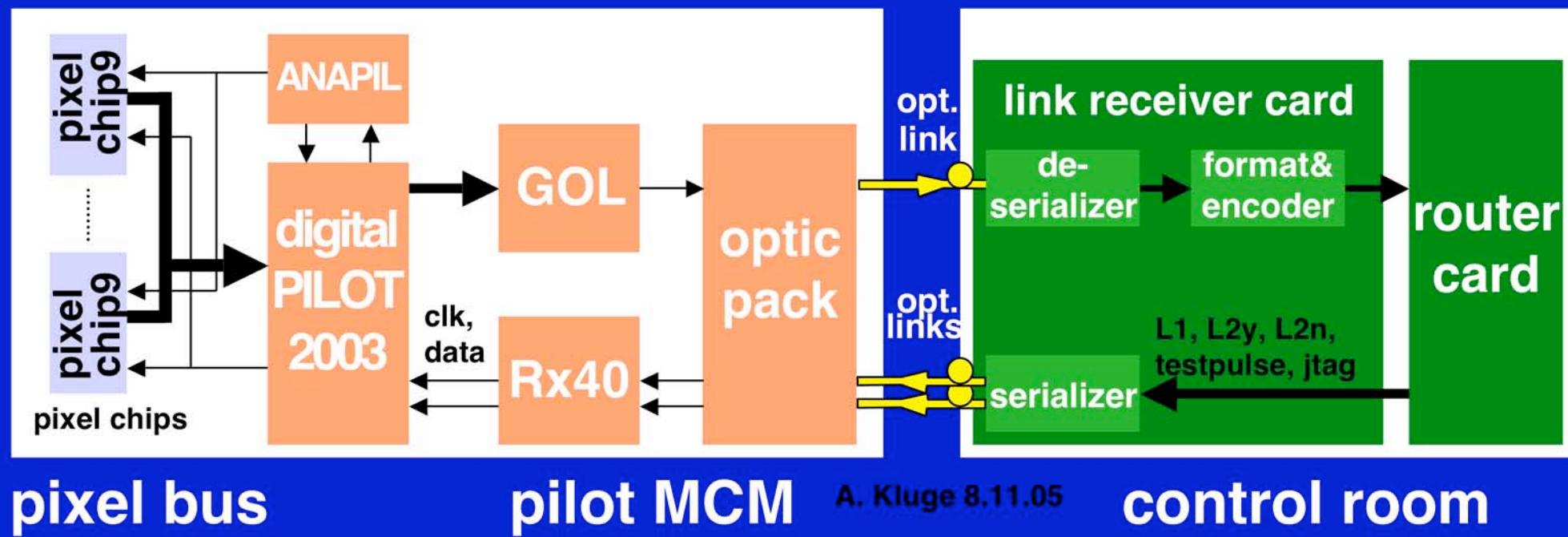
Pilot MCM ASICs



On detector electronics elements

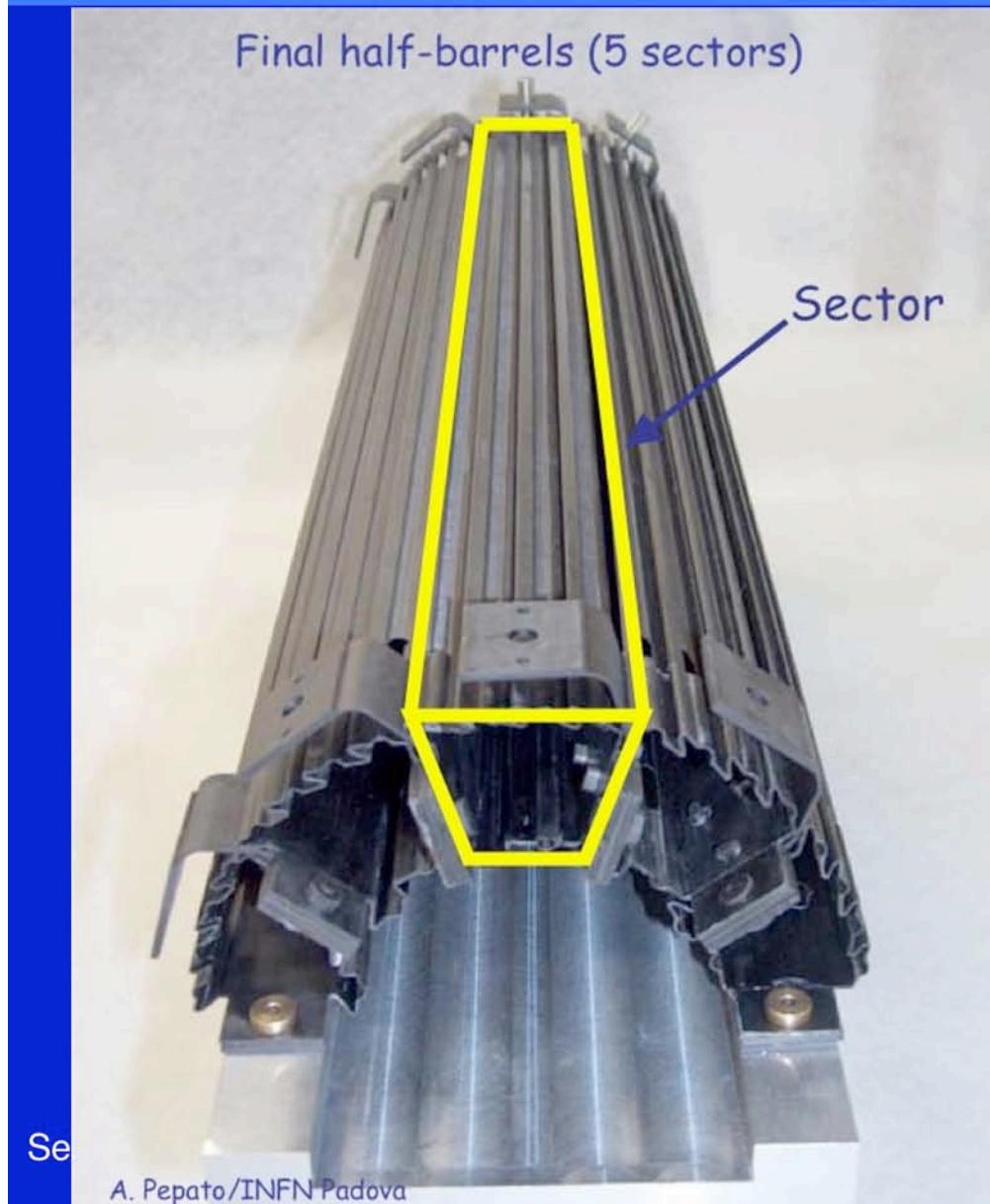
- The pixel chip & sensors
- Multi chip module + ASICs
- Al Multi-layer kapton cable (Bus)

Pixel read out system



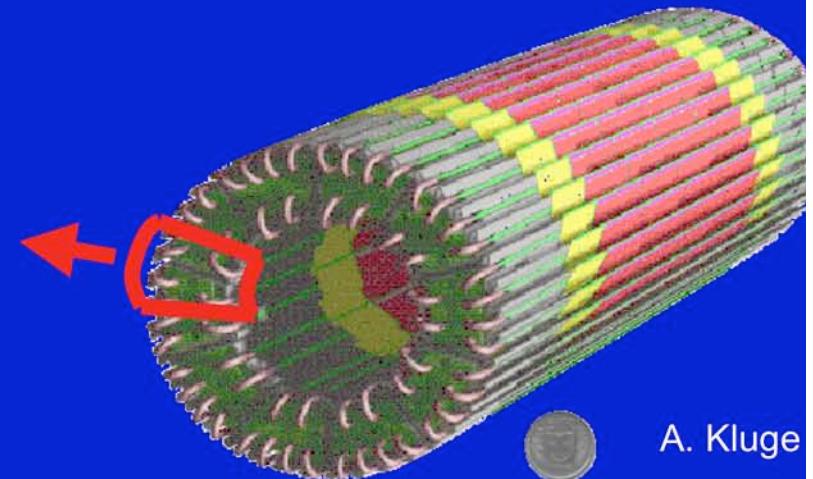
On detector electronics integration

Integration

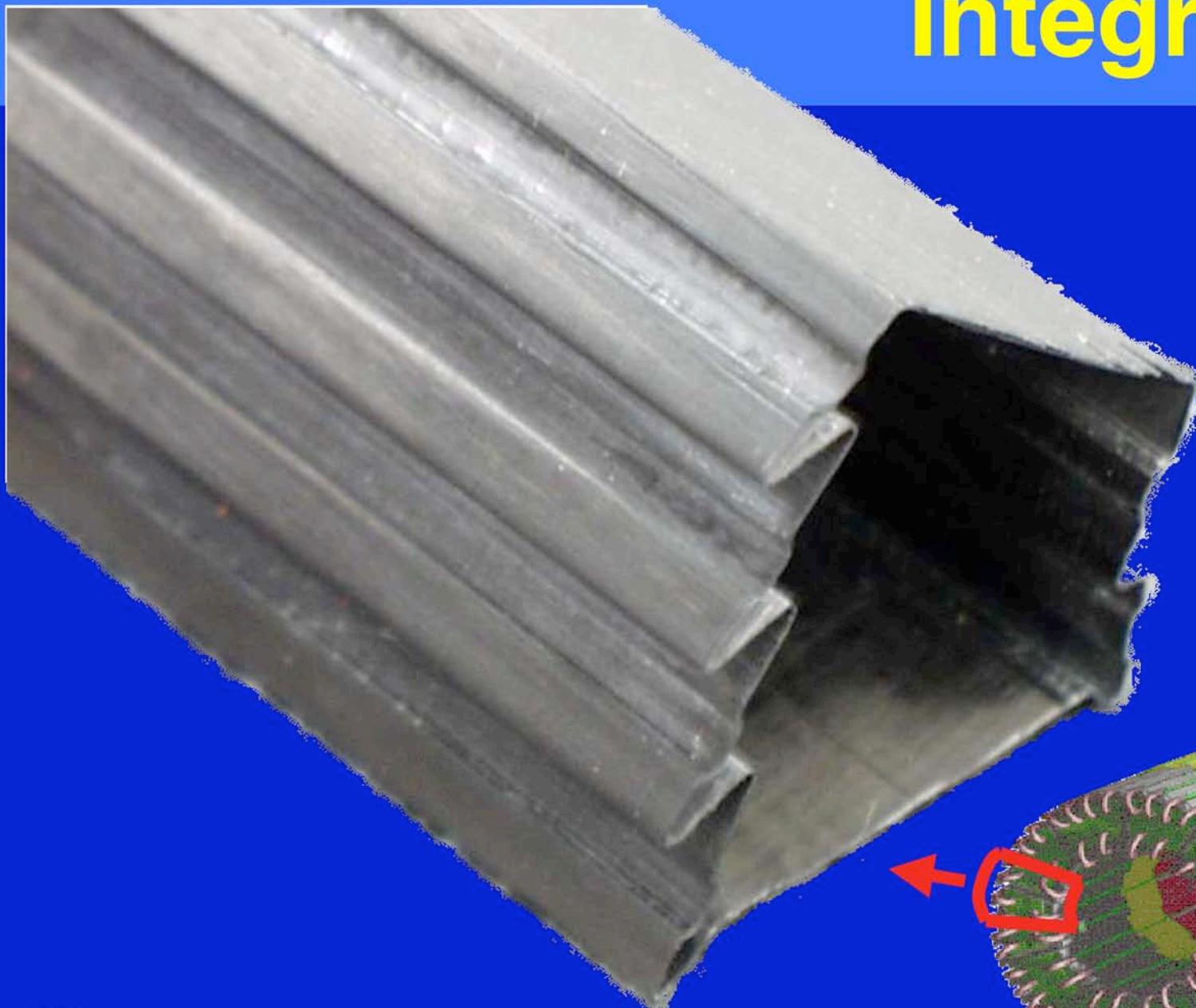


200 μm carbon fiber support

40 μm PHYNOX cooling tubes integrated



Integration

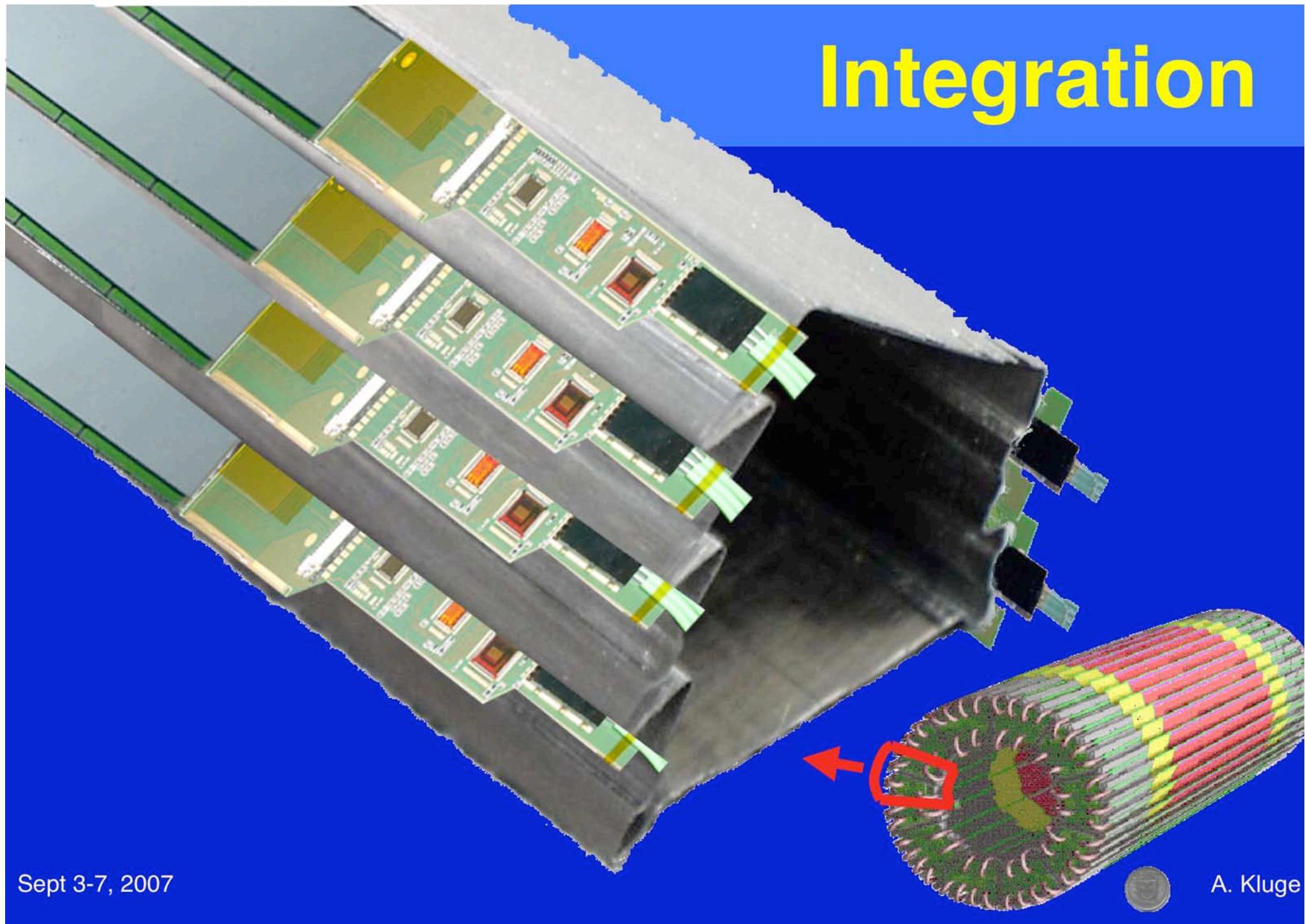


Sept 3-7, 2007



A. Kluge

Integration

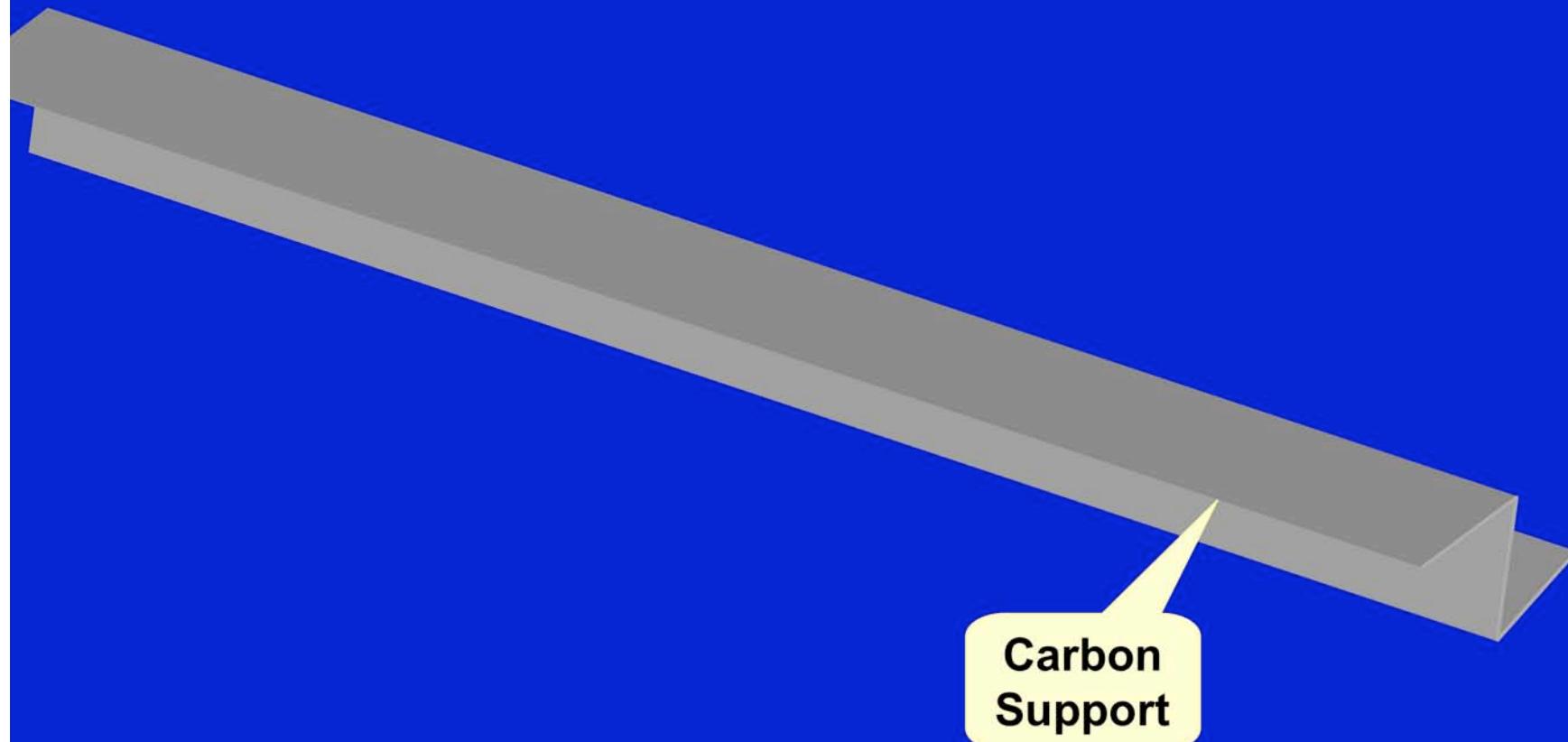


Sept 3-7, 2007

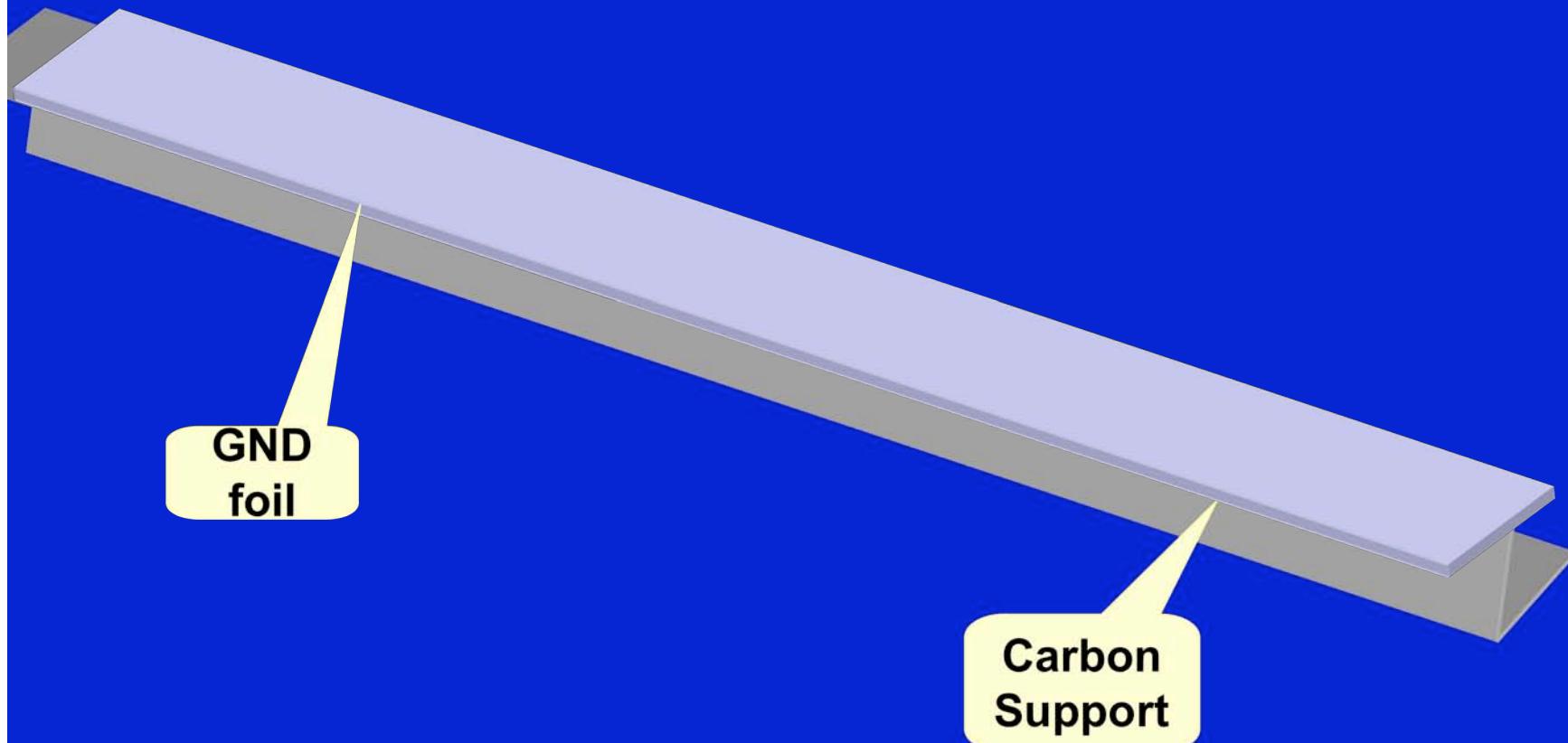


A. Kluge

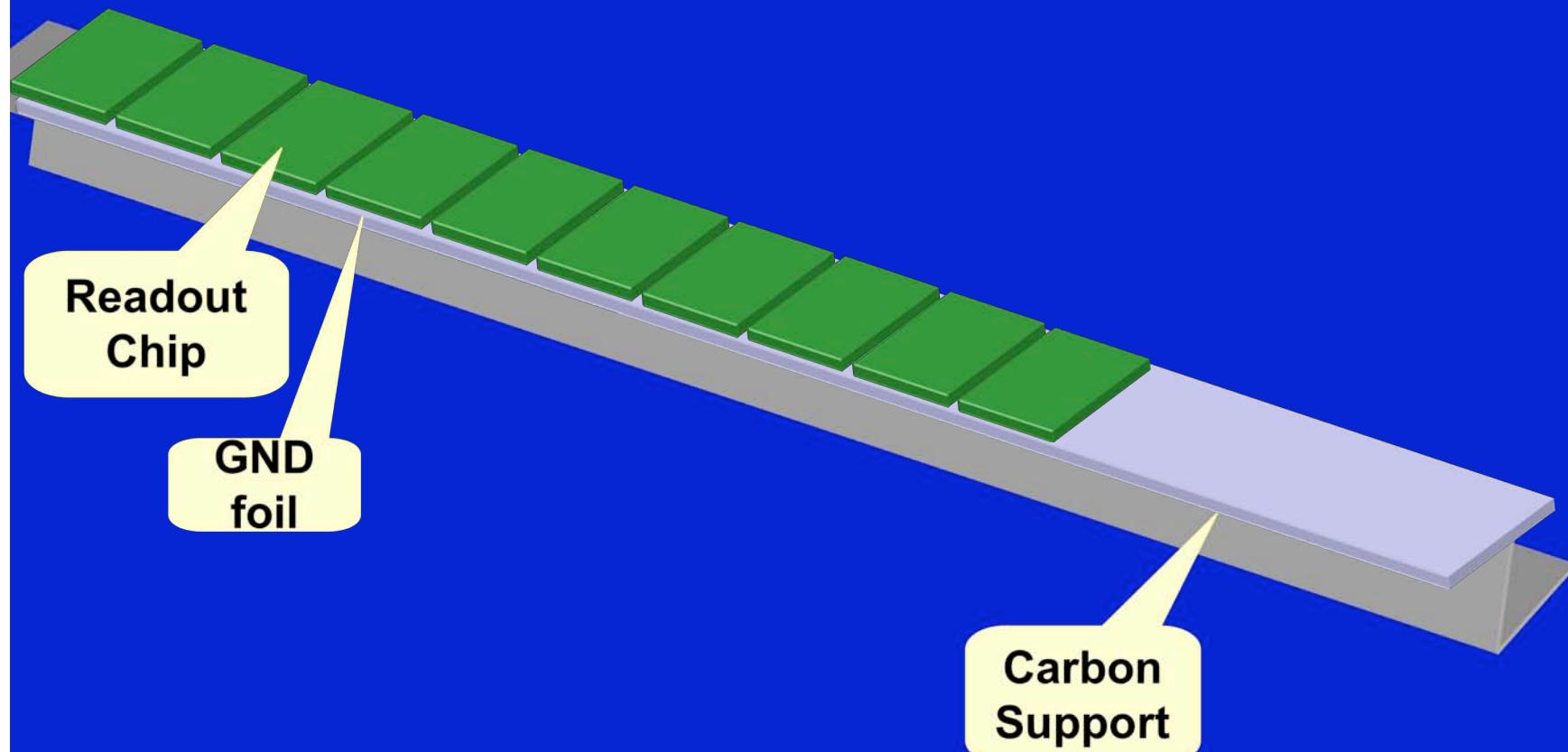
Electronics integration



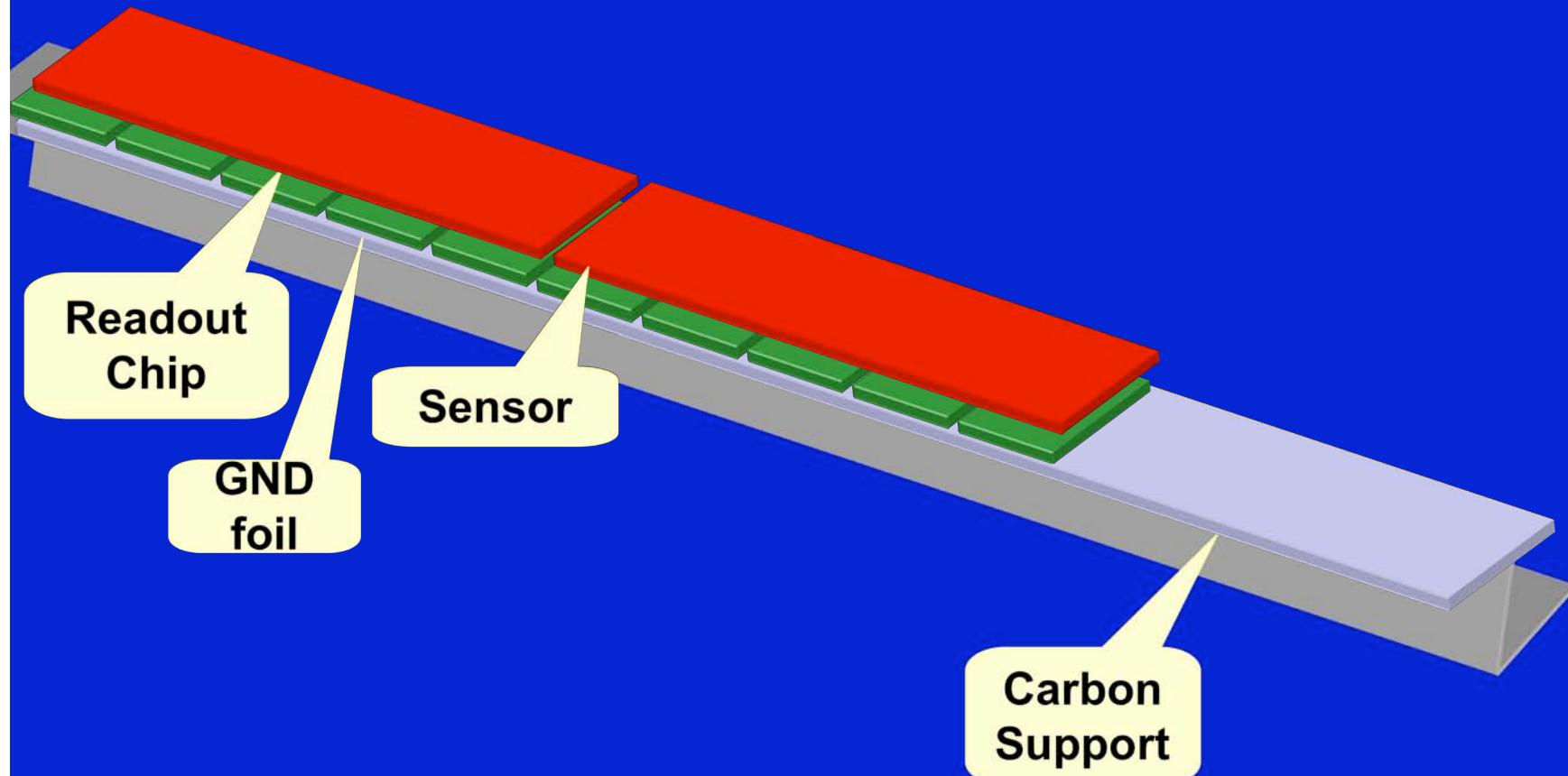
Electronics integration



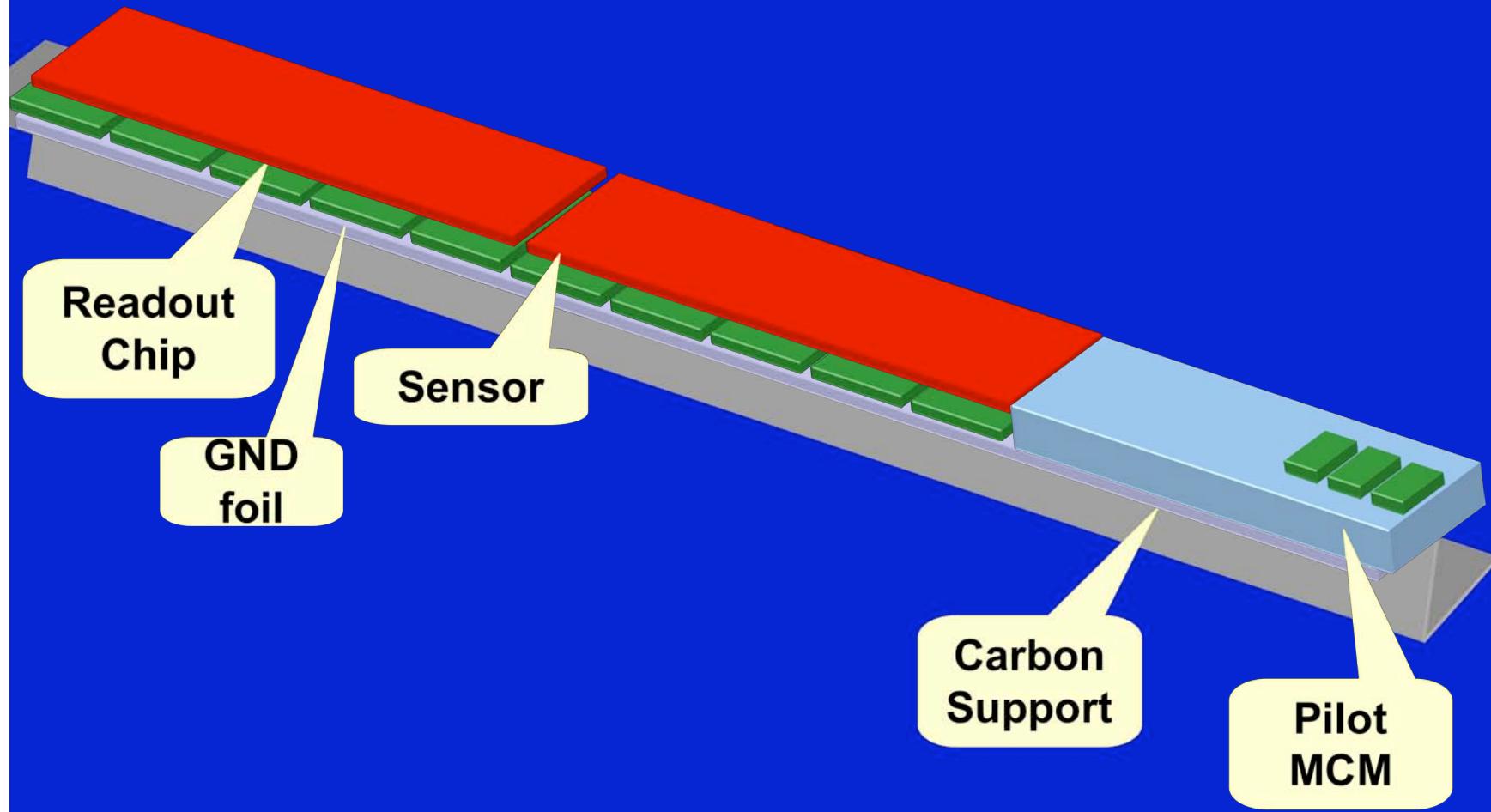
Electronics integration



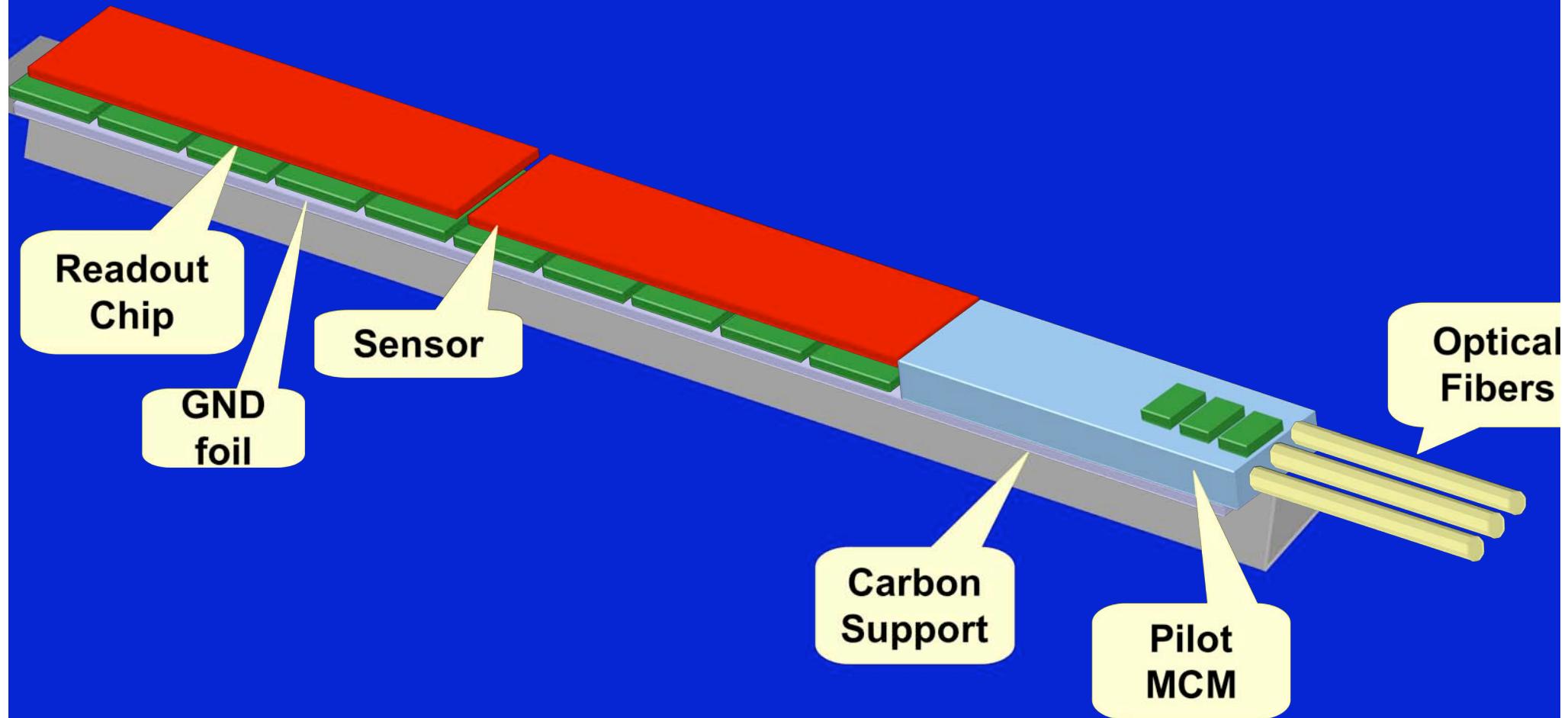
Electronics integration



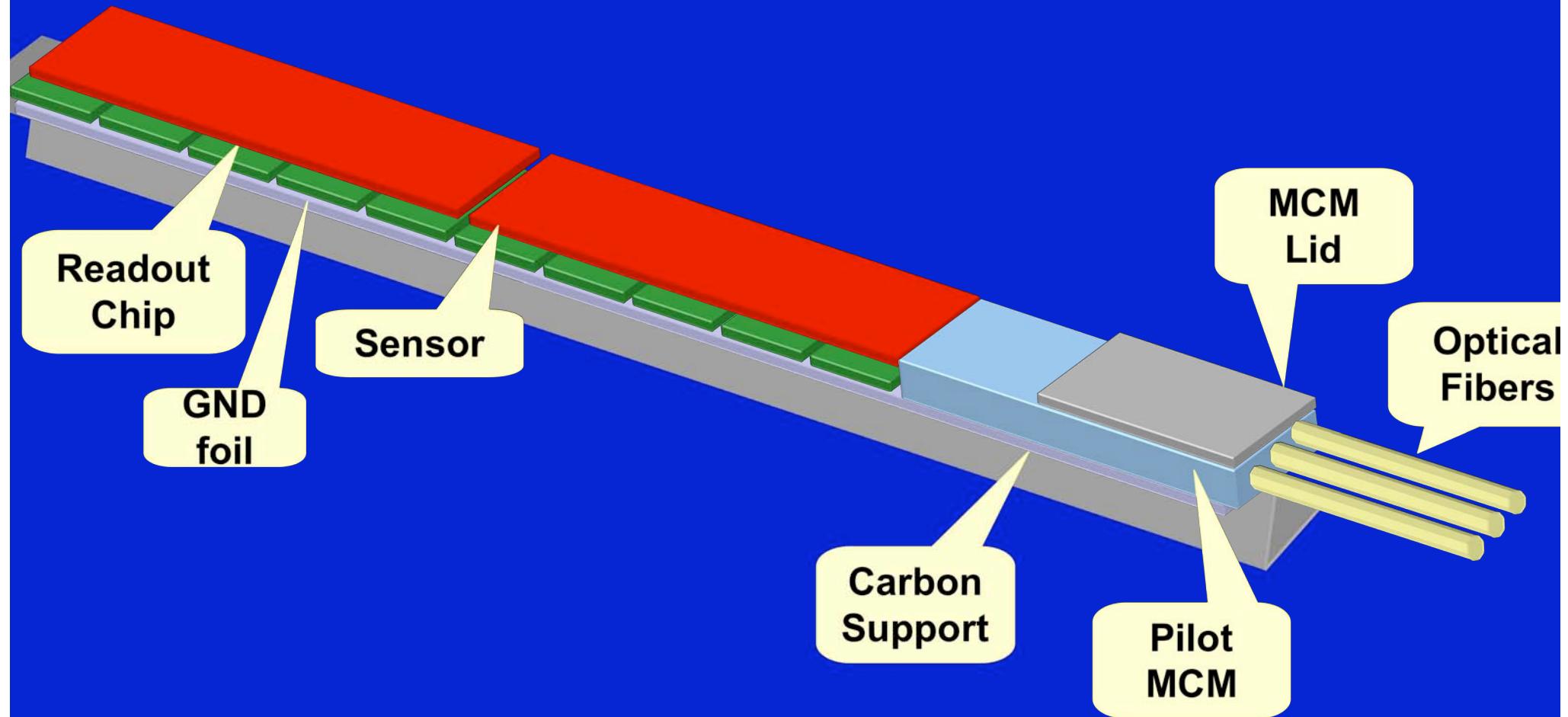
Electronics integration



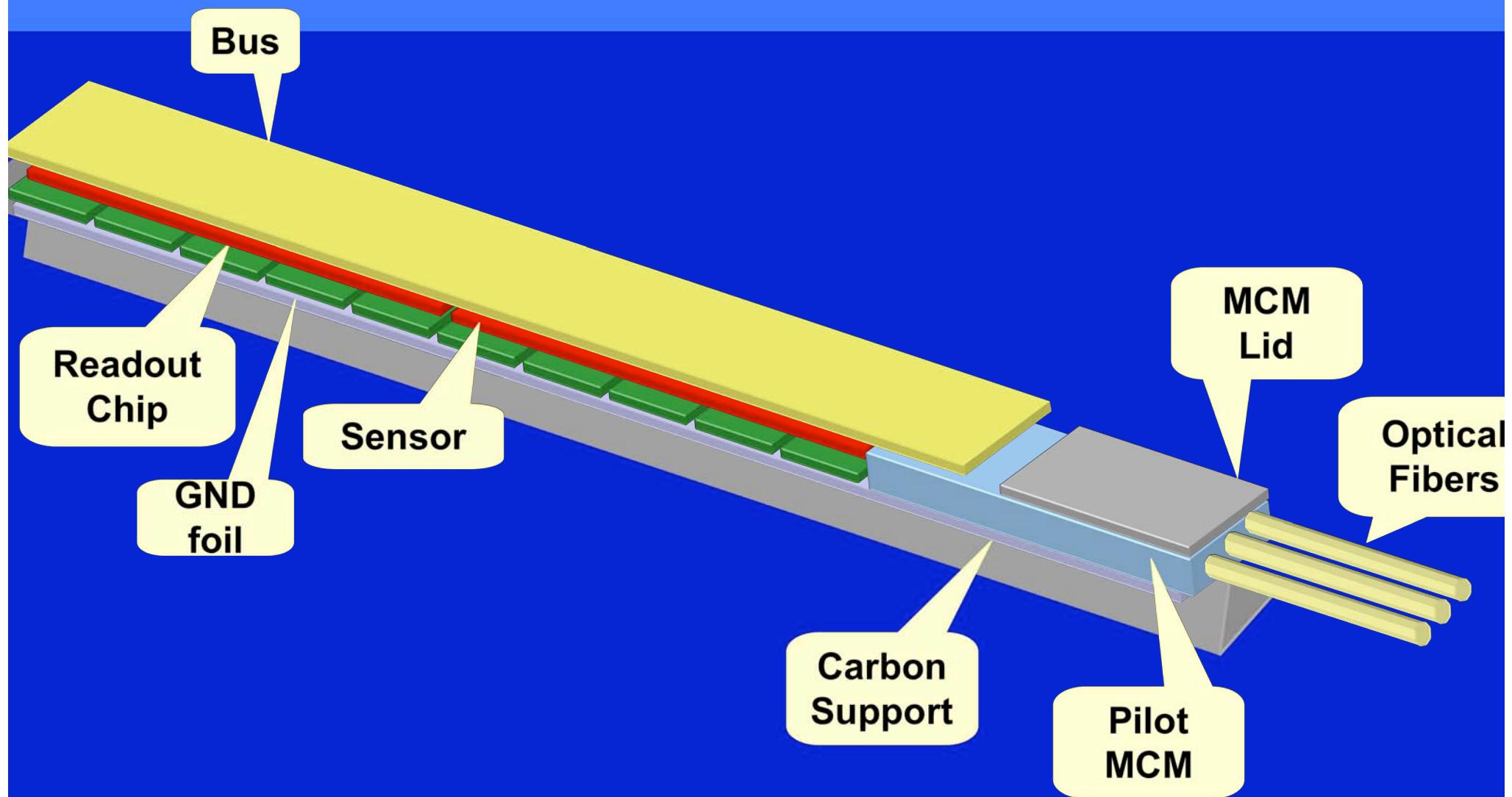
Electronics integration



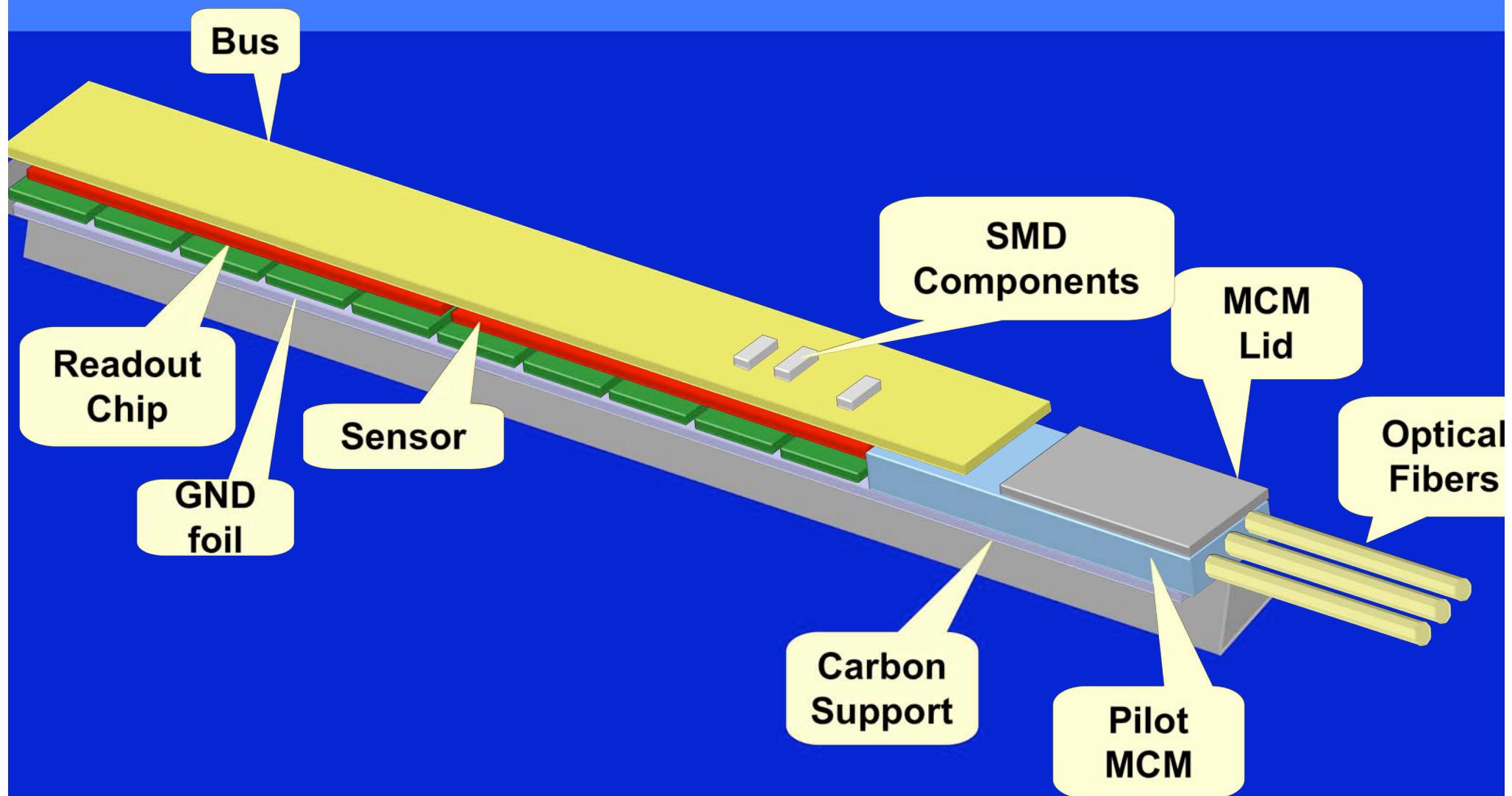
Electronics integration



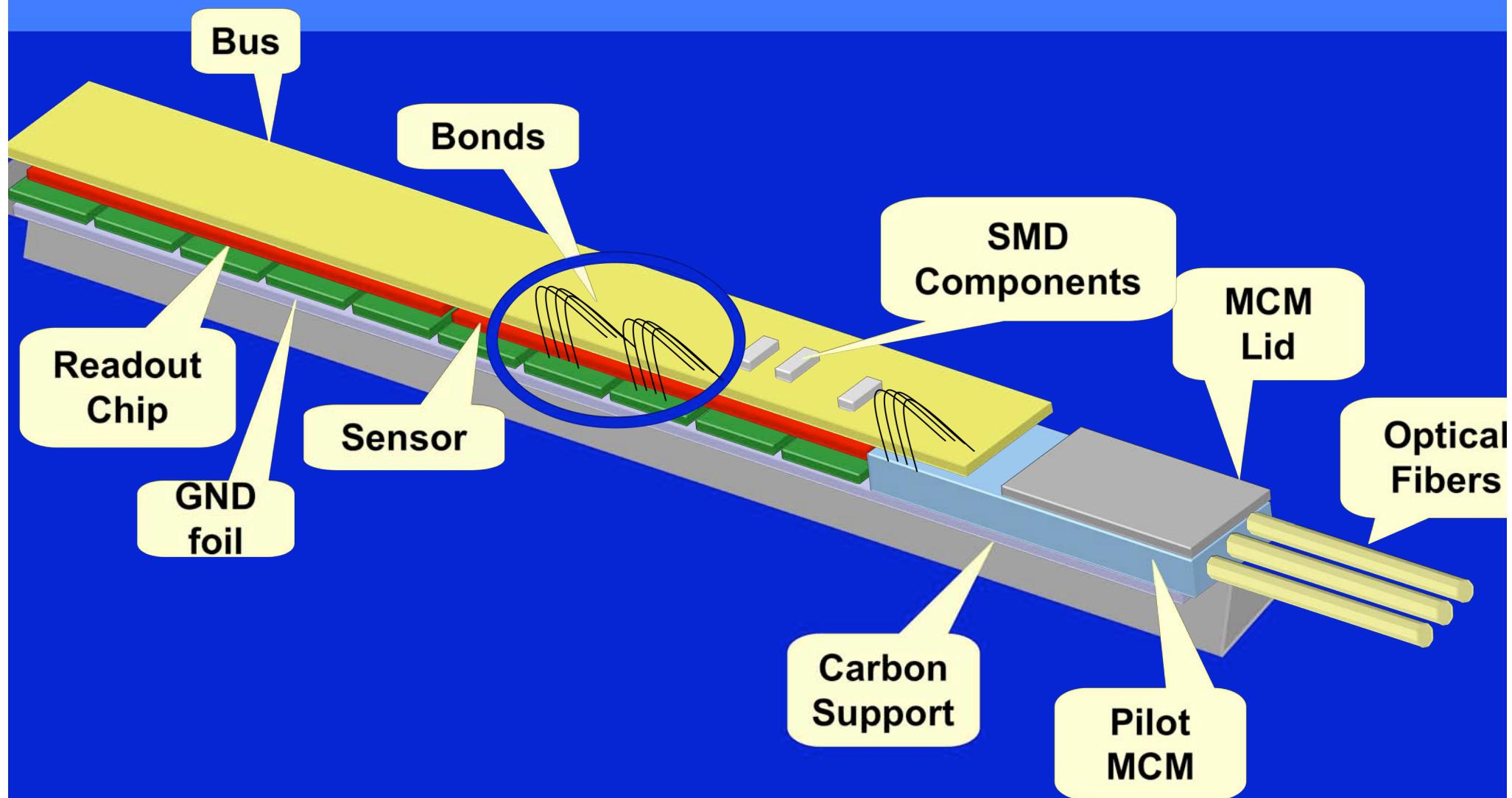
Electronics integration



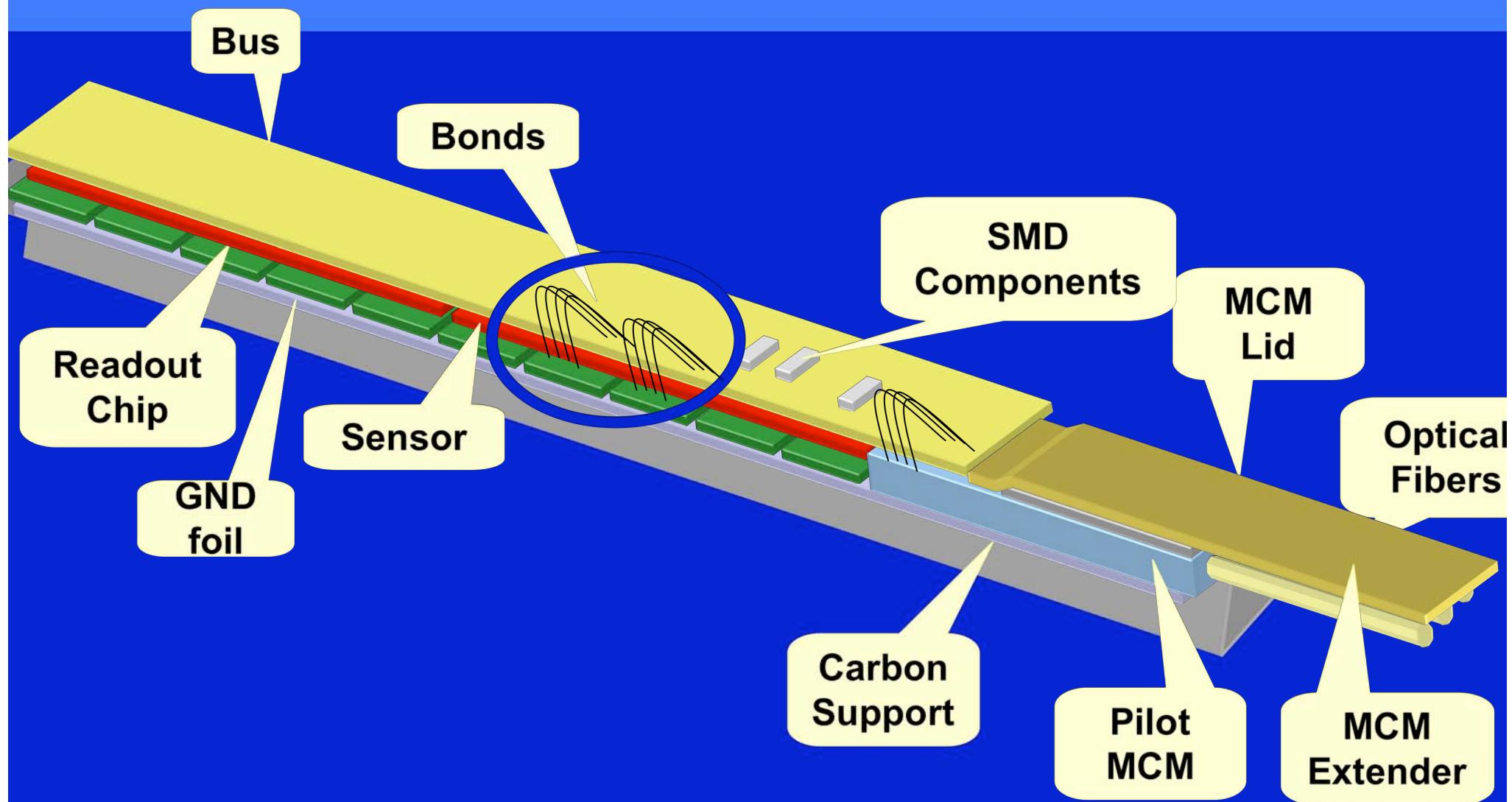
Electronics integration



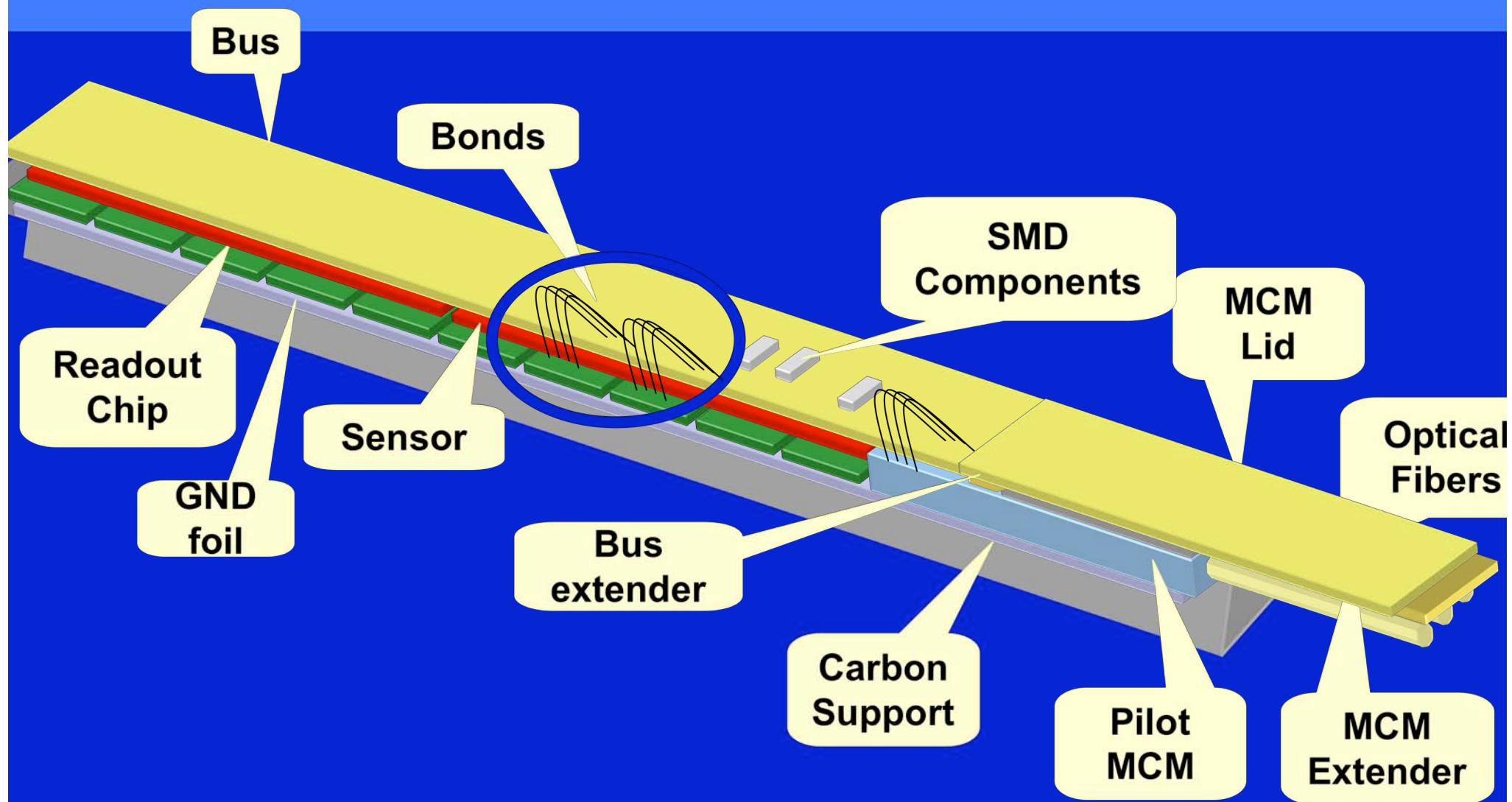
Electronics integration



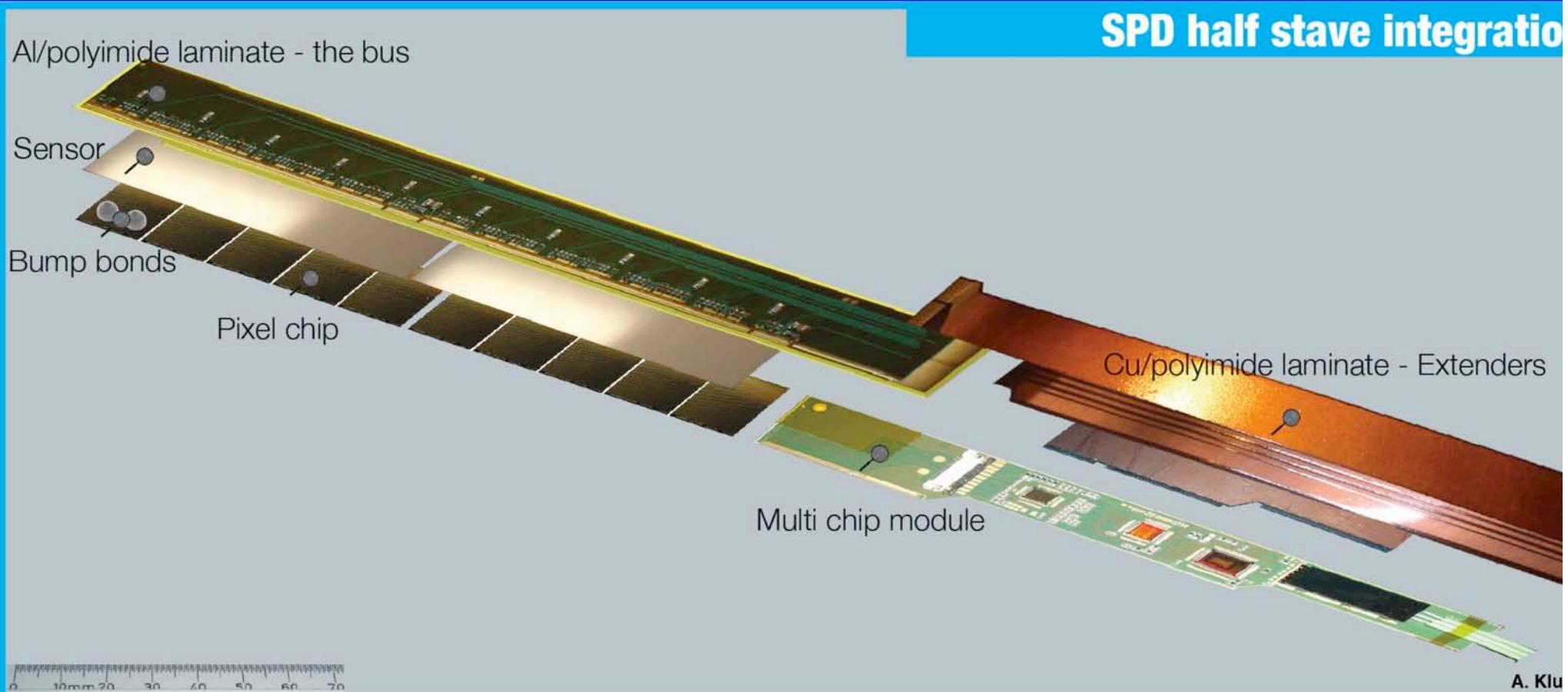
Electronics integration



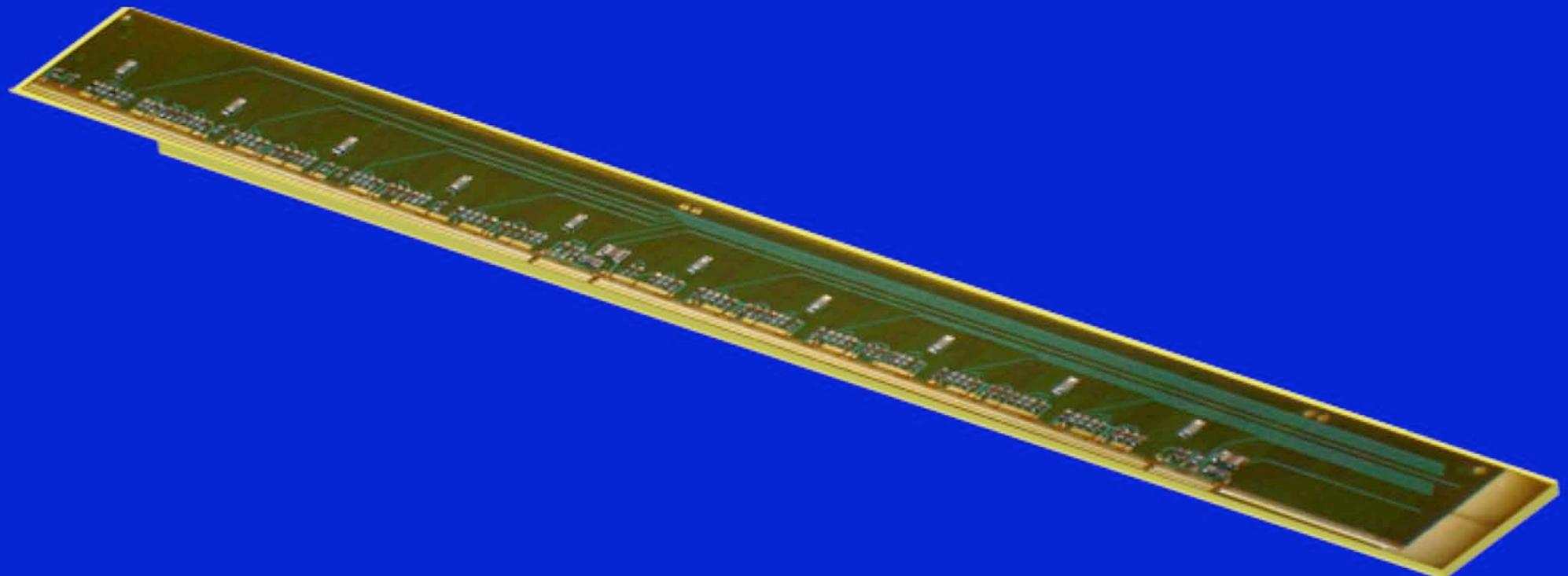
Electronics integration



Electronics integration



The pixel bus



The pixel bus

Aluminum

Length: ~ 20 cm, width ~13 mm

Total thickness: 220 μm

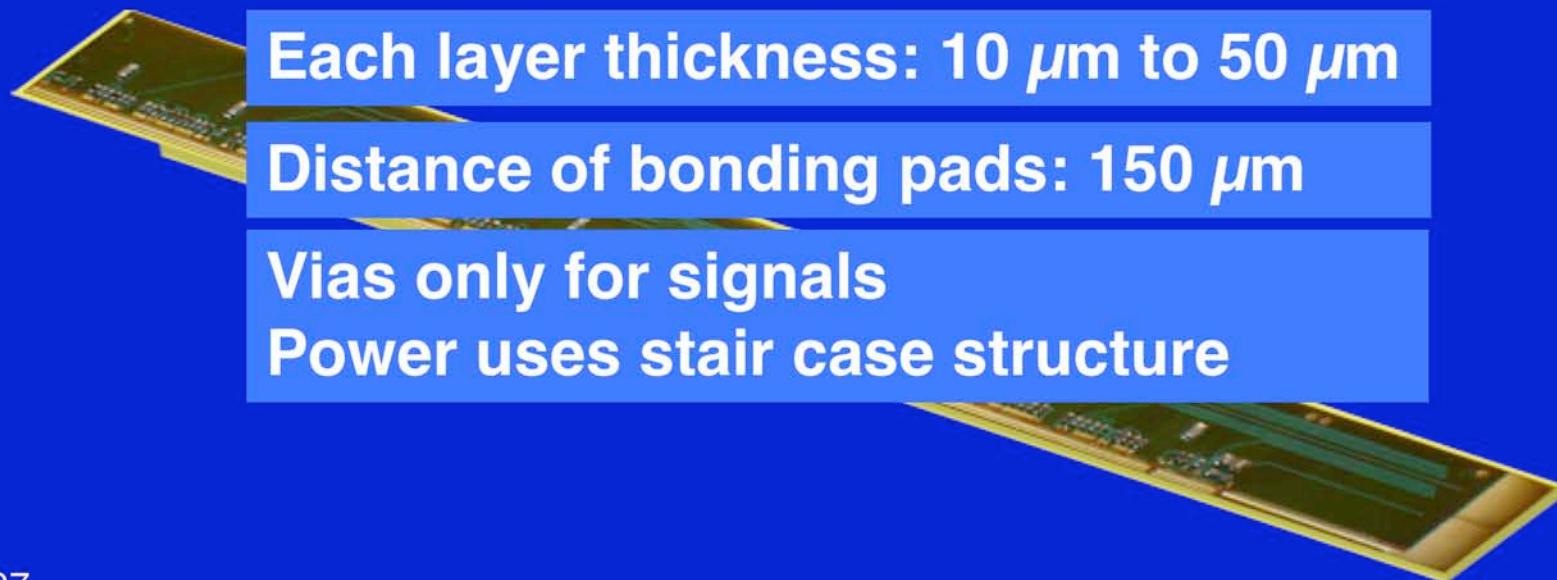
5 layers: Power, GND, 3 signal layers

Each layer thickness: 10 μm to 50 μm

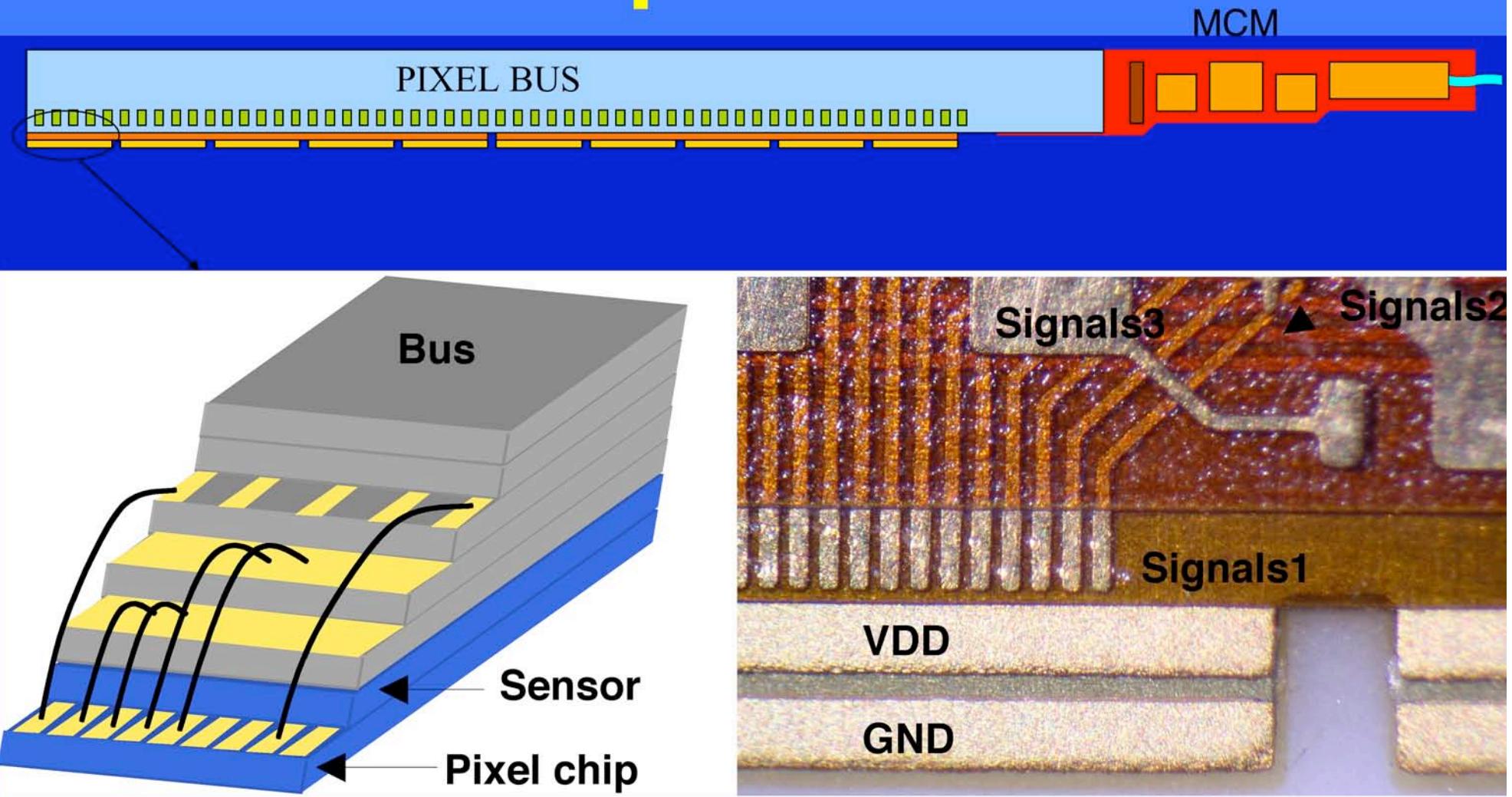
Distance of bonding pads: 150 μm

Vias only for signals

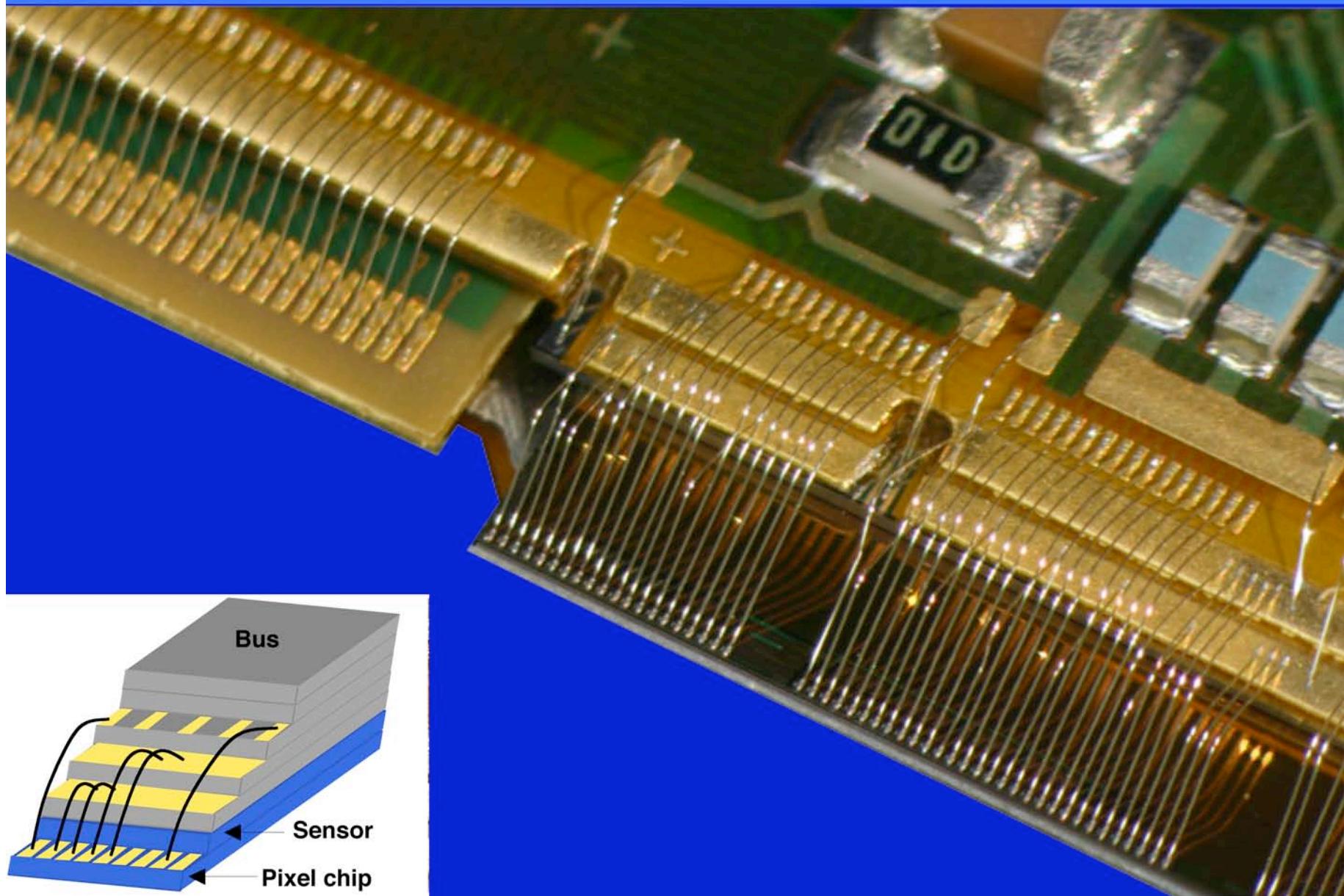
Power uses stair case structure



The pixel bus

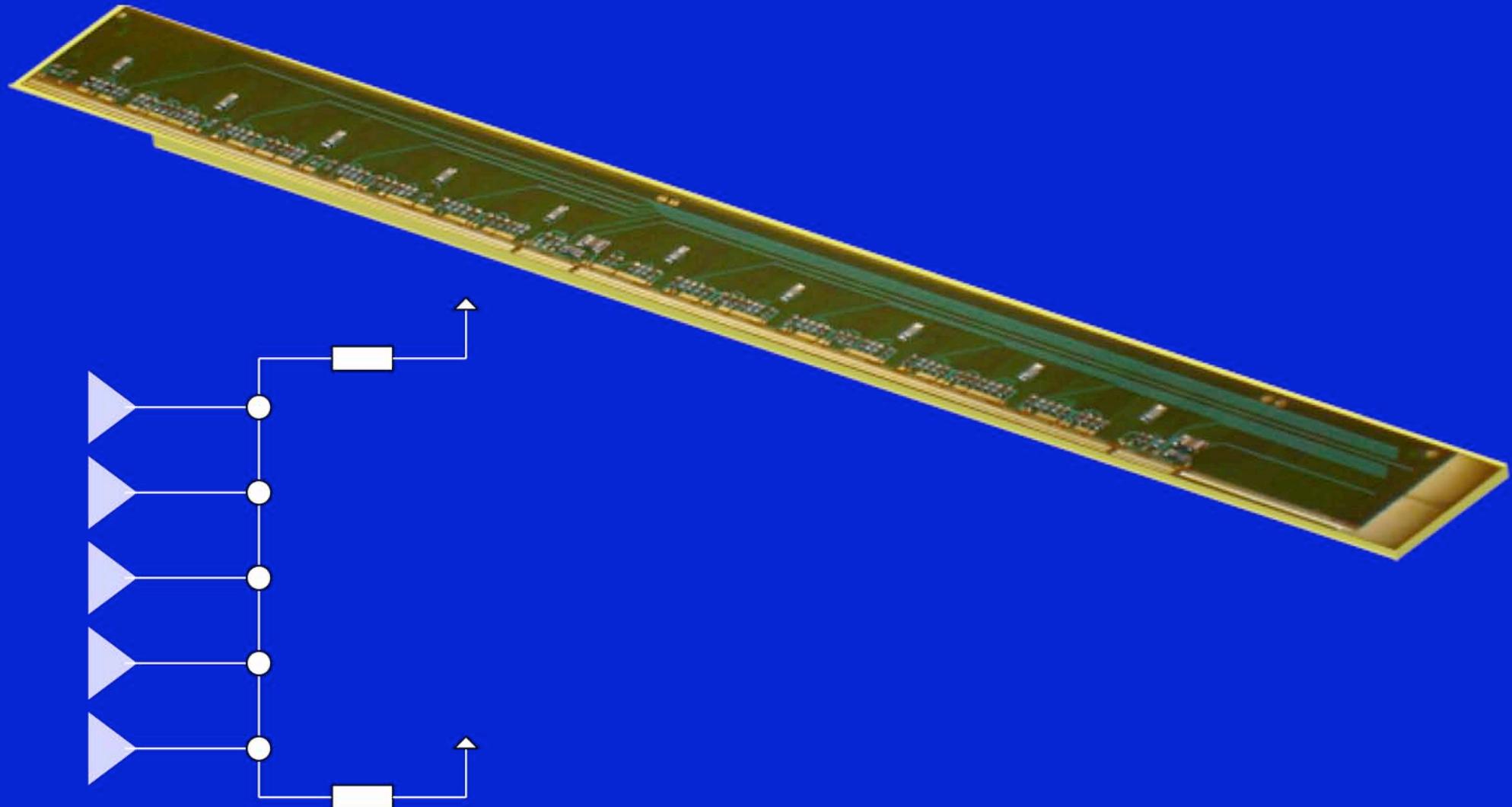


The pixel bus

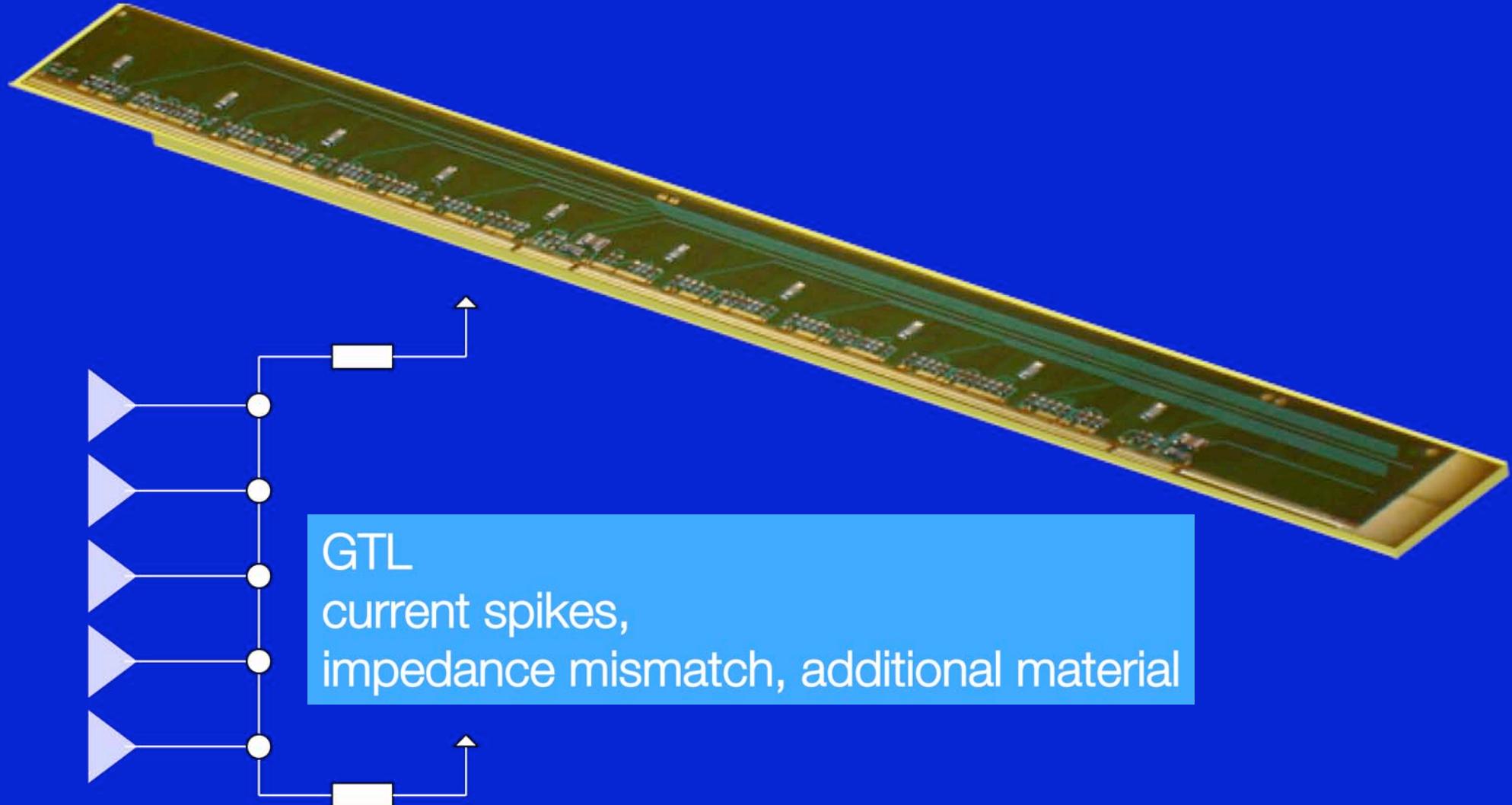


A. Kluge

The pixel bus

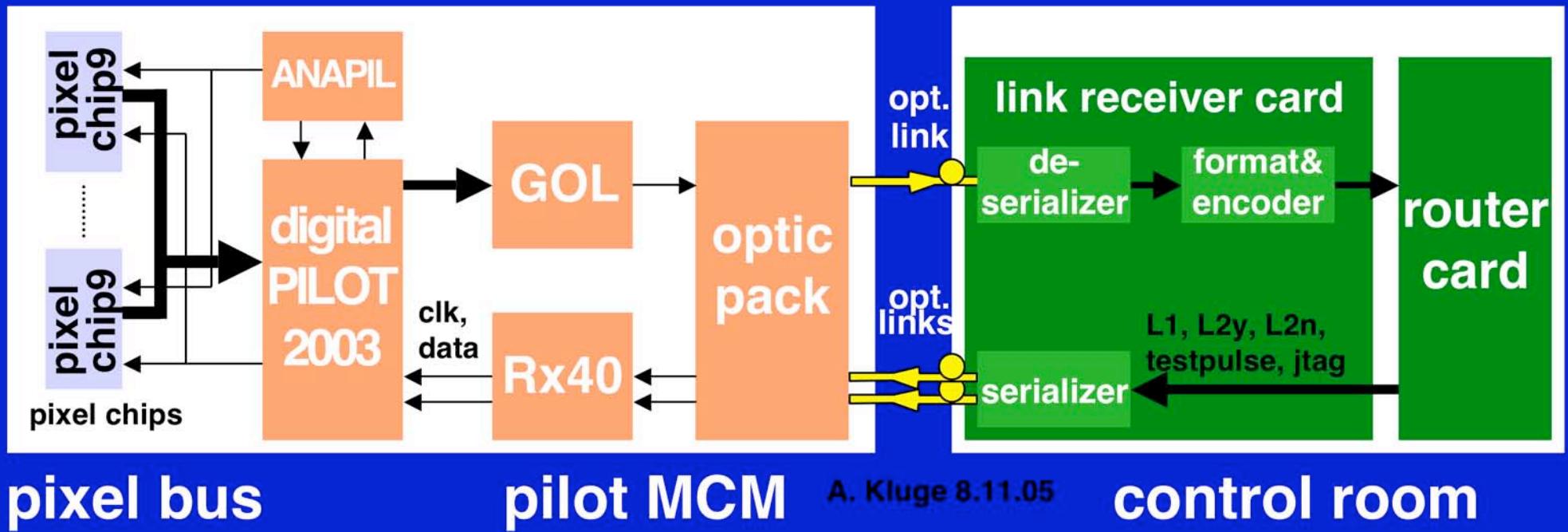


The pixel bus

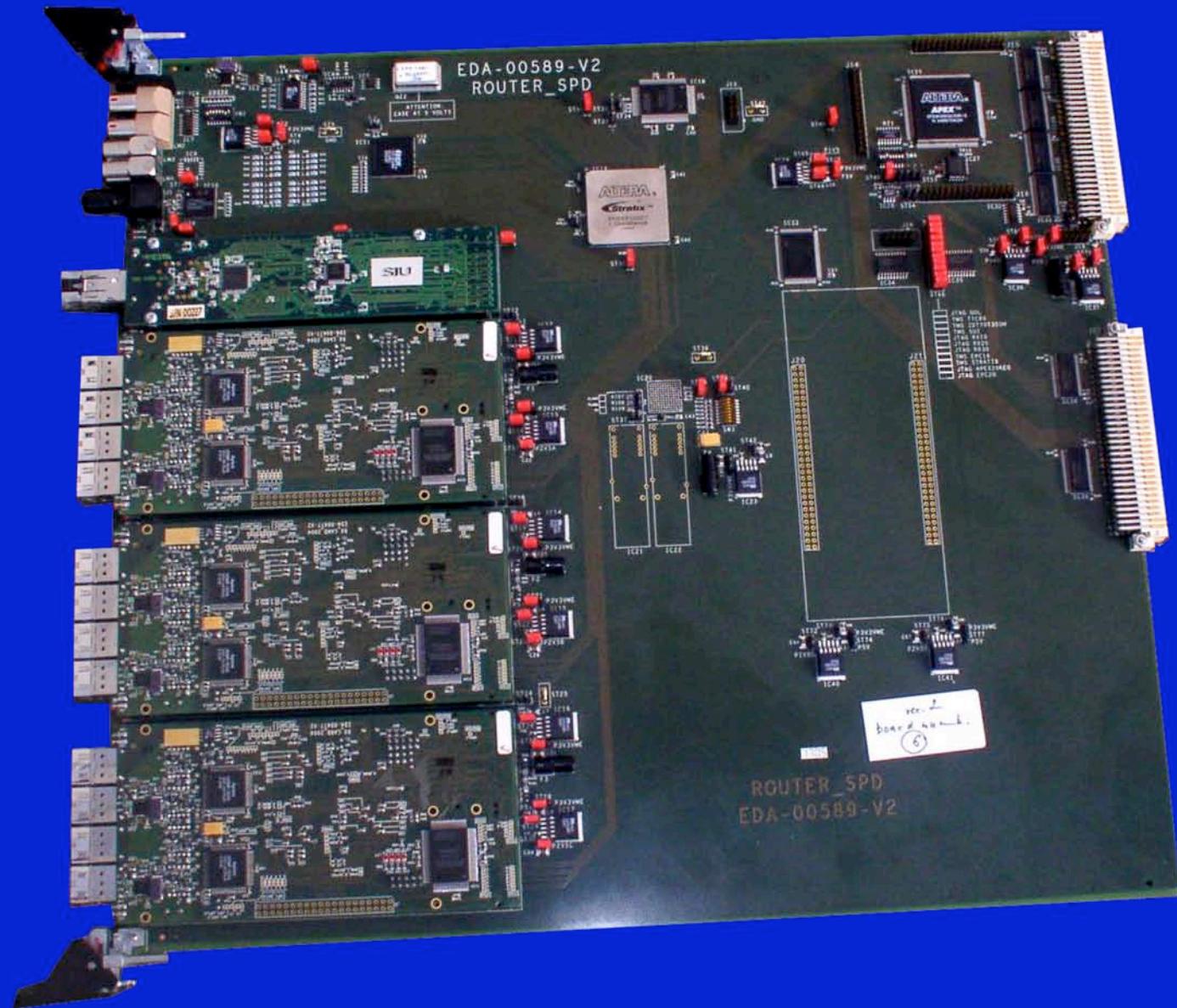


Off detector electronics

Off detector electronics

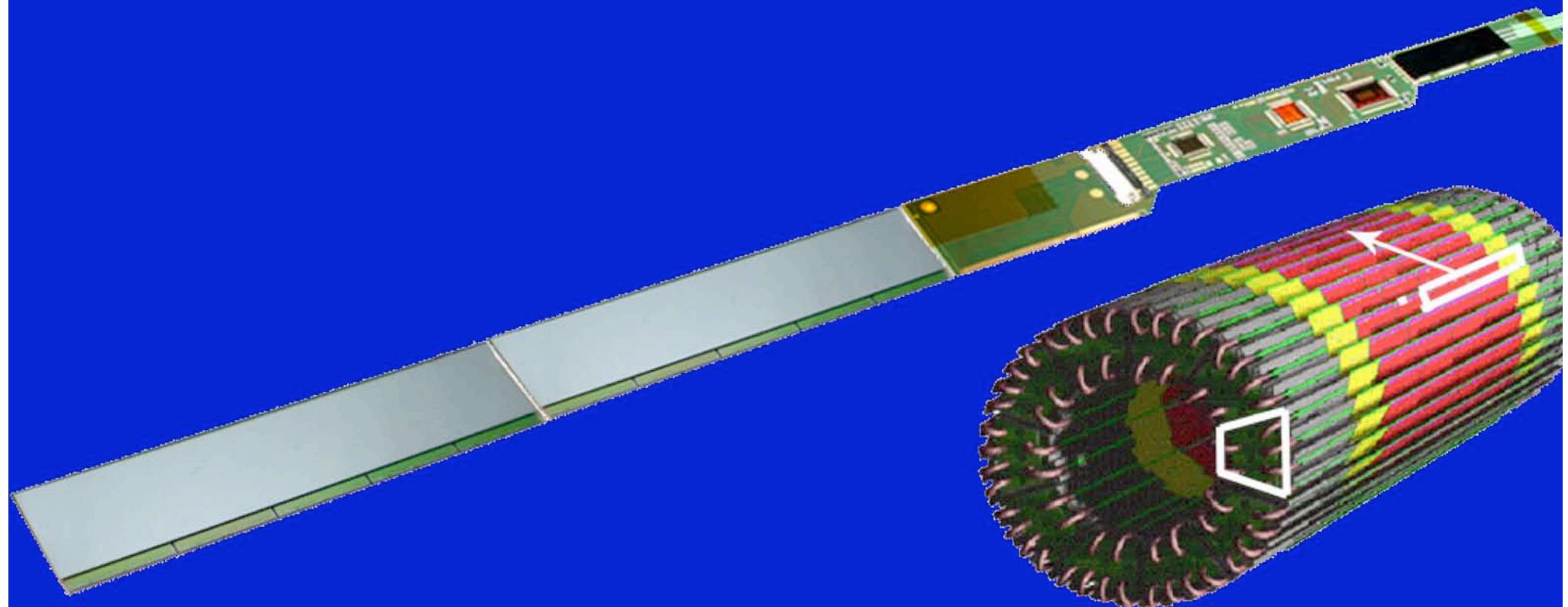


Off detector electronics

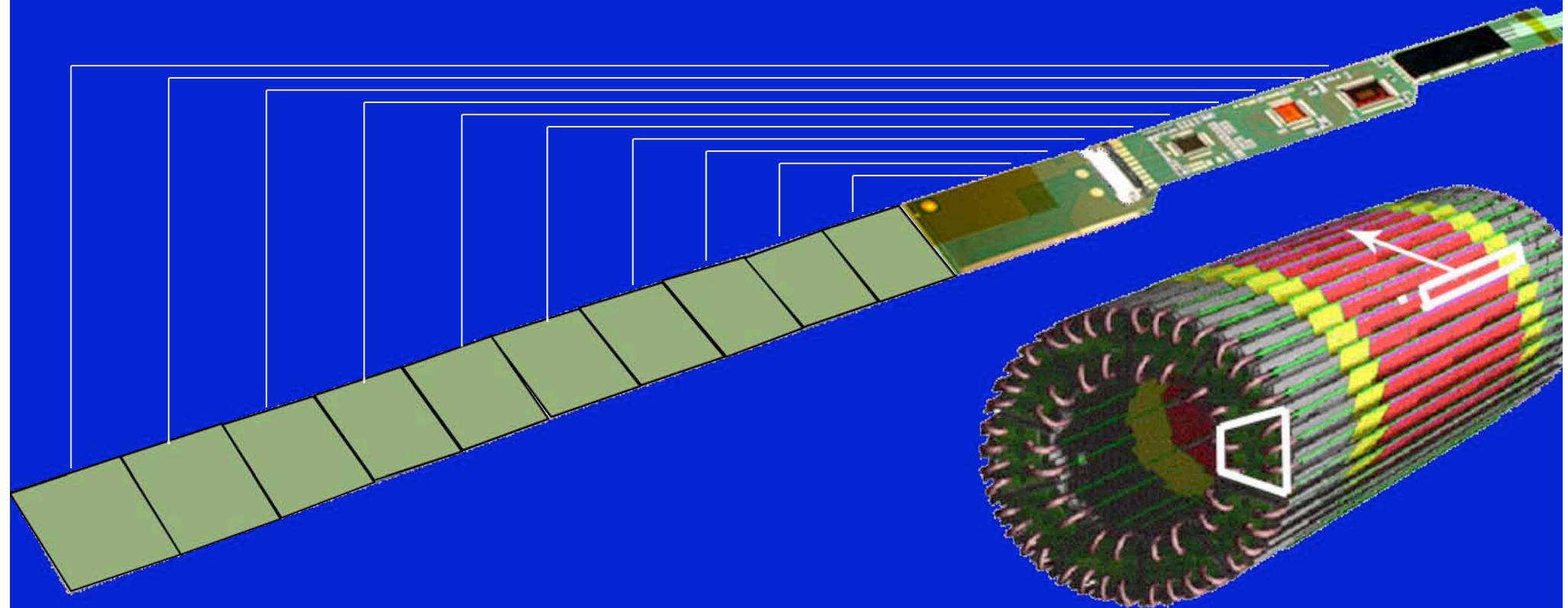


L0 pixel trigger

FastOr generation

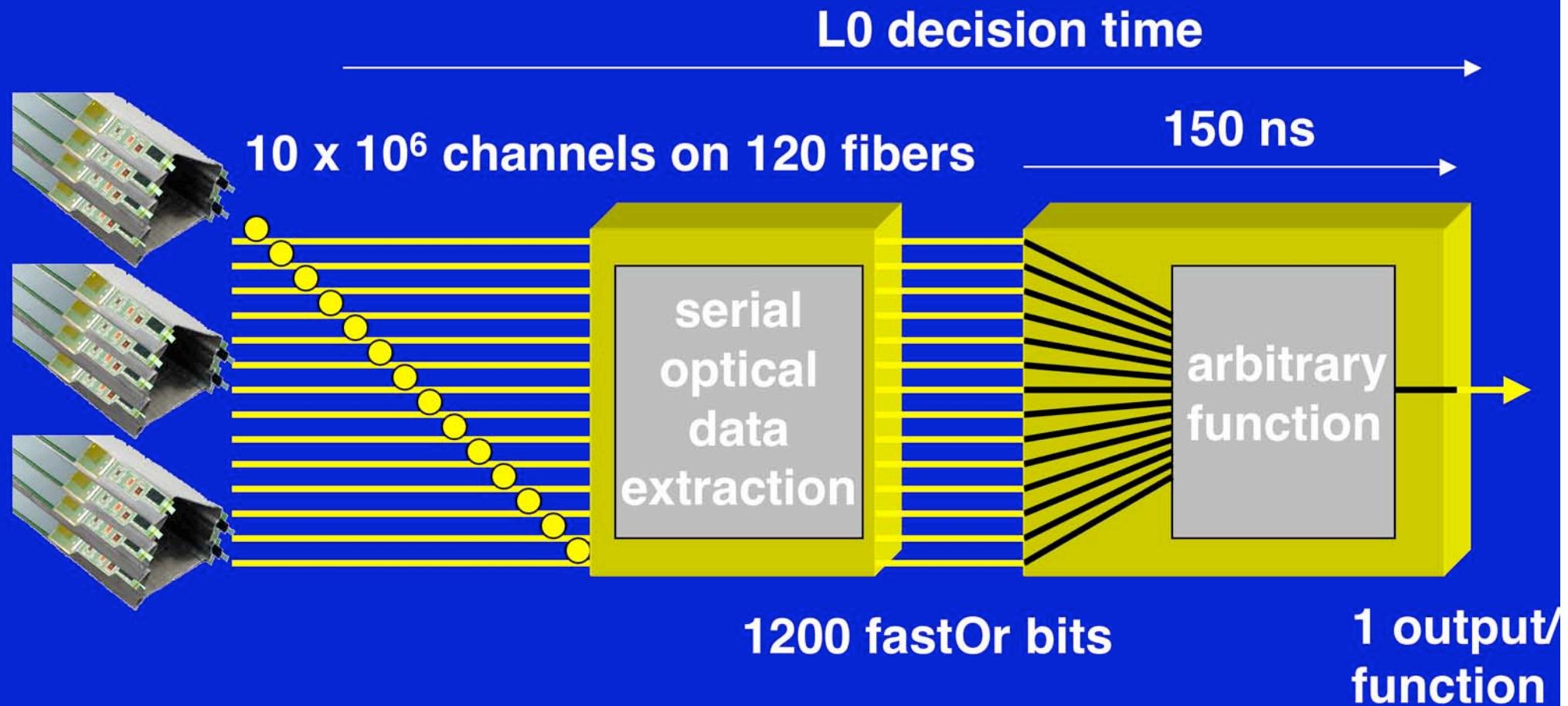


FastOr generation



**120 x half staves each 10 bit fastOr
= 1200 pads of (13 x 12 mm)**

Pixel trigger



PIT electronic boards

9U BRAIN board
Large I/O space FPGA,
1500 pins

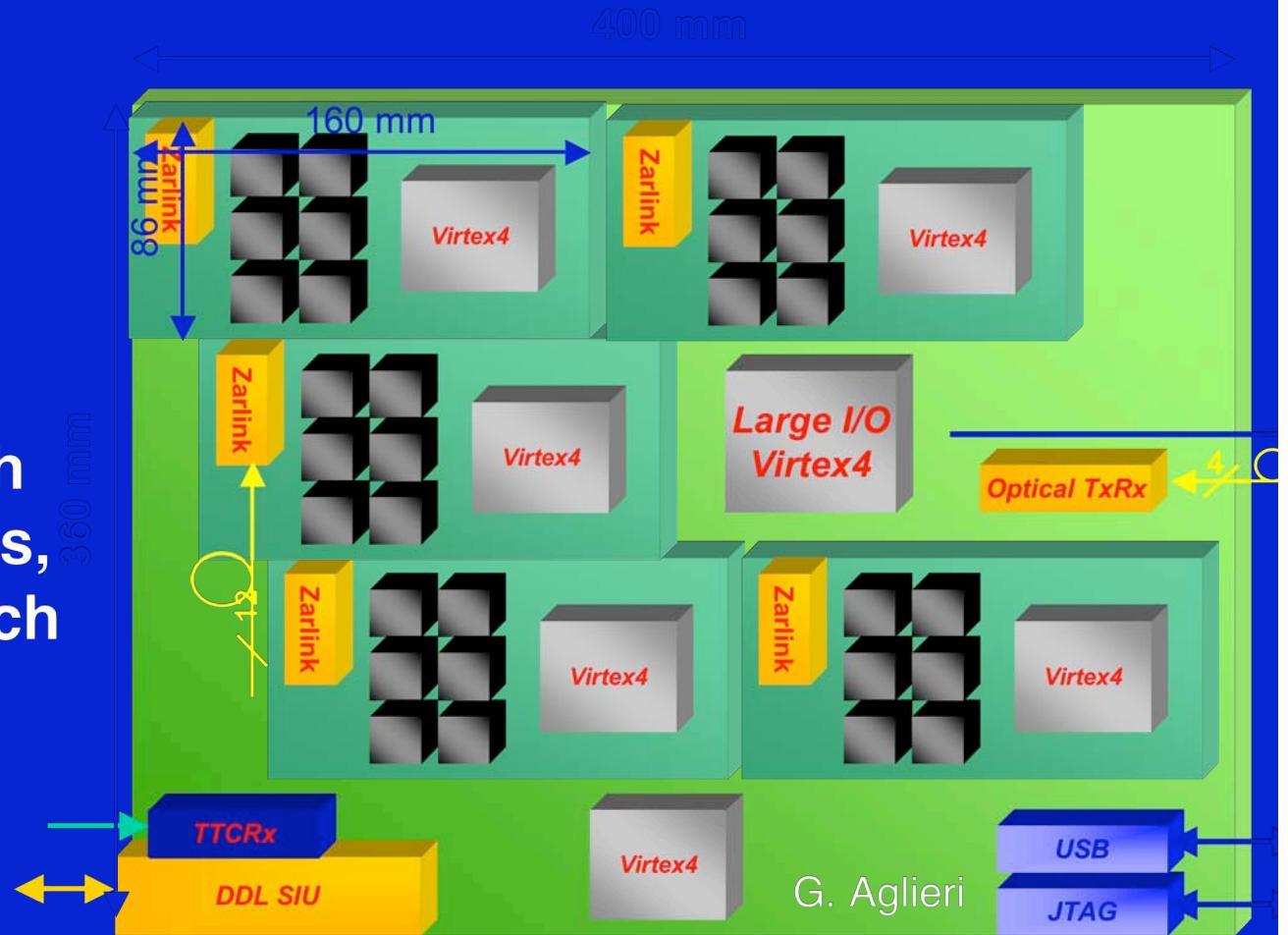
5 OPTIN boards on each
side as mezzanine cards,
serving 12 channels each



PIT electronic boards

9U BRAIN board
Large I/O space FPGA,
1500 pins

5 OPTIN boards on each
side as mezzanine cards,
serving 12 channels each

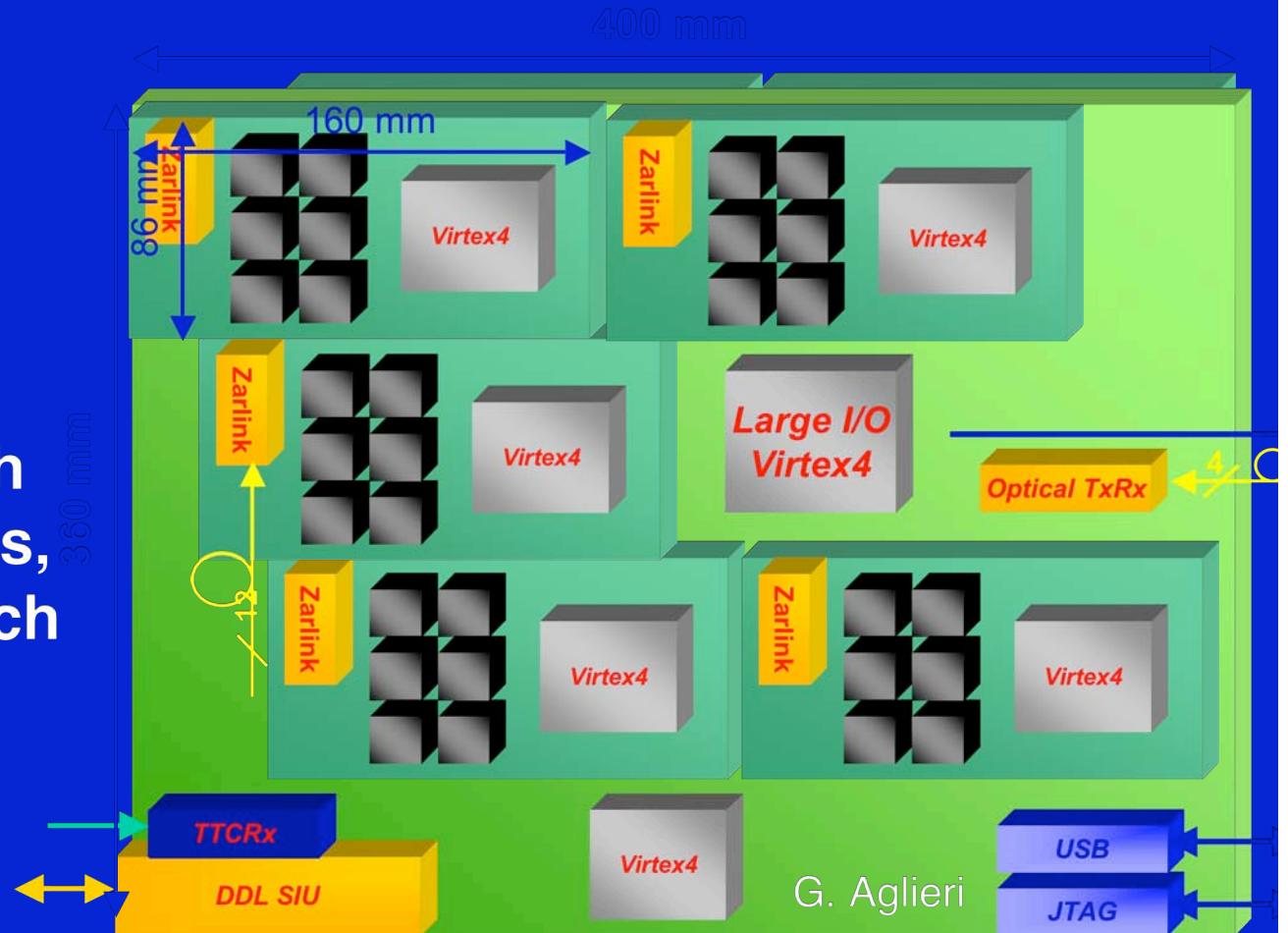


G. Aglieri

PIT electronic boards

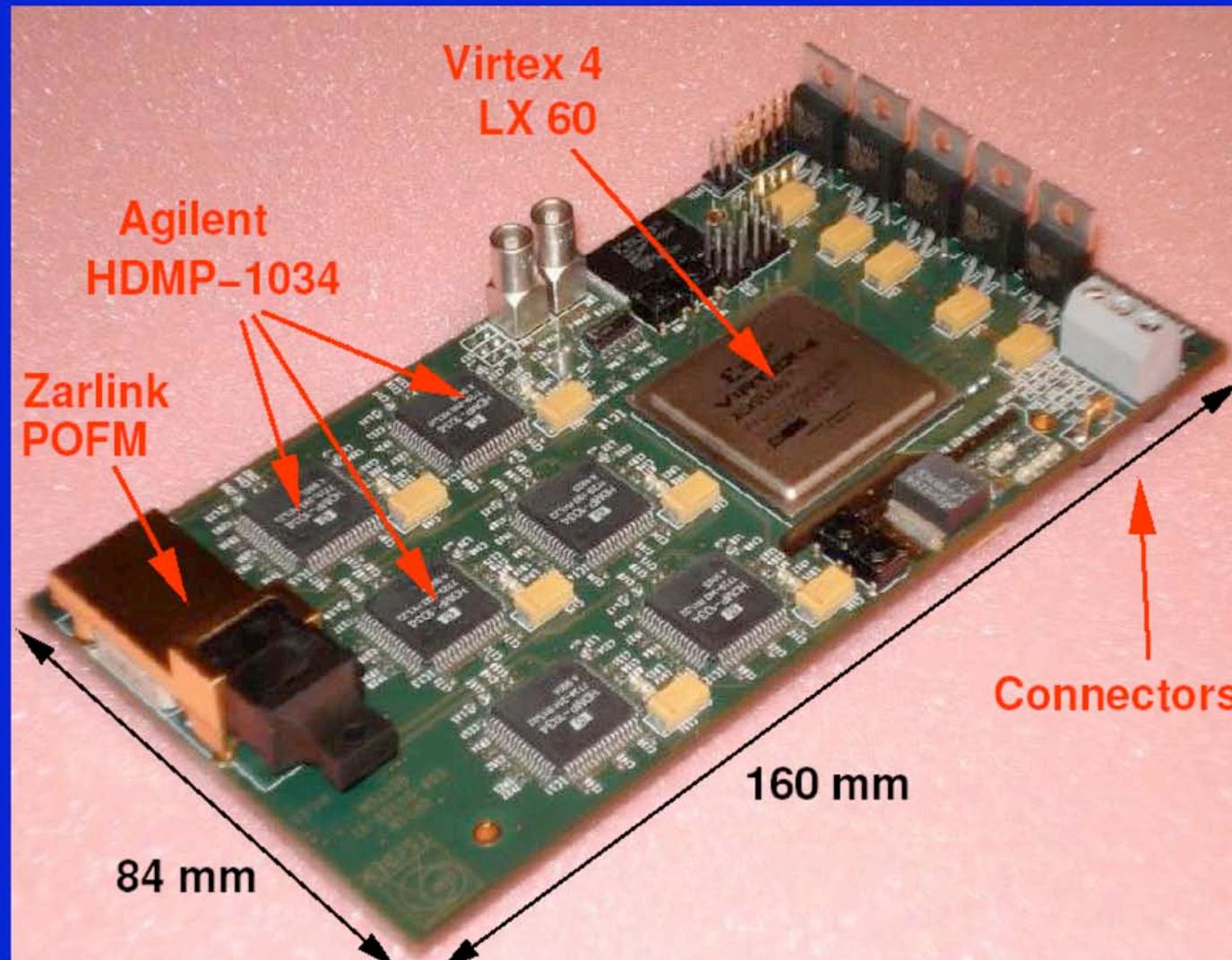
9U BRAIN board
Large I/O space FPGA,
1500 pins

5 OPTIN boards on each
side as mezzanine cards,
serving 12 channels each

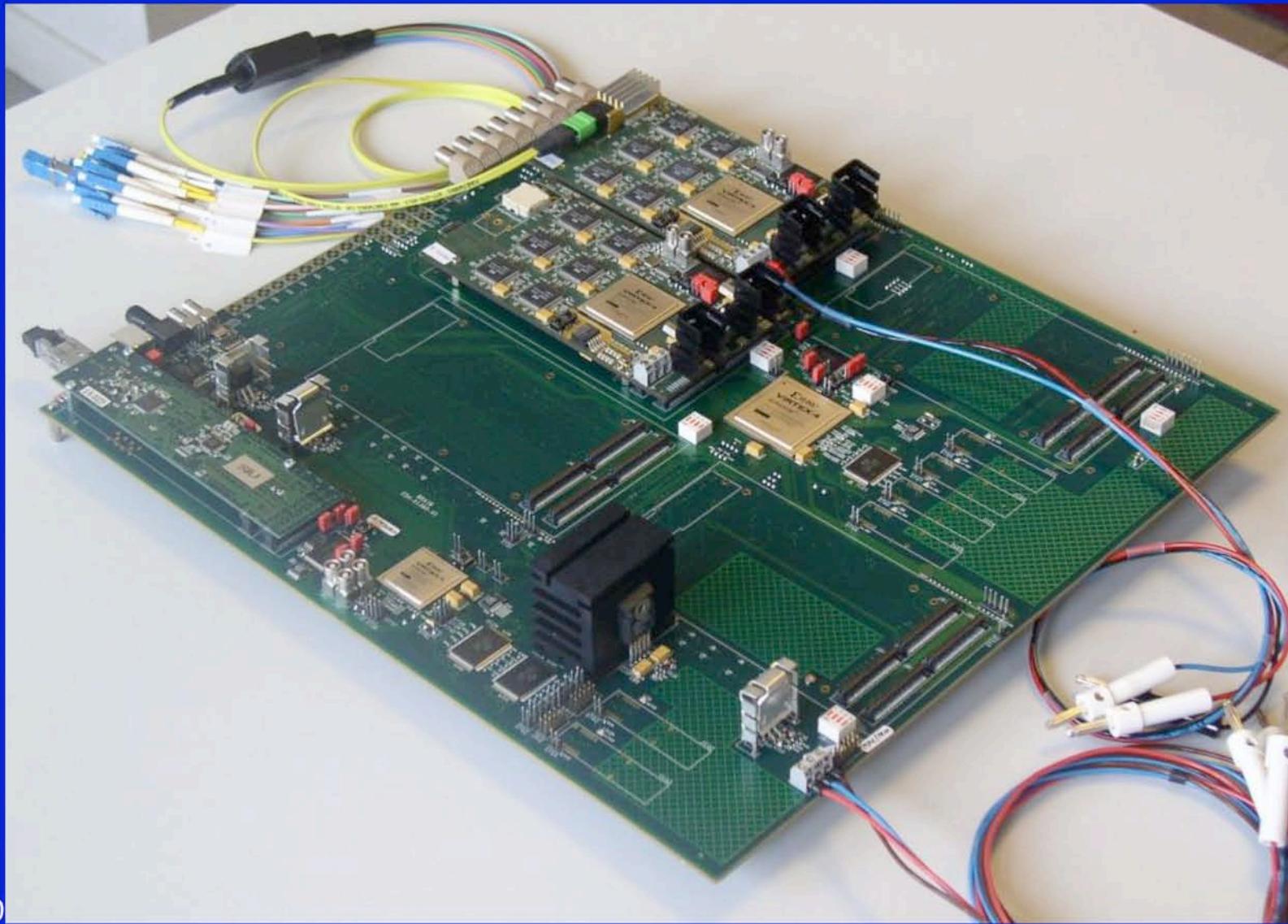


G. Aglieri

OPTIN receiver board



Brain - Processing board



Sept 3-7, 200

A. Kluge

SPD system Installation & Pre-Commissioning in the clean room

System and Detector Integration

ALICE SPD detector

ALICE SPD DCS & DAQ

ALICE SPD trigger interface

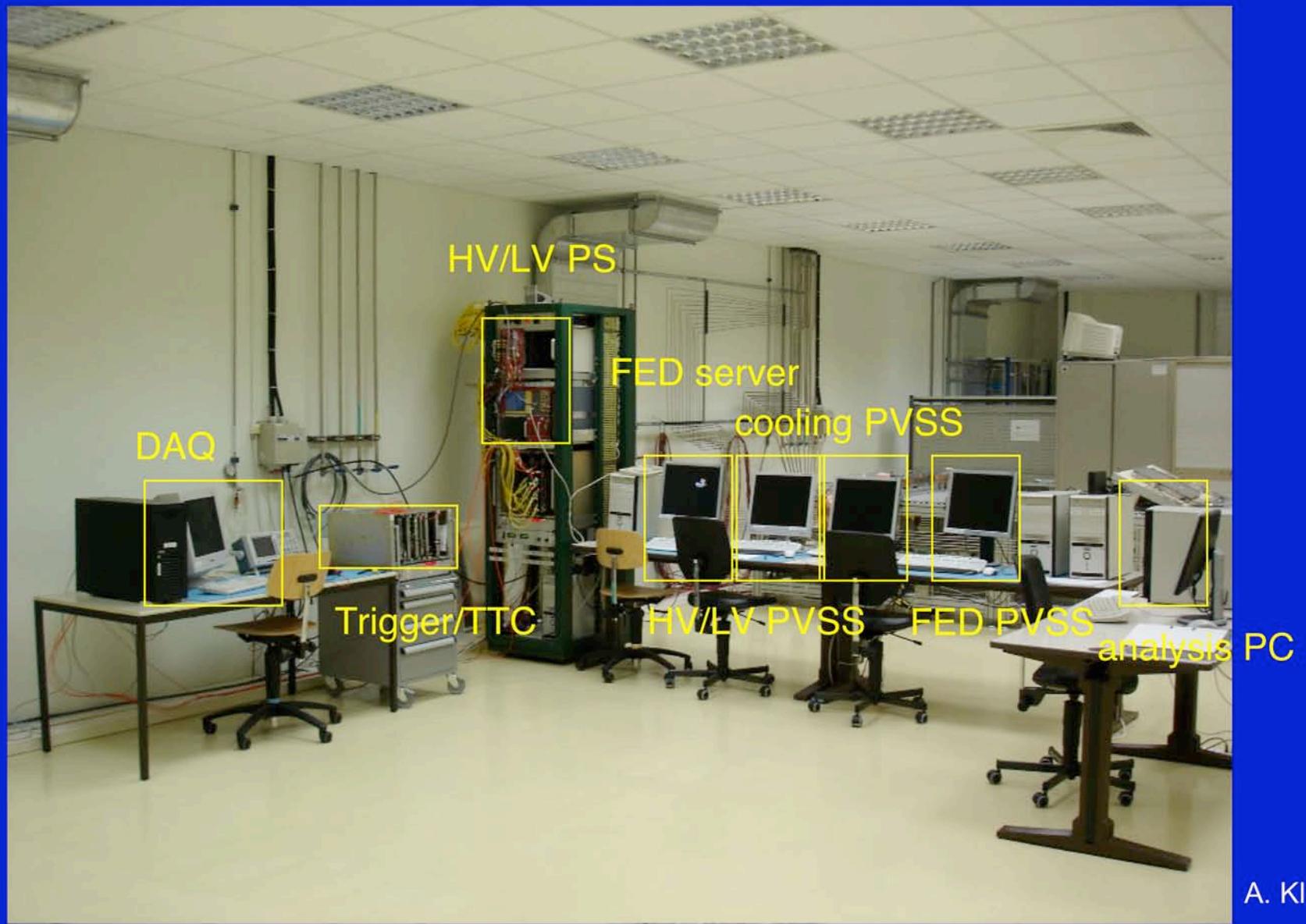
ALICE SPD LV & HV system

ALICE SPD cooling

ALICE SPD cabling & patch panels



System and Detector Integration





Sab



Sept 3-7, 2007

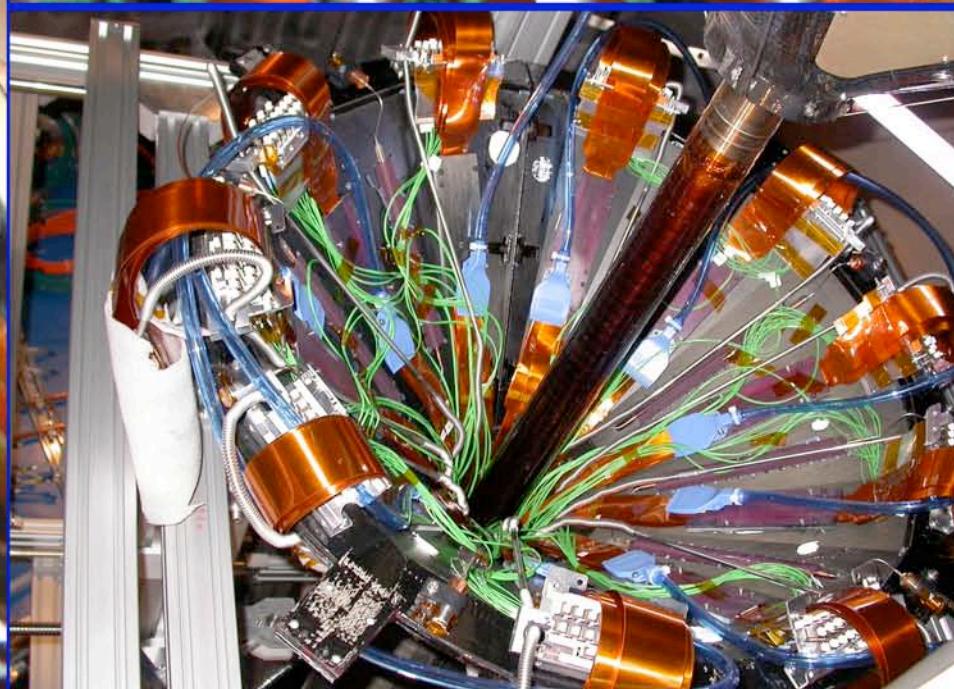
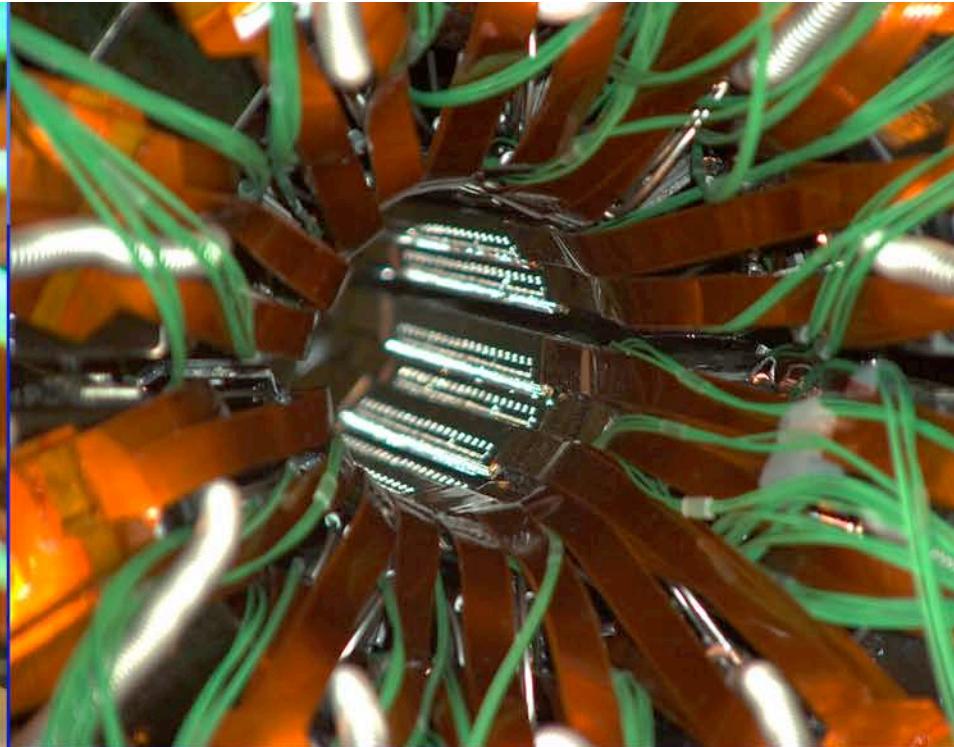
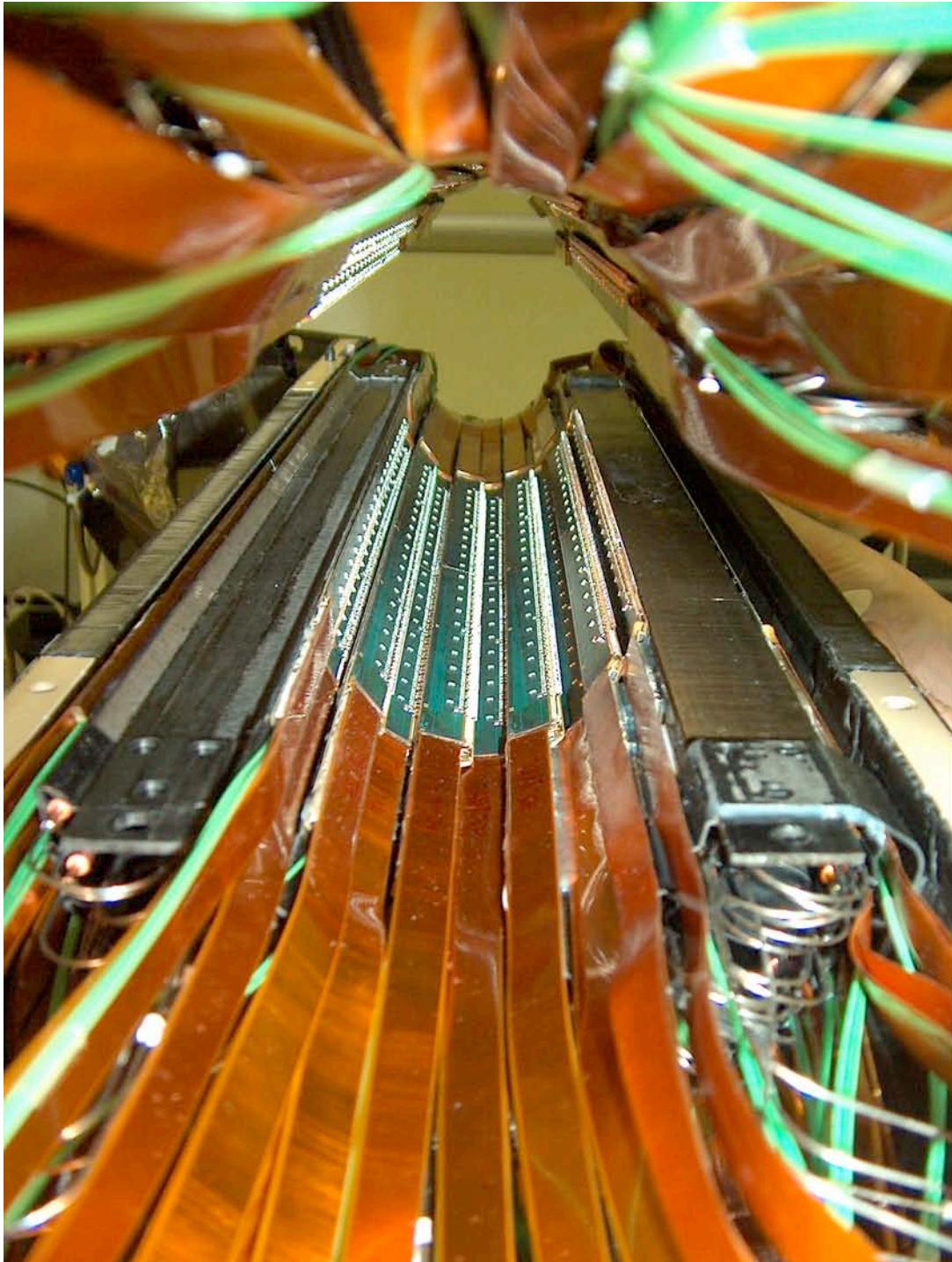
A. Kluge

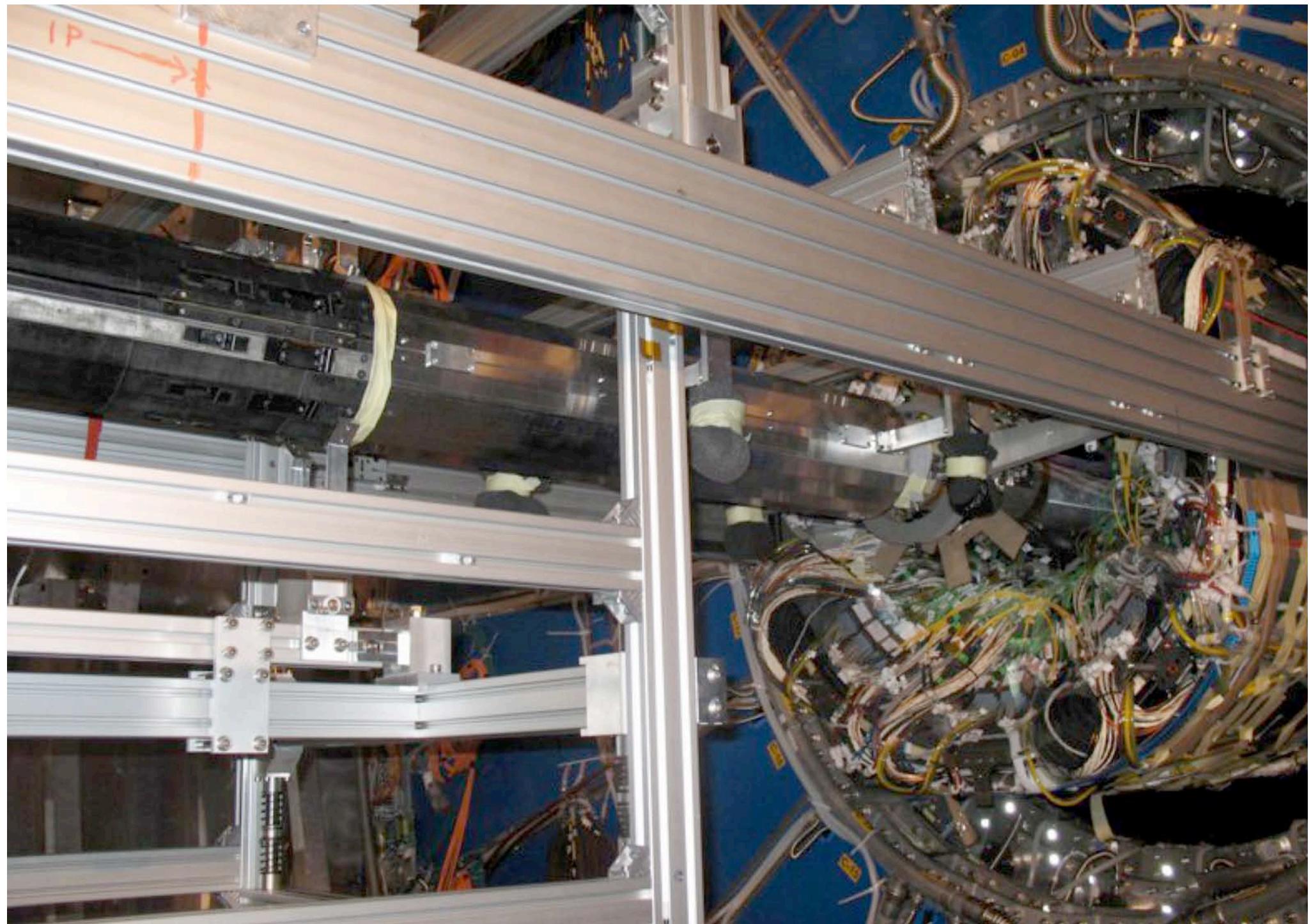


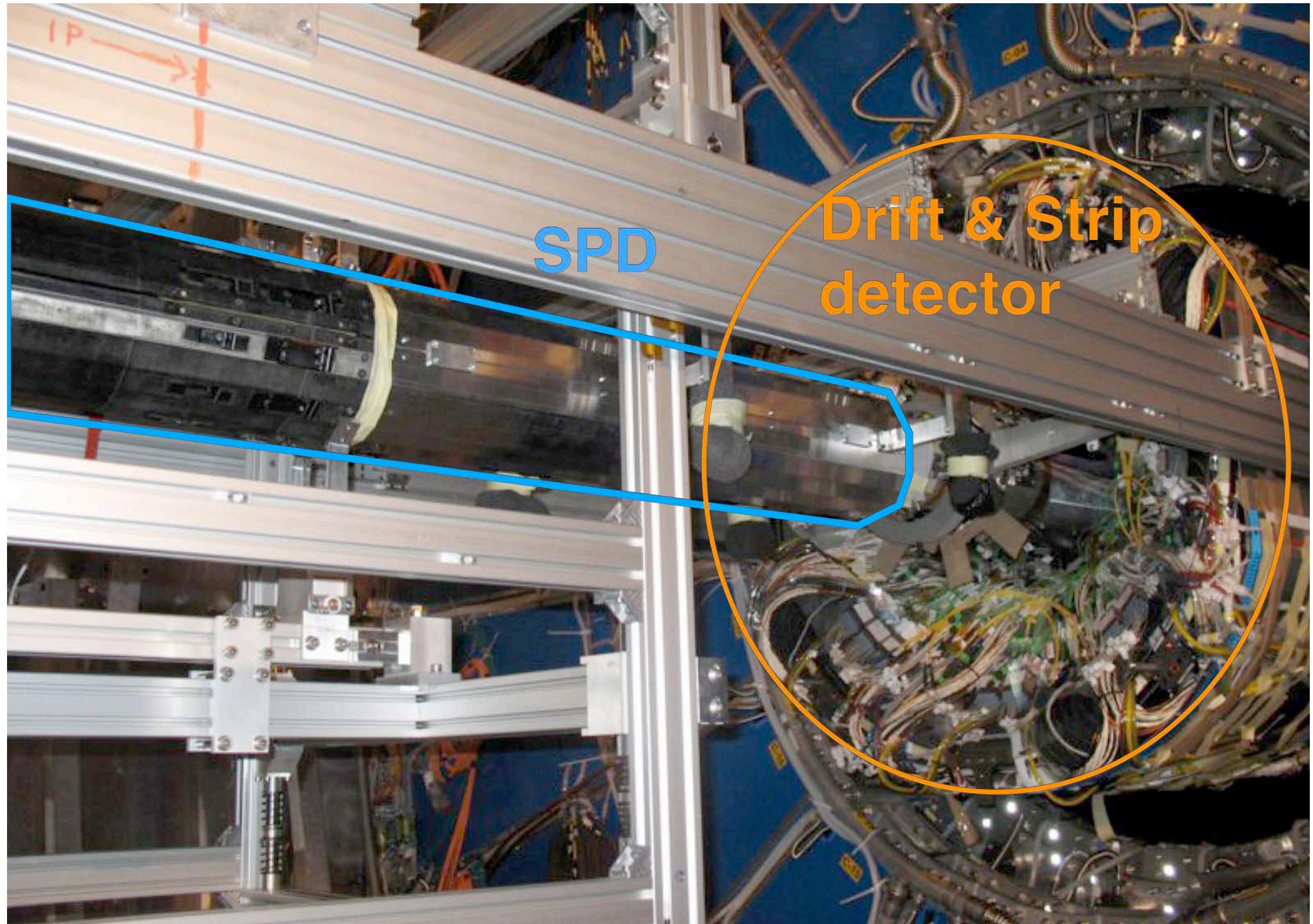
Sept 3-7, 2007

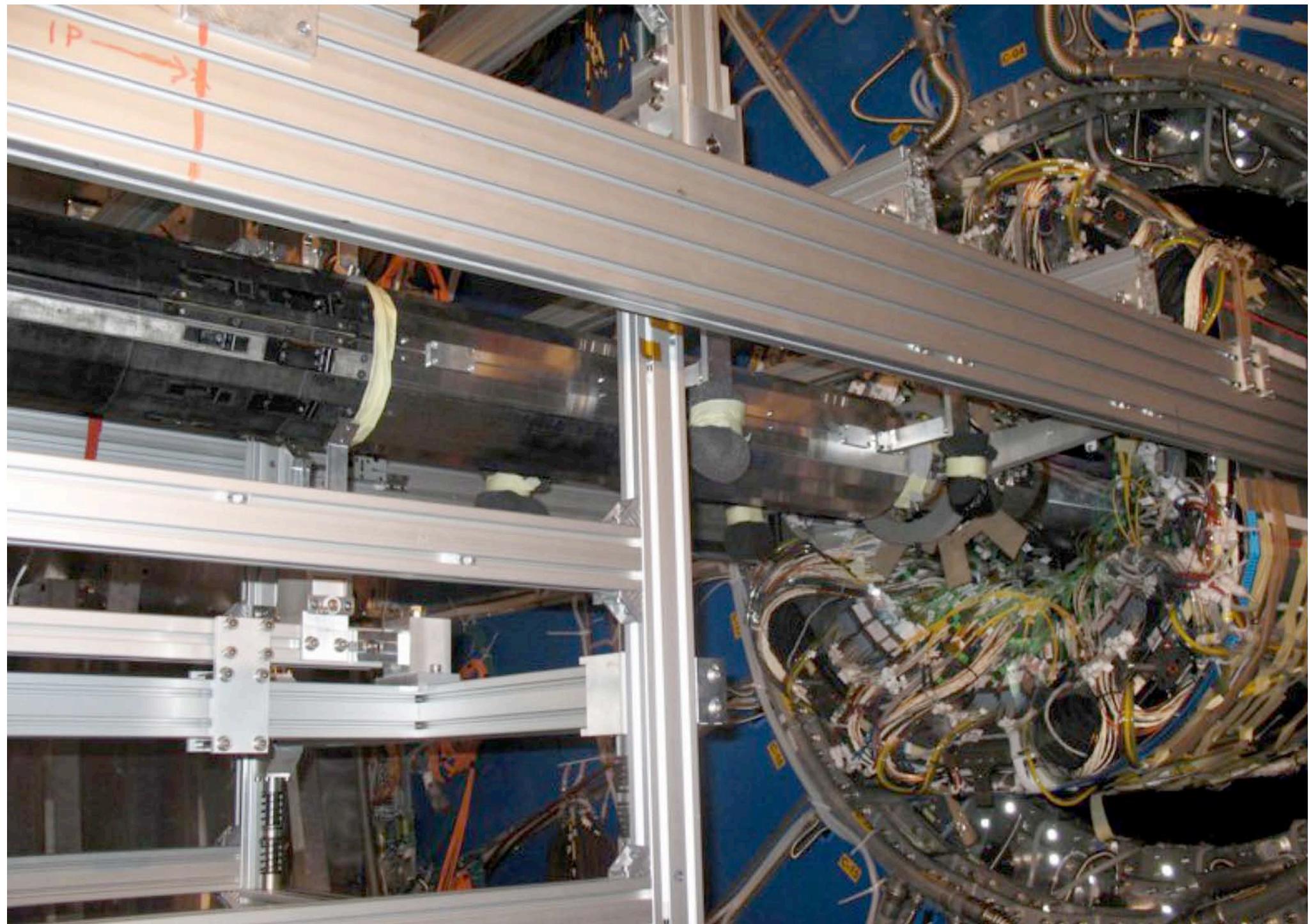
A. Kluge

SPD installation









Sept 3-7, 2007

A. Kluge

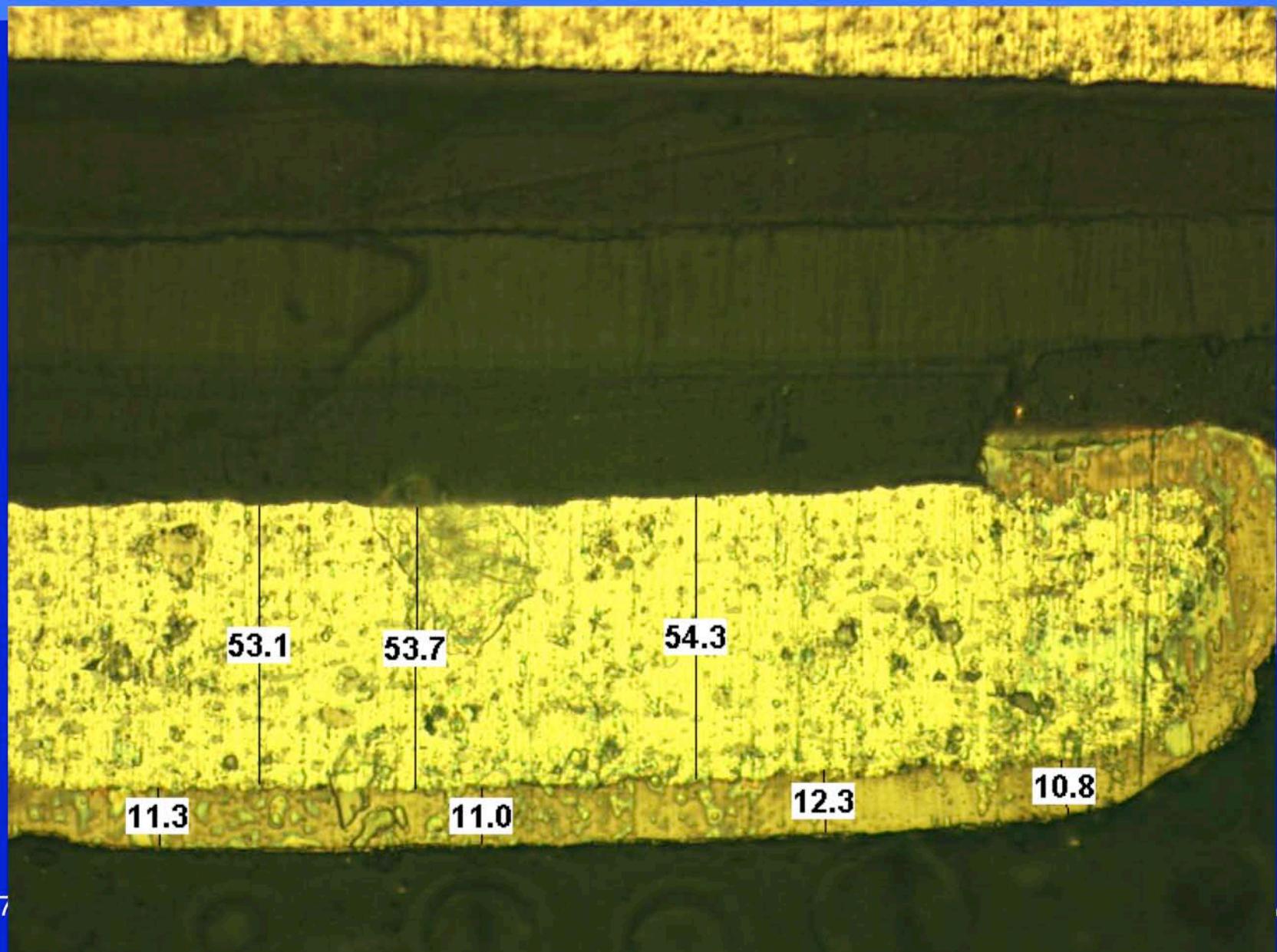
Conclusion

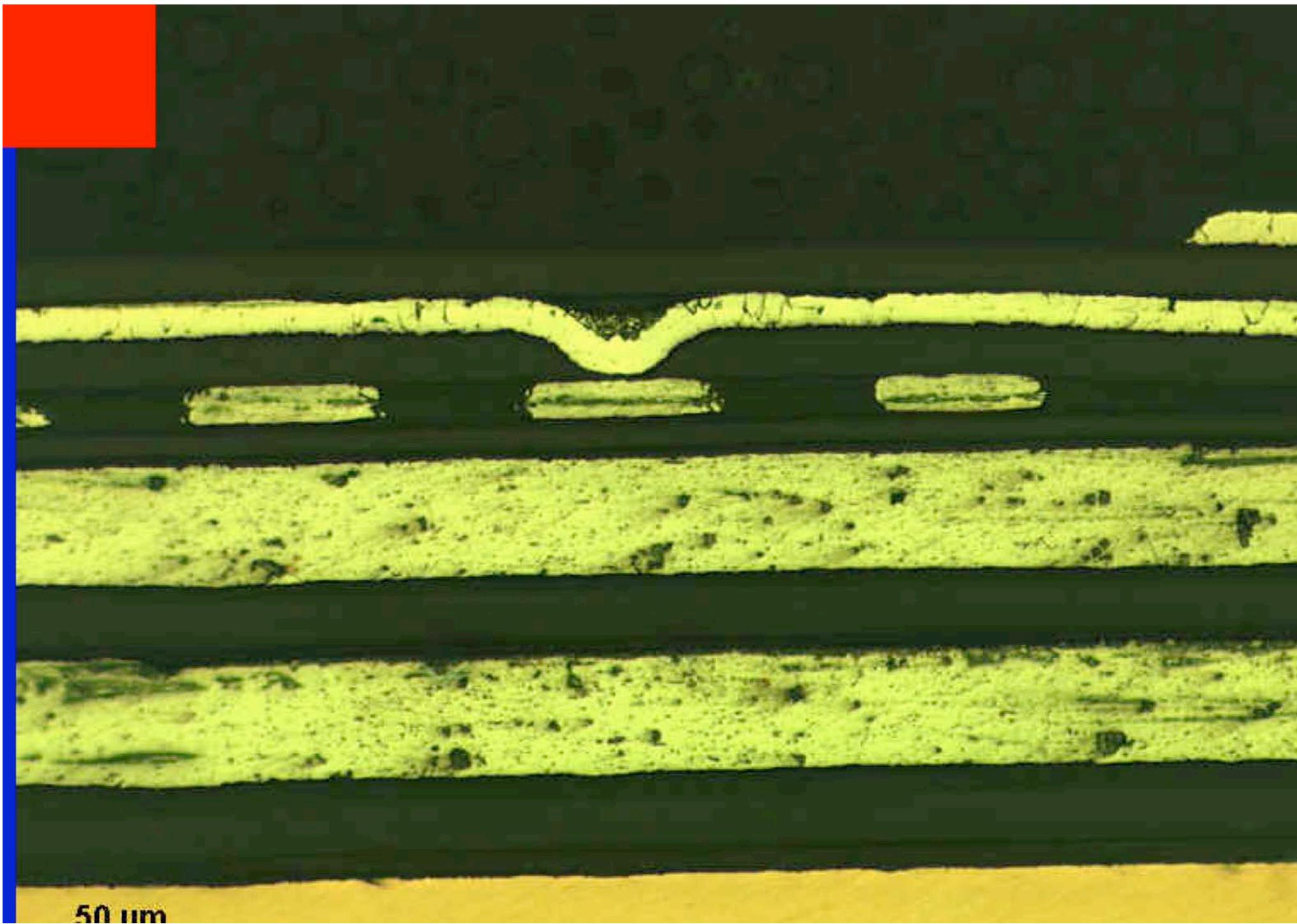
- SPD has been installed in ALICE
- SPD system has been pre-commissioned in clean room



Additional slides

The pixel bus

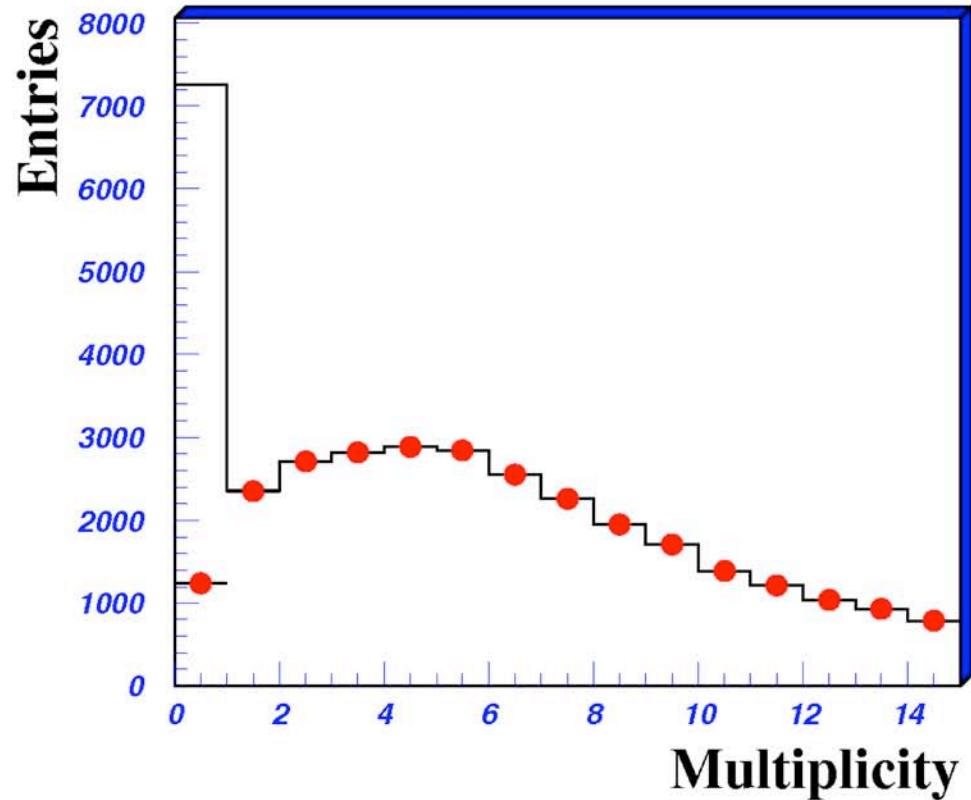




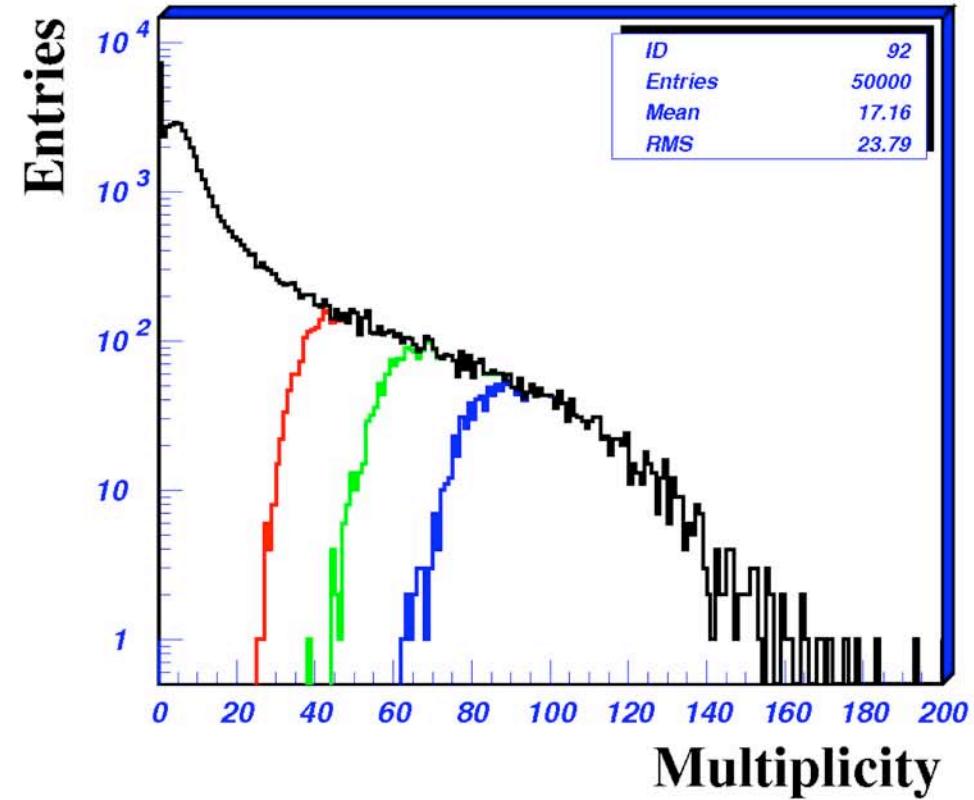
50 μm

Pixel trigger

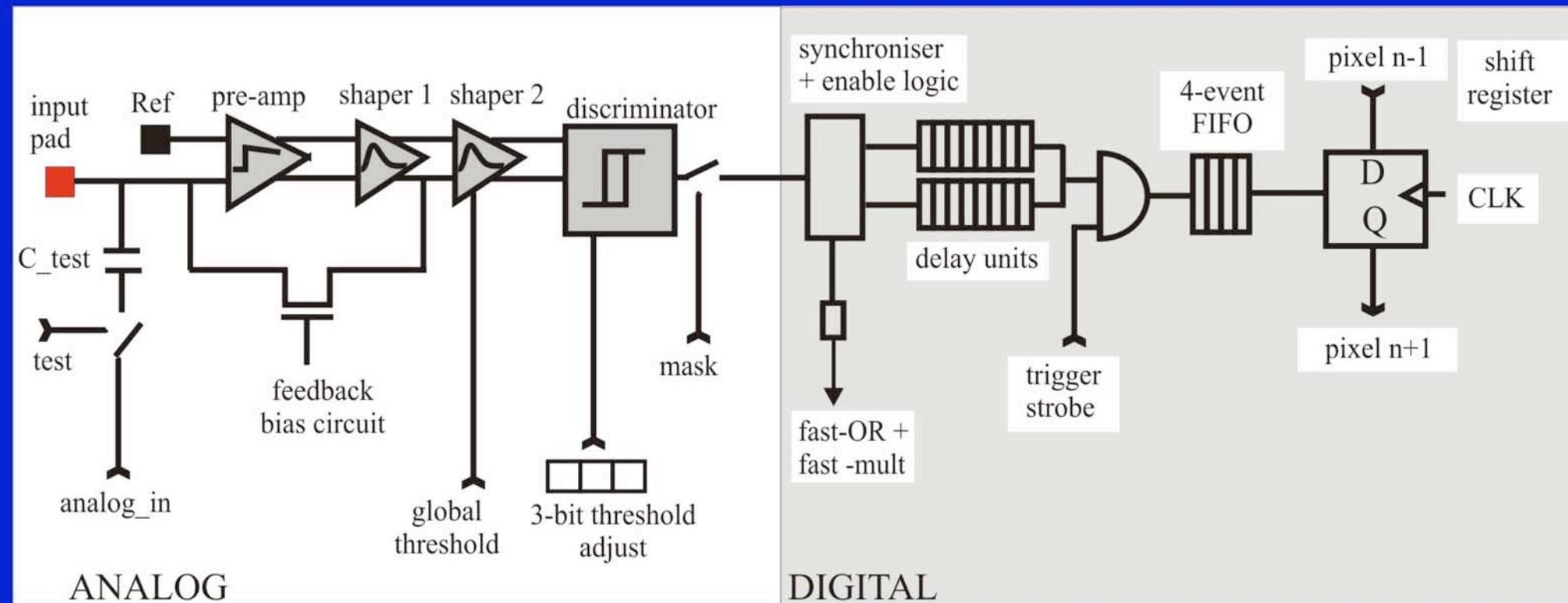
Minimum bias



Multiplicity



Pixel chip



Detect
SPD

Infrastructure & Cabling

RB26
C side

RB24
A side

2514 connections
bundled in 1899
cables



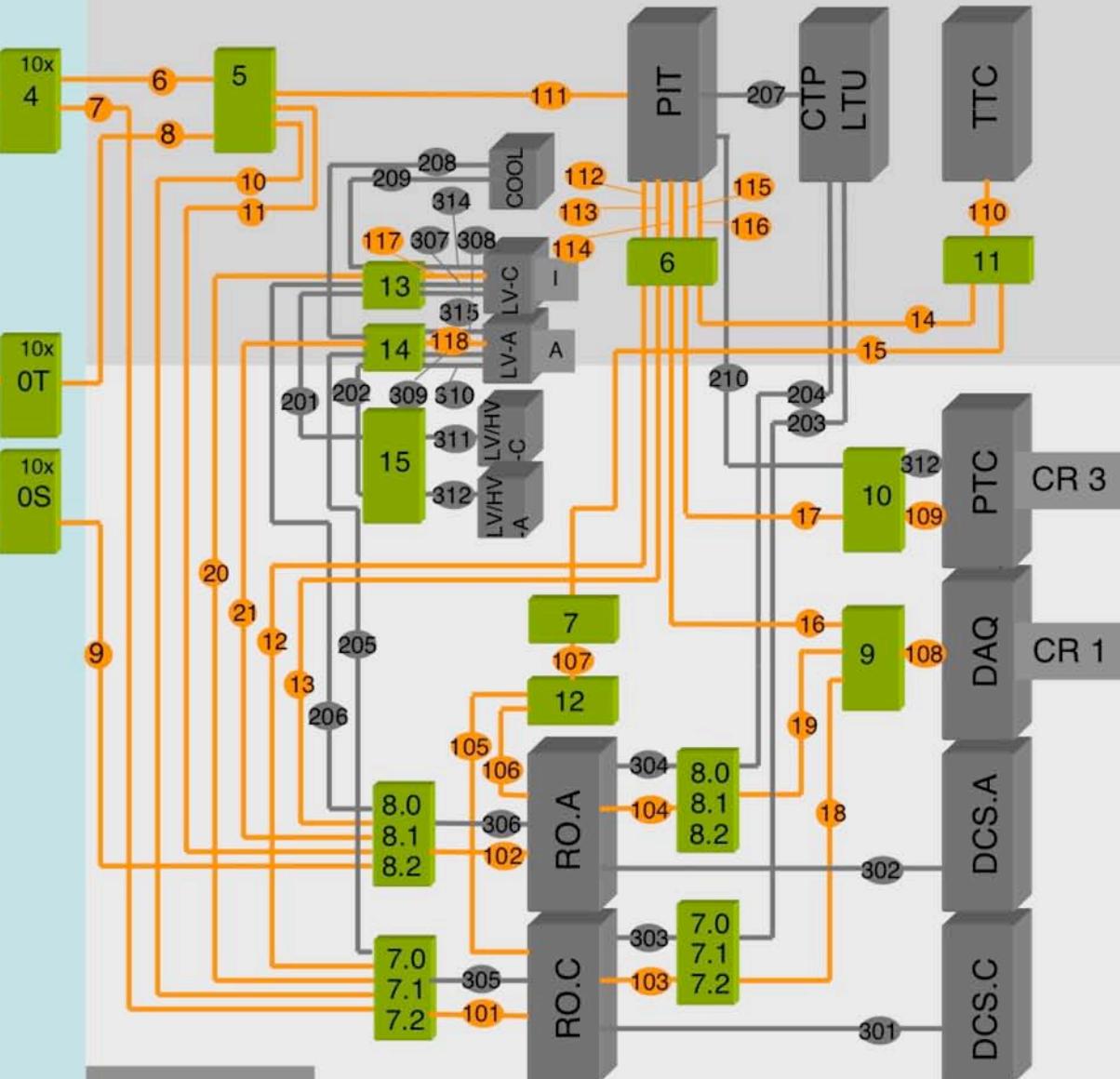
optical

patch panel

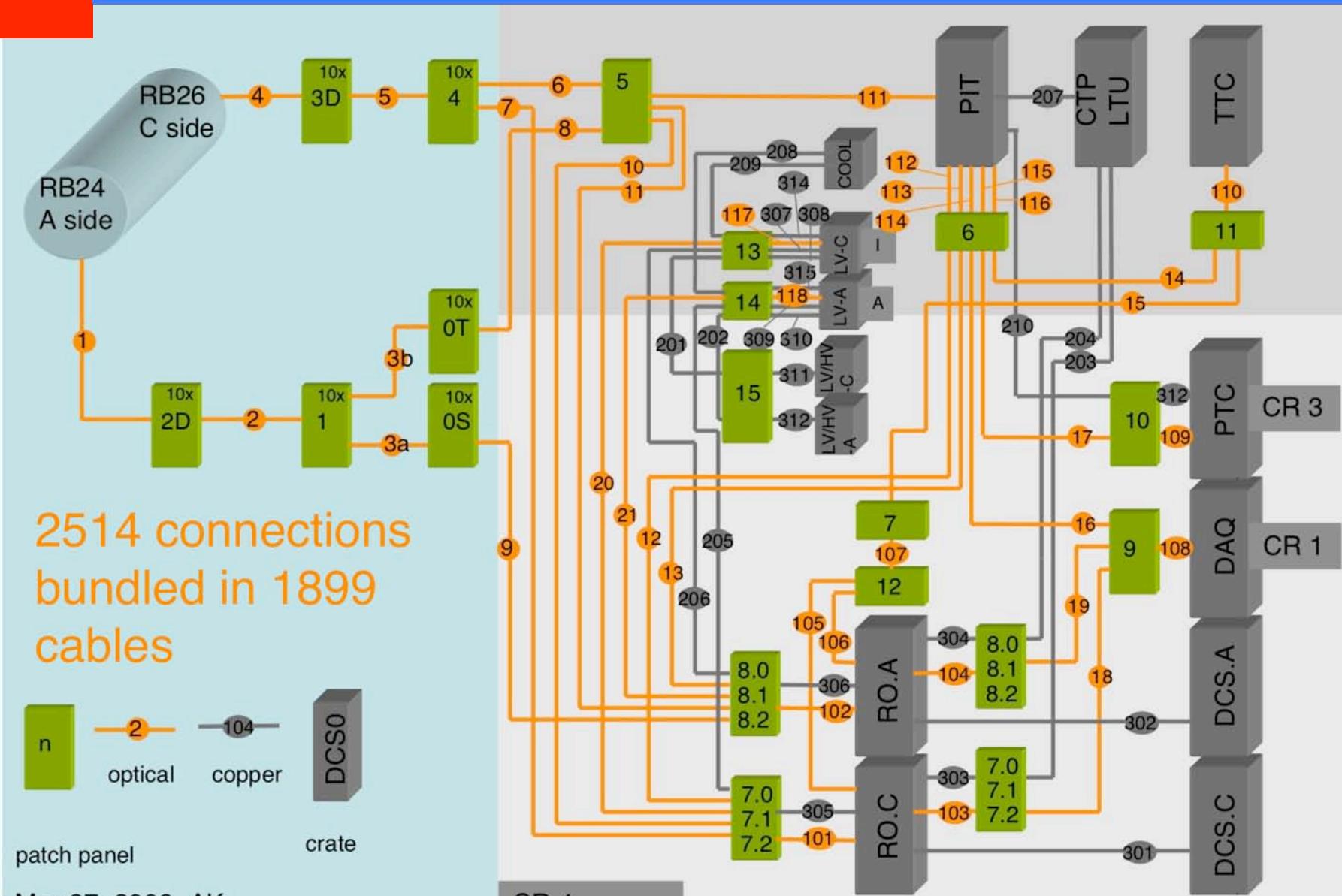


copper

crate



Infrastructure & Cabling



2514 connections
bundled in 1899
cables

patch panel

2 optical ————— 104 copper

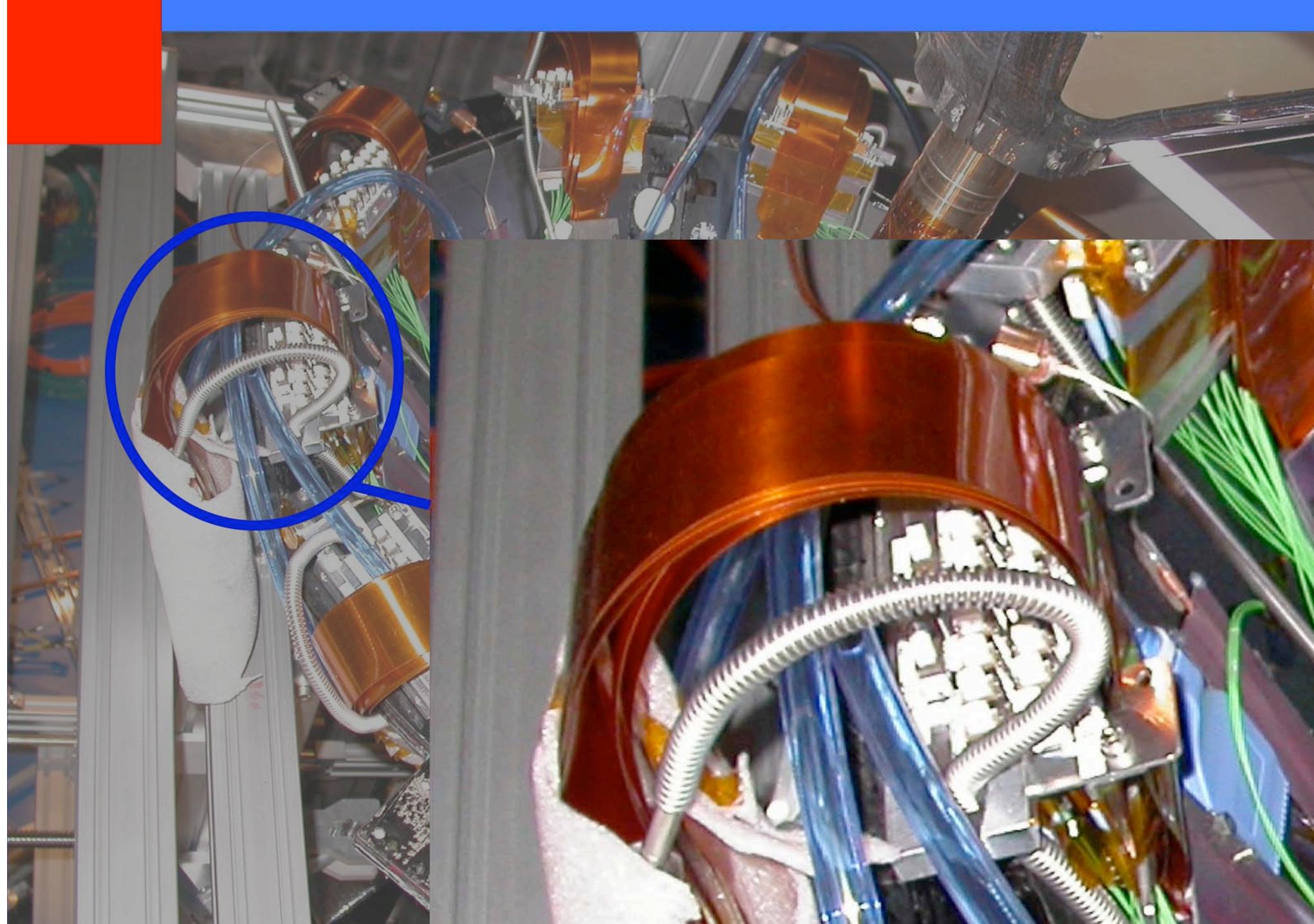
DCSO

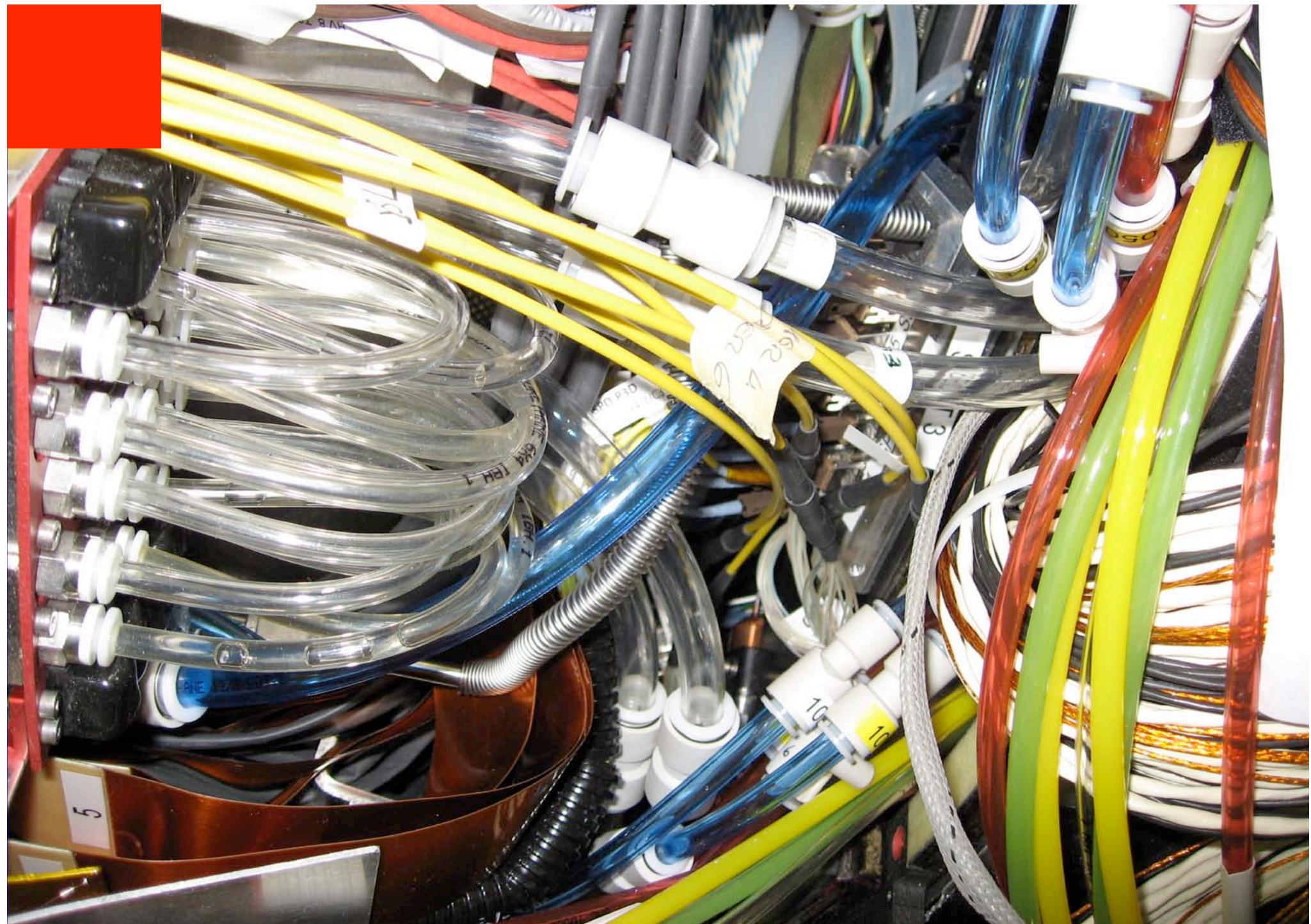
Sept 3 Mar.27, 2006, AK

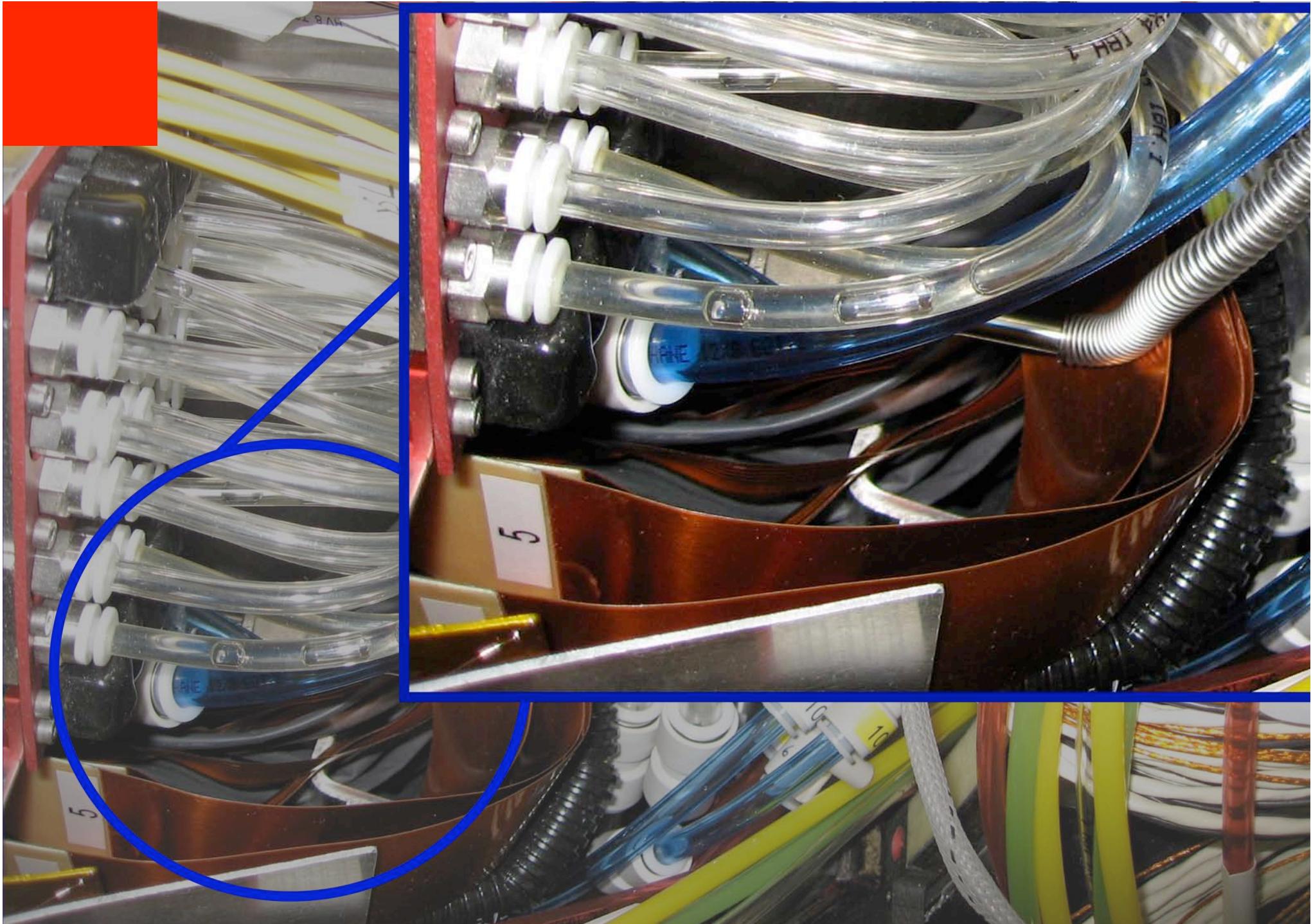
CR 4

uge











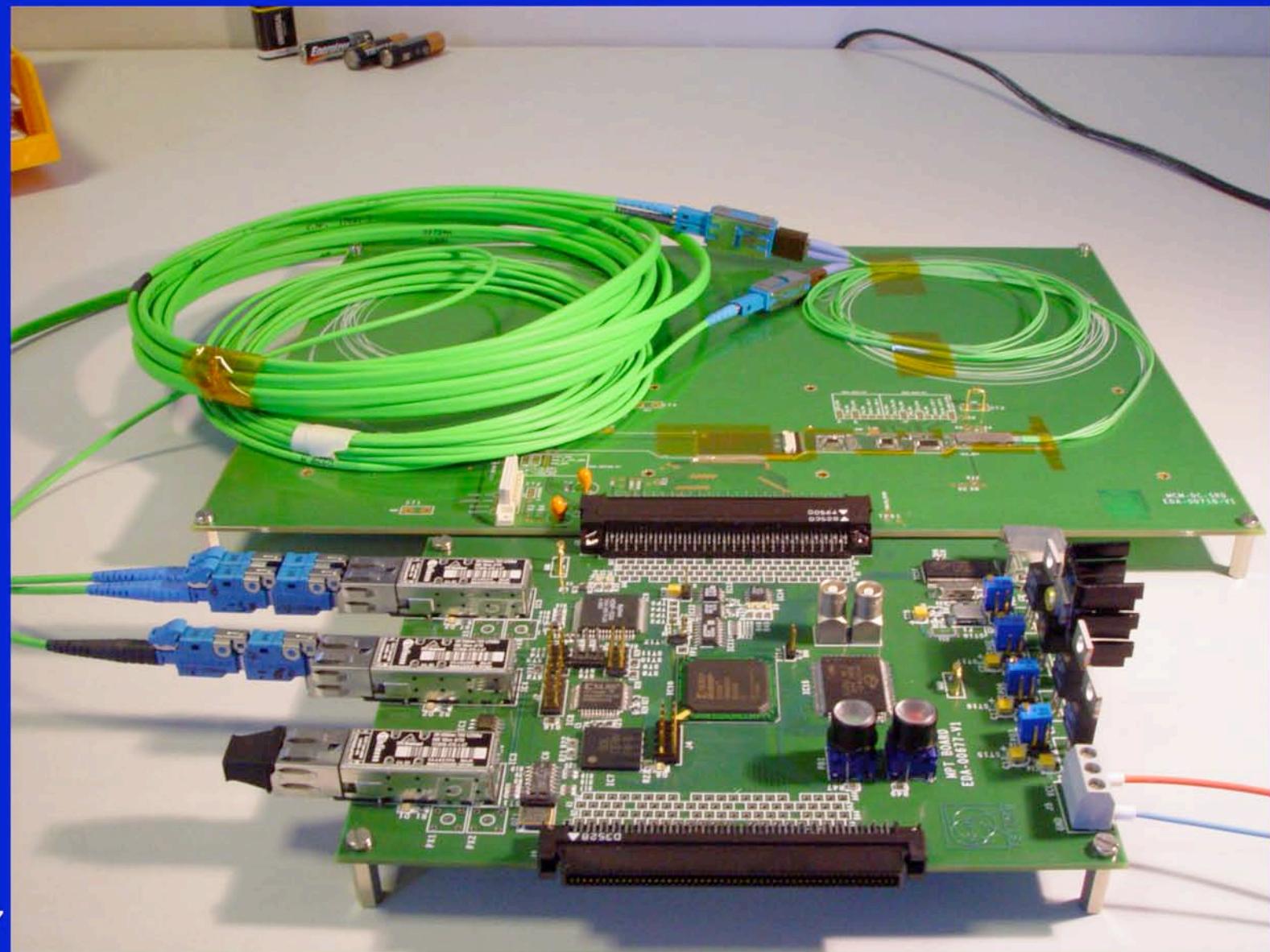


Sab



Total number of ladders tested: 439
Class 1 ladders: 79 %
Failure modes:
Leakage current > 2 μ A: 13 %
Bump bonding > 82 missing: 5 %
Chip errors: 3 %

MCM



Sept 3-7, 2007

A. Kluge



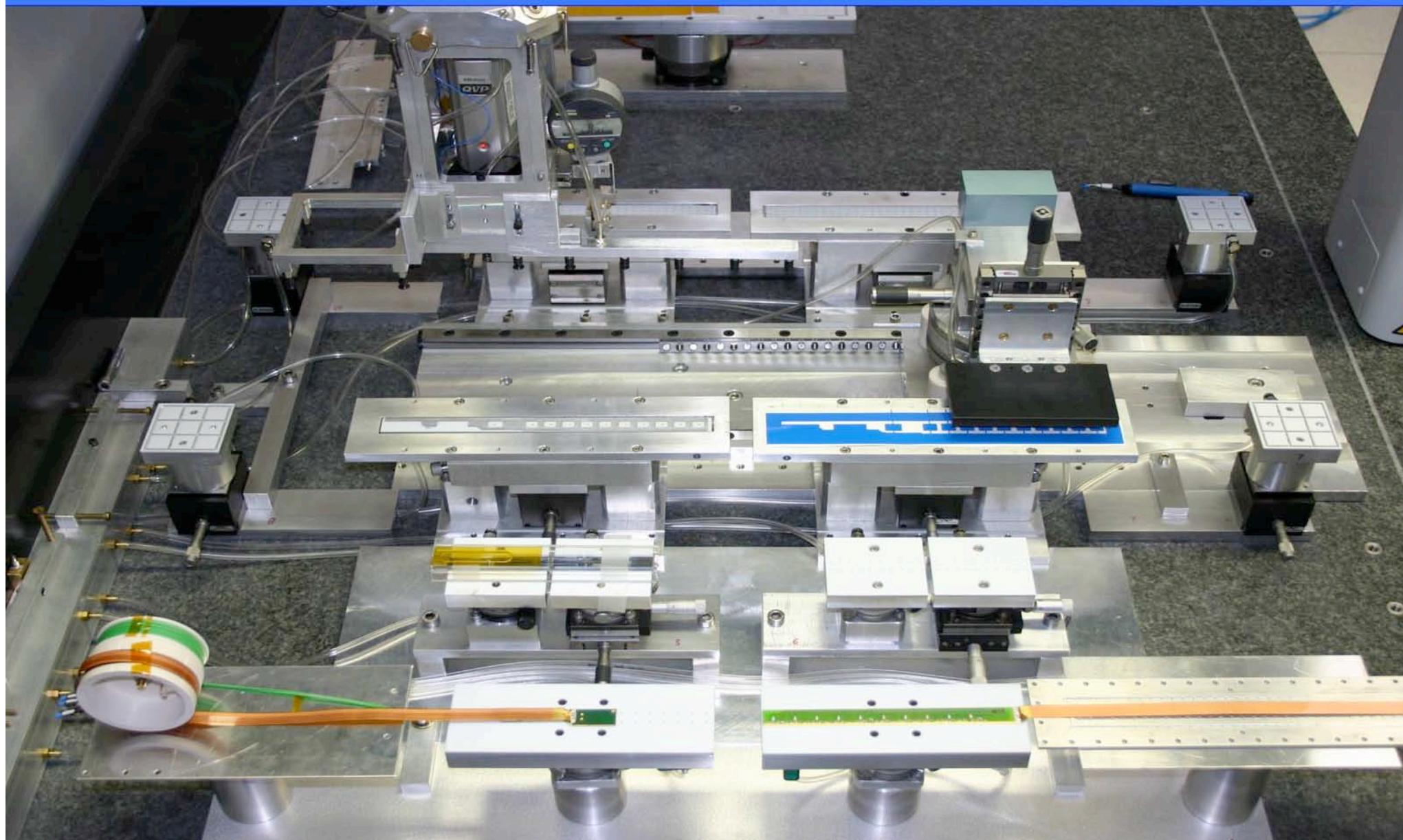
Sept 3-7, 2007

Saba

A. Kluge

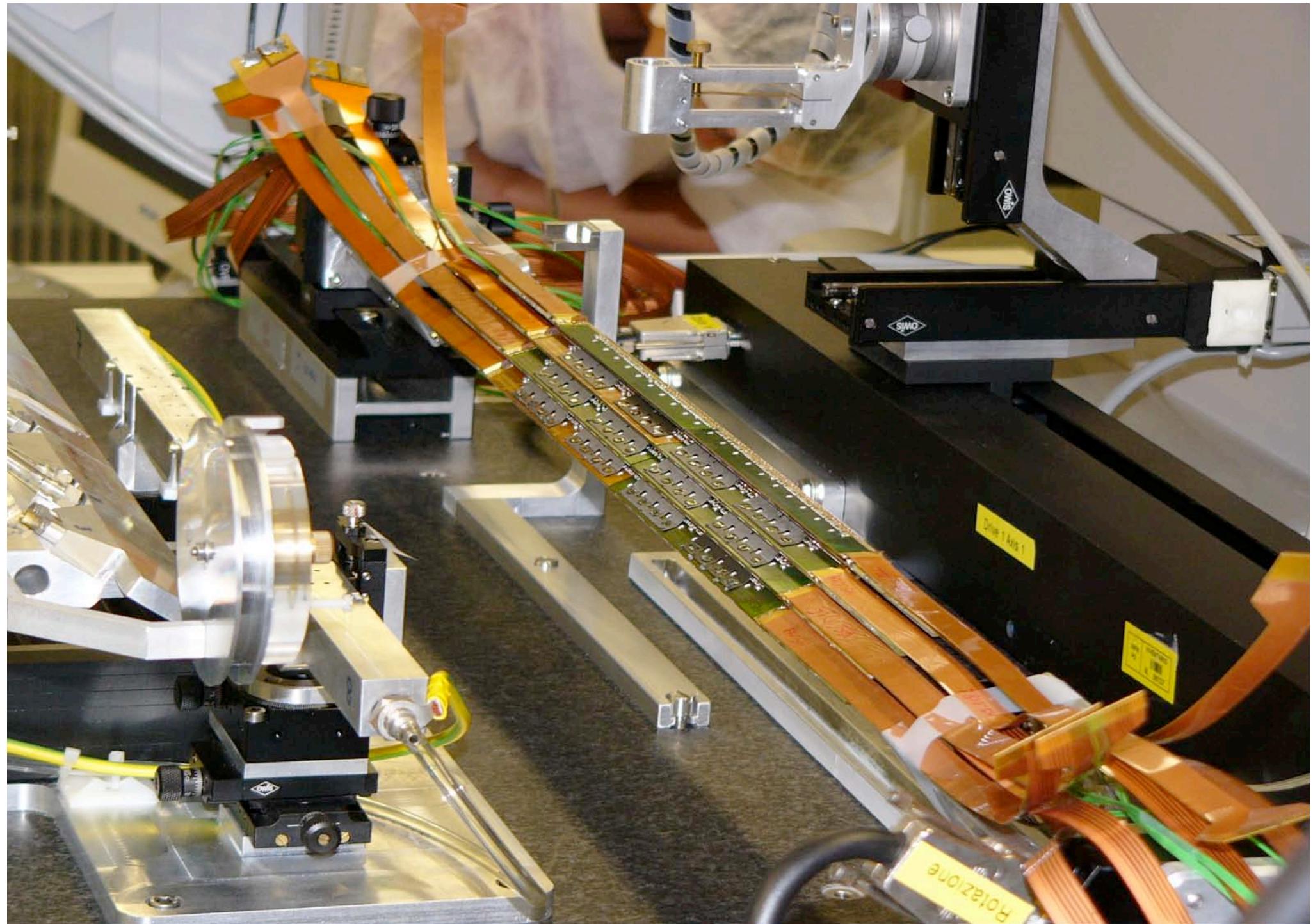
Half stave & sector assembly

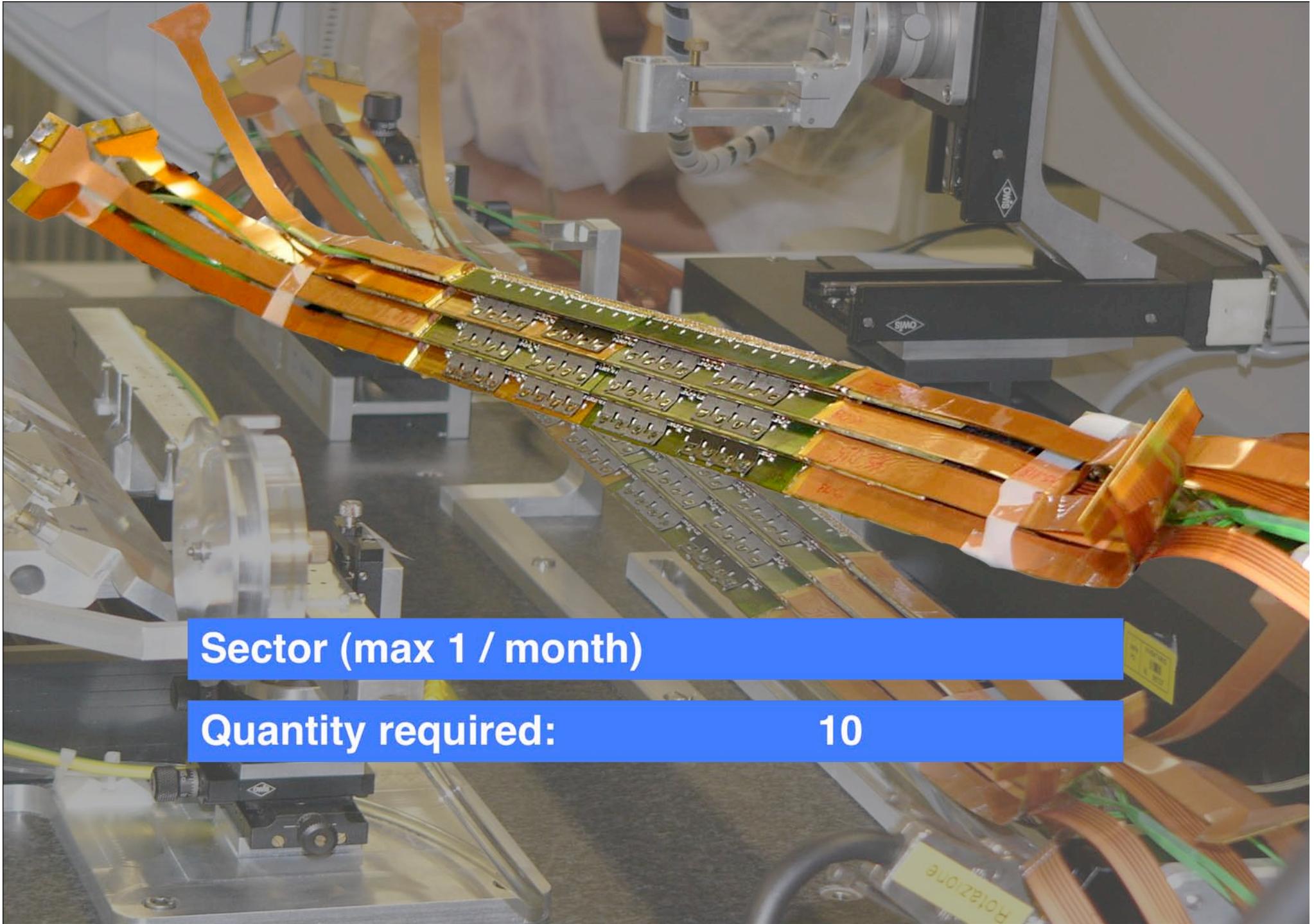
Half stave assembly station



Half stave assembly station

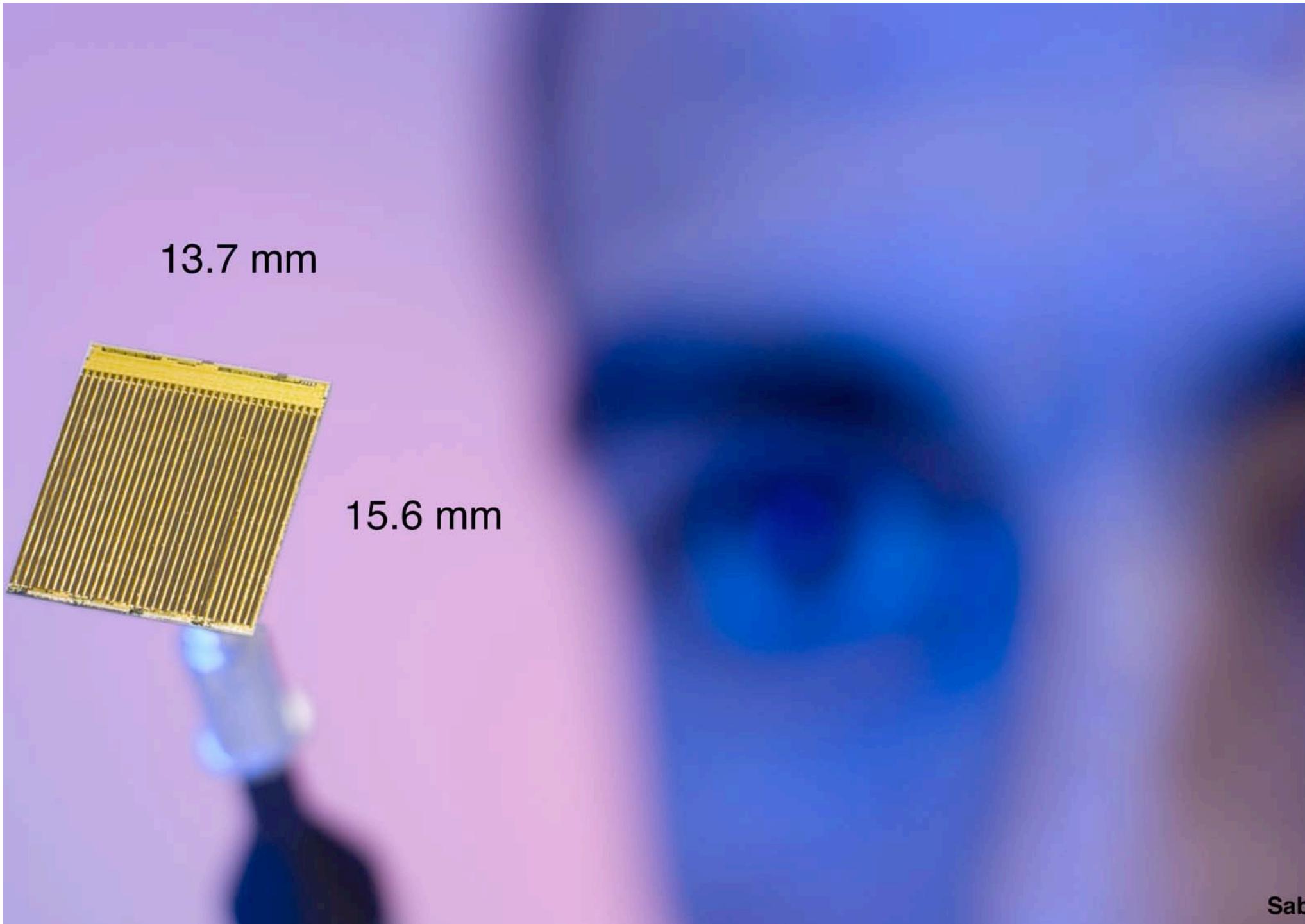






Sector (max 1 / month)

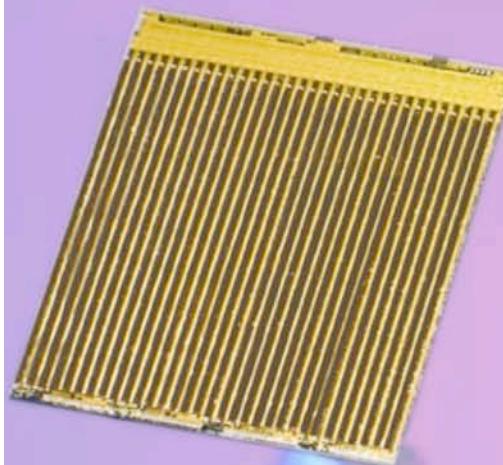
Quantity required: 10



13.7 mm

15.6 mm

Sab



13.7 mm

15.6 mm

pixel size $425\mu\text{m} \times 50 \mu\text{m}$

pixel matrix $256 \times 32 = 8192$

differential front end

150 e⁻ noise, $100\mu\text{W}/\text{pixel}$

binary synchronous read-out

read-out on 32 bit parallel bus @ 10 MHz

configuration loading via JTAG

I/O with GTL logic

**5 bit reg./pixel &
42 DACs for configuration**

external analog bias inputs