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The ALICE Silicon Pixel Detector system

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The ALICE silicon pixel detector (SPD) comprises the two innermost layers of the ALICE inner tracker system. The
SPD includes 120 half staves each consisting of 10 ALICE pixel chips bump bonded to two silicon sensors and one
multi-chip read-out module. Each pixel chip contains 8,192 active cells, so that the total number of pixel cells in the
SPD is ≈ 10^7. The on-detector read-out is based on a multi-chip-module containing 4 ASICs and an optical transceiver module. The constraints on material budget detector module dimensions are very demanding. An overview of the electronics integration, test results and test procedures are presented.

Summary

1. SPD layout The ALICE silicon pixel detector (SPD) consists of two barrel layers at radii of 3.9cm and 7.6cm, respectively. The basic detector module is the half-stave, in which the active elements are two ladders glued to a multi-layer Al flexible flat cable carrying power and signal lines. Each half-stave consists of 10 pixel chips bump bonded to two silicon pixel sensors (70.7 x 16.8 mm2) and is read out by a multi-chip module. Each pixel chip contains a matrix of 8192 cells. The SPD contains 9.83 x 10^6 pixel cells in total. The half-staves are mounted on 10 light-weight carbon fiber sectors, each sector supporting 4 half-staves on the inner layer and 8 half-staves on the outer layer. The pseudorapidity coverage of the inner layer is $|\eta| < 1.95$.
2. SPD electronics 2.1. Electronics system architecture The pixel chips provide binary hit information, which is stored in a delay line during the L1 trigger latency. In case of a positive L1 decision the hit is stored in one out of four multi event buffers where the data wait for the L2 trigger decision to be read out or discarded. In each half-stave, a multi-chip module (MCM) initiates the read-out and performs the configuration process of the pixel chips. The connection to the control room is established via three optical fibers. The MCM contains three ASICs and a custom developed 800 Mbit/s optical link for the data transfer between the detector and the control room. All on-detector ASICs have been implemented using a commercial 0.25μm CMOS process; radiation hardness is obtained by appropriate gate design rules and by redundancy in the critical nodes. In the control room FPGA-based electronics performs zero suppression, data formatting and sends the data to the ALICE data acquisition system.

2.2. Electronics integration
The compactness of the design sets severe constraints on the material budget and dimensions of the detector elements and the interconnects.
The very small clearance between the SPD inner layer and the wall of the beam pipe requires that the overall radial thickness of the half staves is less than 3 mm. The width of the half-staves is determined by the pixel chip
dimensions; the clearance between the edges of adjacent half-staves is down to ≈ 0.2mm and the width of the MCM substrate is limited to 11mm in order to avoid interference with the other structural elements. In order to
keep the material budget within 1% X0 (each layer), the read-out chip and the sensors are 200 μm thick and the
pixel chips are thinned down to 150 μm. The interconnection between the pixel chips and the read-out MCM is
established via an multi-layer flexible bus in which aluminium layers are used as conductor to even further reduce
the material budget.

2.3. Full system and production tests
Full system tests in beam setups and in the laboratory of the entire detector system including the sensors, pixel
read-out chips, the multi-chip module, the optical links, the off-detector electronics, the ALICE trigger system and
the ALICE data acquisition system have been performed.

2.4. Summary

The tight material budget and the limitation in physical dimensions required by the detector design introduce new
challenges for the integration of the on-detector electronics. The full system as well as an overview of the integration of the on-detector electronics are presented.

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