Test and commissioning of the CARLOS control boards for the ALICE Silicon Drift Detectors

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Abstract

This paper presents the test strategy employed during the installation of the CARLOS end ladder boards developed for the Silicon Drift Detectors (SDD) of ALICE. Each CARLOS board compresses the data provided by the front-end electronics of one SDD and sends them via an optical link of 800 Mbit/s to the data concentrator card (CARLOSrx) located in the counting room. The paper describes the integration of the CARLOS boards in the final SDD system, including its cooling and mechanical support, the power supply distribution and the optical interconnections. The results of the tests performed after each step of the installation sequence are reported.

I. INTRODUCTION

The ALICE SDD system consists of two cylindrical layers. The detectors are mounted on linear carbon fibre supports, called ladders [1]. The inner layer ("layer 3") is made of 14 ladders and the outer layer ("layer 4") of 22. The number of detectors per ladder is 6 for layer 3 and 8 for layer 4. The ladders are readout from both ends. An SDD module is formed by a sensor and its front-end electronics [2], which is located on two hybrids mounted near the sensor. Each module has its own low voltage and high voltage distribution cards and is read-out by a dedicated CARLOS board.

A module needs three optical links implemented over single mode fibres with 1310nm wavelength. The links provide respectively the following signals:

1. master clock, at 40.08 MHz, obtained from the TTC net [3];
2. serial back-link, at 40.08 Mb/s, used to download the configuration parameters for the readout electronics and to transmit the trigger signal to the module;
3. data-out and BUSY; at 800 Mb/s, based on the GOL - QPLL chip-set and used to transport the output data to the data concentrator (CARLOSrx) [4].

The links are laid down between the detectors and the racks located in Counting Room, about 50 meters away. At the detector side the links are headed on the CARLOS board. Each card carries one pigtailed laser-pill and two pigtailed PIN-diodes. The pigtails are terminated with MU connectors which are inserted in MU-MU adapters. These are mounted on the carbon-fibre structure supporting the ladders (see Figure.1).

The monitoring of vital parameters of the read-out chain such as voltage levels, current consumption and temperature is performed by DCU chips [5] located on the low-voltage and on the CARLOS boards. The chips are driven by the Detector Control System (DCS) unit through the I2C bus. The CARLOS board also provides to the front-end hybrids the analog and digital power supply, under the control of the DCS system.

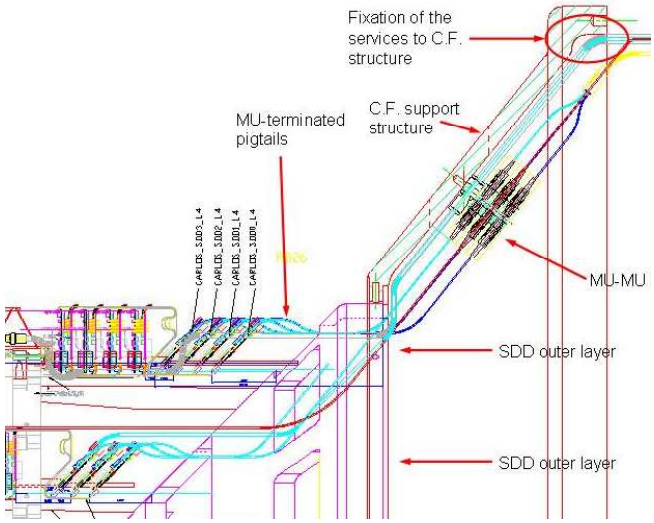

Figure 1: Layout the optical link.

II. CARLOS End Ladder Board

The CARLOS board is placed on both sides of each ladder with the purpose of acquiring and compressing the data coming from each SDD module before sending them towards the CARLOSrx card located in counting room. The board contains the compression chip CARLOS [6], [7] that applies a bi-dimensional compression algorithm to the data stream coming from front-end electronics.

The 16-bit output of the ASIC is serialized via the Gigabit Optical Link (GOL) [8]. The CARLOS board has a size of 54mm x 49 mm and a thickness of only 16 mm in order to comply with the material budget constraints imposed by the experiment.

The board has been initially characterized with a dedicated test system [9]. In a second phase more extensive measurements were performed using a complete SDD chain, from the actual front-end hybrids to the CARLOSrx card and the ALICE DAQ system [10]. These tests confirmed the full functionality of the board.

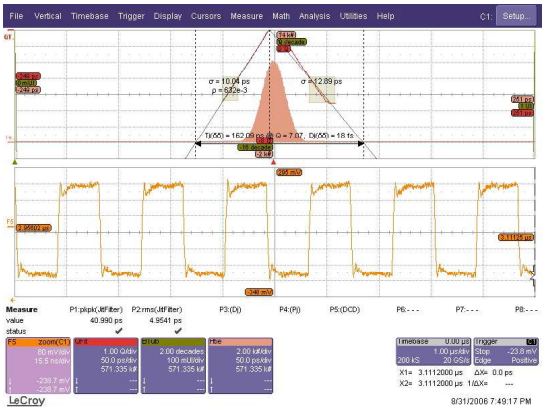

Figure 2: QPLL jitter filtering results.

Figure 2 shows the measurements for the CARLOS end ladder board hosting the QPLL circuit. The output clock jitter is less than 10 ps RMS when the jitter of the input clock is less than 120 ps RMS. This performance is fully adequate for our application.

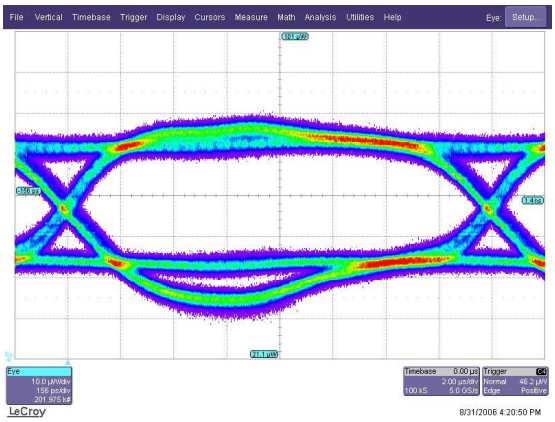

Figure 3: Eye diagram at 800 Mbits/s.

The CARLOS end ladder board delivers a clean eye diagram when driven with a bias current of 16 mA at 800 Mb/s, as shown in Figure 3. At this current, the optical power output from the MU connector is approximately –3 dBm.

Figure 4 shows the bathtub plot for the transmitting data via optical link. The horizontal axis is the Unit Interval (UI) of 1.25 ns, and the logarithmic vertical axis is the bit error rate (BER). The estimated BER from the signal-to-noise ratio of the eye diagram is less 10^{-16} with a 70% open eye. This diagram shows the quality of the optical link and of the filtered clock.

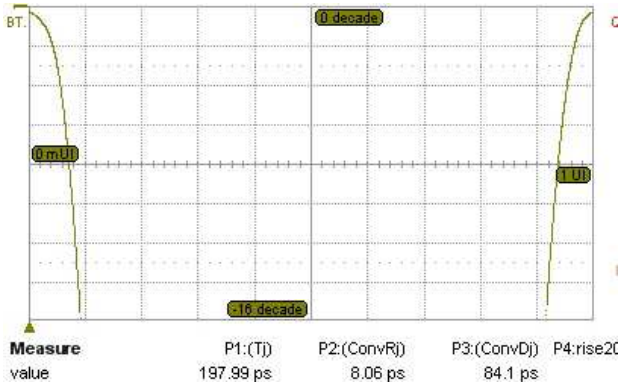

Figure 4: Bathtub curve.

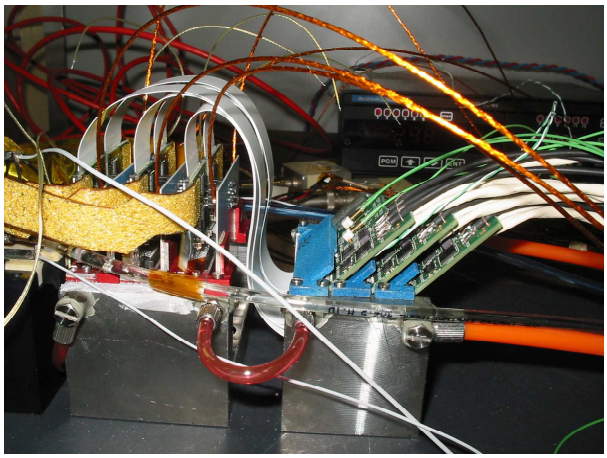

Figure 5: CARLOS end ladder boards assembled in the ladder structure.

III. Integration With The FEE

The CARLOS end ladder board has been tested and assembled in the ladder structure with the final FEE, readout and power supply electronics. In Figure 5 the CARLOS end ladder boards placed to the end side of the ladder are shown. The connections between the detectors and the front-end electronics, and between the module and the low and high voltage supplies are assured with flexible aluminium-polyimide micro-cables that are Tape Automatic Bonded (TAB). The dataset that originate from the FEE enters the card through the Molex connectors and is read by the CARLOS chip. No errors were attributed to the CARLOS end ladder board during these tests.

Figure 6: The SDD detector completely assembled, ready to be integrated with the Silicon Strips.

IV. CARLOS End Ladder Board Assembled In The SDD Barrel

The ladders have been assembled on a CFRP (Carbon-Fibre Reinforced Plastic) structure made of a cylinder, two cones and four support rings. The cones provide the links to the outer Silicon Strip Detector barrel and have windows for the insertion of the SDD services. Each ladder, once assembled and measured, was completely tested. In a few cases, modules with problems were replaced. In Figure 6 the completely assembled SDD detectors are shown, prior to insertion in the SSD.

Figure 7 shows the SDD barrel routing for optical links, power supplies and I2C control busses for one side of the SDD system. The routing is identical at the other side. Each side contains the following parts:

- 130 SDD detectors
- 260 FEE cards
- 130 CARLOS end ladder boards
- 390 optical links (clock at 40.08 MHz, serial back-link at 40.08 Mb/s, data-out at 800 Mb/s)
- 390 power supply cables
- 390 I2C cables for control bus
- 130 High voltage cables of – 2.4 KV
- 130 bias supply cables of − 40 V

As an example of final system performance Figure 8 and 9 show the RMS noise measured for two typical SDD ladders. These figures have been obtained with the SDD already integrated in the full ITS.

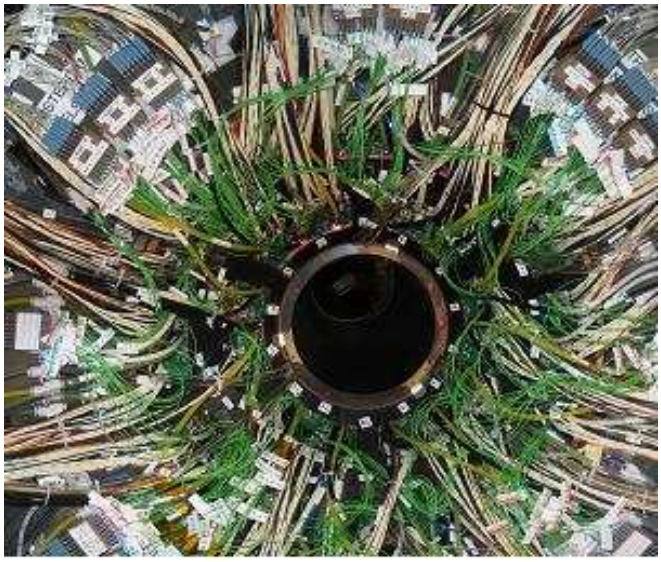

Figure 7: SDD barrel routing for optical link, power supply and I2C control bus.

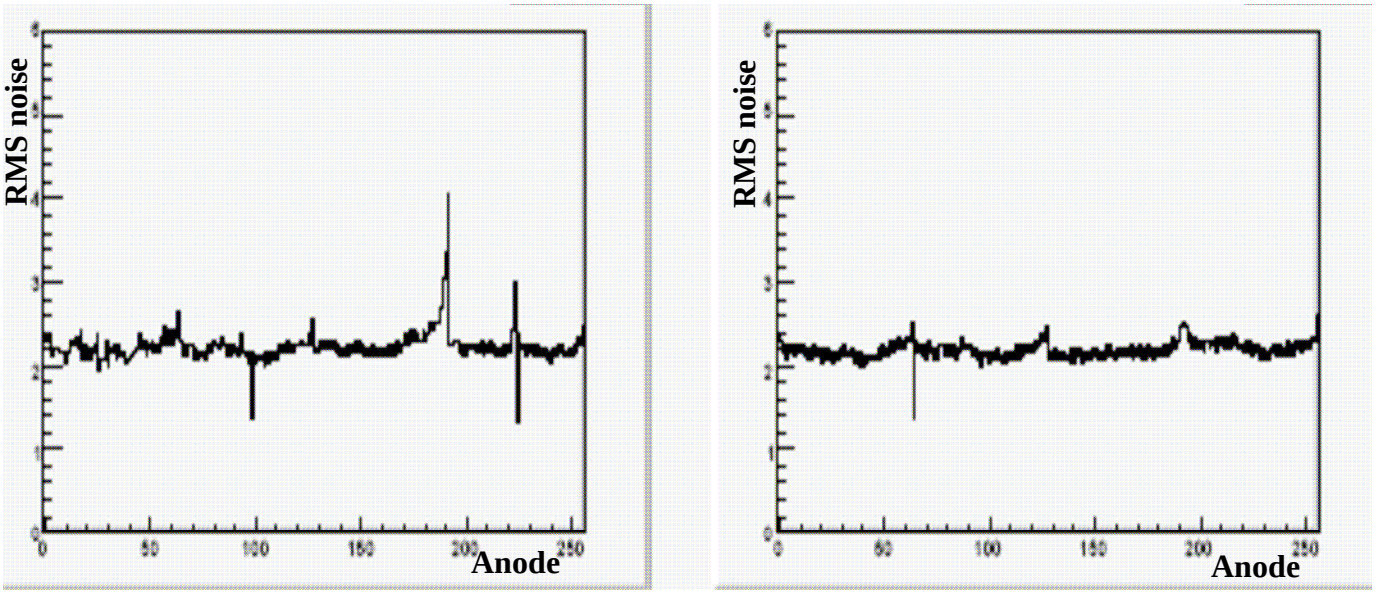

Figure 8: RMS noise for layer 4 ladder 15 (module 0).

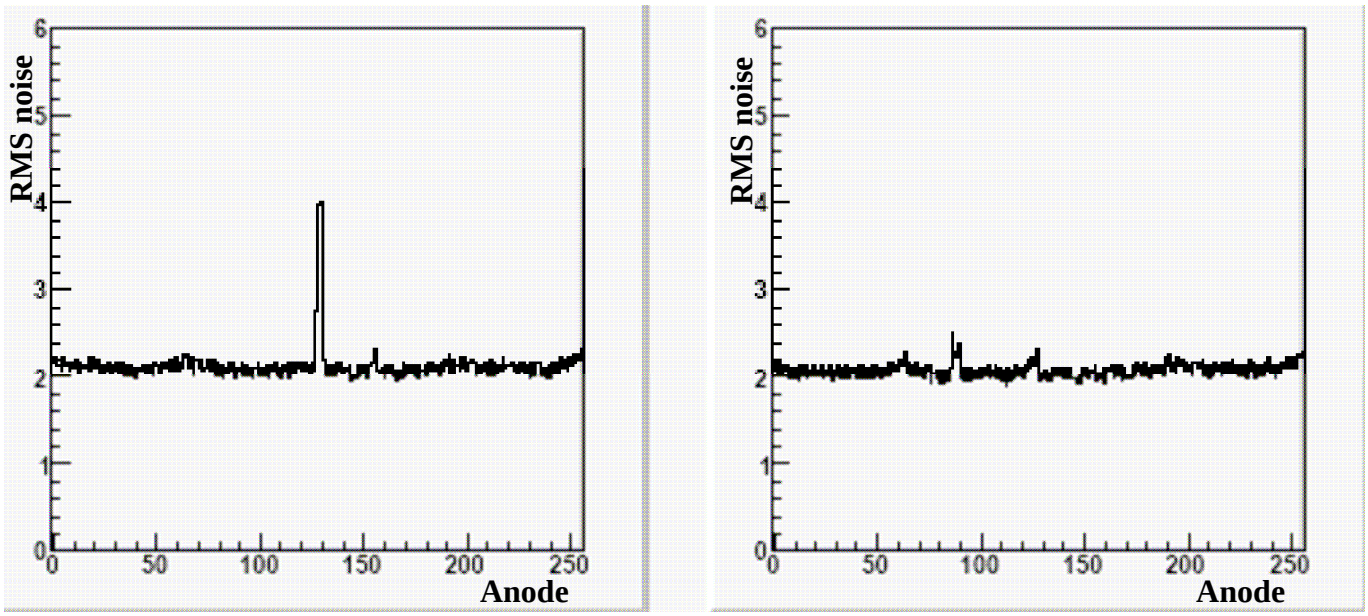

Figure 9: RMS noise for layer 3 ladder 3 (module 0).

V. CONCLUSIONS

The 260 CARLOS end ladder boards were assembled in the complete SDD barrel structure, that contains FEE electronics, cooling system and mechanical supports. The test of the complete system was successful for what concerns both data transmission and DCS features. The CARLOS end ladder board has a clean eye diagram, low bit error rate (less 10^{-16}) and low clock jitter (10 ps RMS). The noise level after the integration of the SDD in the final apparatus is at the same level of the noise measured for a single ladder. This further validates the architecture implemented for the SDD readout and front end electronics.

VI. REFERENCE

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