Inductor based switching DC-DC converter for low voltage power distribution in SLHC

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Abstract

In view of a power distribution scheme compatible with the requirements of the SLHC environment, we are evaluating the feasibility of on-board inductor-based DC-DC step-down conversion. Such converter should be an integrated circuit and capable of operating in harsh radiation environments and in the high magnetic field of the experiments. In this paper we present results concerning the choice of the technology, the search for the magnetic components and the calculations of the expected efficiency.

I. Introduction

The distribution of power in LHC experiments faces difficult engineering challenge, given the global requirements in terms of power needs, available cooling capacity and limited material budget. The harsh radiation environment (up to several Mrd in Total Ionizing Dose) and the intense magnetic field (up to 4 T) make conventional switching converters unusable in many locations. Therefore the present LHC distribution scheme foresees power suppliers outside the detector. The front-end circuits are reached with long cables that do not guarantee a stable input voltage and dissipate power in heat, increasing the cooling system's load. In some case linear regulators are placed on intermediate patch panels to stabilize the input voltage closer to the load.

In view of LHC upgrades where front-end circuits might require even larger supply currents at low voltage, it is necessary to evaluate an alternative power distribution scheme. This could be based on the distribution of higher voltage (12-24 V, in comparison with the actual solution of 2-4 V) from external power supplies to custom made radiation-hard converters capable of resisting to high magnetic field, installed locally inside the detectors. They will then convert the power to the low voltage and high current required by the front-end circuits.

In this context we are developing an inductor based switching DC-DC step-down converter. This work focuses on the analysis of the different components of the converter to assess their availability and the feasibility of a converter matching the above requirements.

II. Choice of the converter architecture

Step-down converters can be divided in 2 classes: isolating and non-isolating. Isolating converters have no electrical path between source and load while non-isolating devices have a common ground between source and load. The first class uses transformers and the second uses just one inductor. We are evaluating the possibility of using a non-isolating step-down converter topology called buck. A schematic illustration is shown in Figure 1. The buck converter is composed by two power transistors (SW1 and SW2 in Figure 1), an inductor, a capacitor and a control circuit. The two transistors work in opposition of phase and they are used as switches that alternately connect and disconnect the input voltage to the inductor. The latter is used as an energy storage element, accumulating energy in the first phase and delivering it in the second one. The capacitor is used in combination with the inductor in order to filter spurious harmonics and make the ripple on the output signals smaller. The control circuit regulates the duty-cycle of the modulated signal that drives the transistors. This is made in order to provide a constant output voltage even though the current needed by the load may be changing.

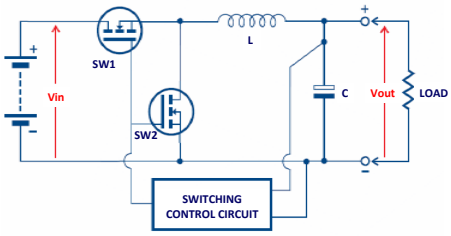

Figure 1: Basic step-down (buck) converter.

The choice of the technology for the design of the two power transistors and the control circuit is dictated by the radiation tolerance requirements and the need of working with high voltages. The two transistors are directly connected to the input voltage (12 - 24 V) so they need to be able to operate with such voltage applied between source and drain. It is also necessary to choose magnetic components able to properly work in presence of a 4 T magnetic field because of the saturation of all ferromagnetic materials. Another key point in the design is to limit the power dissipation and to attain the highest efficiency possible. Parameters such as input/output voltage, output current, inductors resistance and inductance, output voltage ripple and transistor size can be chosen to optimize the efficiency.

In the following sections the study of a suitable CMOS technology, the choice of the inductors and evaluation of achievable efficiency will be described. Then, having fixed the specifications for the power transistors, they were designed, fabricated and tested. Irradiation results concerning these transistors will be presented.

A. *Technology*

Because of the limited number of high voltage technologies available on the market, a 0.35 μm CMOS technology usually employed in automotive applications was evaluated for the design of the power transistors. The transistors of this technology can stand a V_{DS} of up to of 80V. A study was made to assess total ionizing dose (TID) tolerance of the technology. Tests were performed on transistors embedded in a custom developed chip named Dosetest. Available NMOS transistors in the technology have both vertical and lateral geometry, and samples of the two were integrated in the test chip. Other than the layout recommended by the foundry (standard), devices with modified layout inspired from the ELT (Enclosed Layout Transistors) technique used in low voltage CMOS technologies to enhance radiation tolerance ([1] [2]) were designed and tested. In this paper these transistors will be called MLT (Modified Layout Transistors). All NMOS transistors have W=80 μm. Lateral PMOS transistors, with foundry-recommended (standard) layout, were also included.

Transistors were irradiated at room temperature and under bias using the X-ray machine available within the ESE group at CERN. The dose rate most commonly used was about 20 krd/min, and irradiation was performed in steps up to TID levels of the order of 30-80 Mrd (SiO_2). Different bias conditions were used for NMOS transistors, whilst PMOS transistors were always exposed with all terminals grounded.

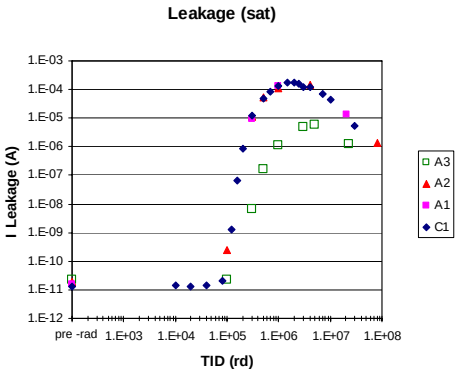

Figure 2: Evolution of the leakage current for NMOS transistors with standard layout, for 4 different chips. Chip A3 has been irradiated with a smaller bias on the gate (2 V) and V_{ds}=30 V.

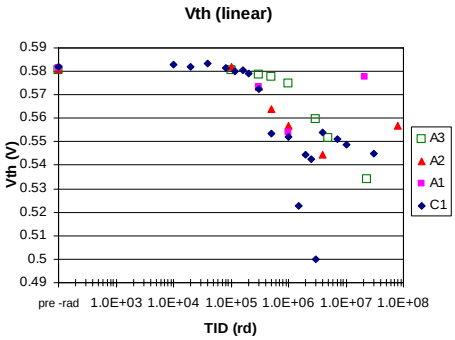

Figure 3: Evolution of the threshold voltage for NMOS transistors with standard layout. Same conditions as described in Figure 2.

NMOS transistors were exposed with either 3.3 V on the gate and all other terminals grounded, or with 2 V on the gate and 14 V on the drain, a condition for which a current of the order of several mA was flowing in the transistors.

In the following, for NMOS transistors only results for the vertical devices will be presented since their performance is superior for our application (both in terms of R_{on} and radiation tolerance).

As shown in Figure 2, NMOS transistors with standard layout suffer from an increase of the leakage current, defined as the value of I_{DS} with V_{GS} =0 V and V_{DS}=30V, with doses up to 1 Mrd. Due to the radiation-induced trapping of positive charges in the thick lateral oxide, a parasitic leakage path opens between source and drain. Above the peak of leakage current which is around 1 Mrd, the leakage current starts to decrease. This is due to formation of interface states. These defect states at the interface between the thick lateral oxide and the channel trap negative charge (in the case of NMOS transistors), and tend therefore to reduce the leakage current [3] [4]. This effect only gets visible after some time in our irradiation test, and determines a decrease of the leakage at TID levels above about 1 Mrd.

Due to trapping of positive charge in the gate oxide, the threshold voltage of NMOS devices decrease with TID. In most tested devices the V_{th} shift is below 50mV, as shown in Figure 3. Variations in mobility and on-resistance are measuerd to be below respectively 20% and 8% respectively.

As shown in Figure 4 the modification of the layout in the MLT transistors eliminates the source of leakage current and only a residual increase of leakage due to a decrease in V_{th} and increase of the subthreshold swing (from 86 mV/dec to 92 mV/dec) is observed. Threshold voltage shift is limited to about -40mV in all conditions for the range of TID explored. Mobility variations below 20% and on-resistance variations generally below 10% have been observed.

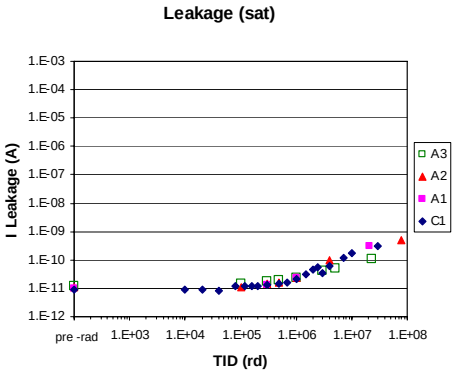

Figure 4: Evolution of the leakage current for NMOS transistors with modified layout. Same conditions are the same as described in Figure 2.

In PMOS transistors no increase in the leakage current is observed. In this case both trapped charge and interface states are positive and contribute to increase the threshold voltage of the parasitic lateral transistors. As a consequence it is not necessary to modify the layout of these transistors.

The main radiation-induced degradation in the charachter-

istics of the PMOS transistor is an increase of the threshold voltage. This can be observed in Figure 5 for transistors with W=80 μm.

The decrease in mobility is always below 20%. As a consequence of the V_{th} increase, also the on-resistance has a slightly larger increase than for NMOS transistors, about 20-25% after the largest TID.

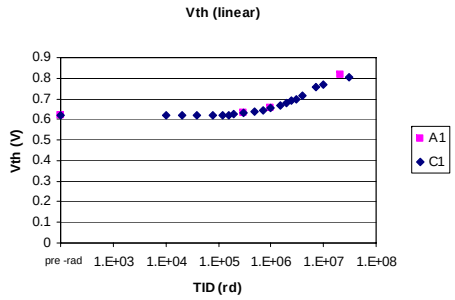

Figure 5: Evolution of the leakage current for PMOS transistors for 4 different chips.

All these studies were made on high voltage transistors, but also low voltage transistors will be used in our application for the control circuitry working at 3.3V. NMOS transistors need to have enclosed layout (ELT) and guardrings because they show a sharp increase of the leakage at 160-200 krd (from pA to tens of μA). ELTs show no increase in the leakage and shifts of the threshold voltage limited to below 40mV. At the same time, variation in mobility was measured to be below 10% for all doses up to 10Mrd and the increase in subthreshold swing was typically from 85 (prerad) to 89 mV/decade. Low-voltage PMOS transistors, as for high voltage applications, do not require dedicated layout to achieve good radiation tolerance. The threshold voltage increases (in absolute value, in reality it gets more negative) with TID, to reach a maximum of about 150mV after 10 Mrad. This is a relatively large shift, and requires to be carefully taken into account in the design of circuits operating in a radiation environment. At the same time, the mobility decreases by about 30% whilst the subthreshold swing does not change significantly from its pre-rad value of about 86-88 mV/decade.

In conclusion, the results obtained on the Dosetest vehicle show that using dedicated layout techniques this technology is suitable for applications in a radiation environment. It is possible to integrate NMOS transistors, both low- and high-voltage, showing no increase in source-drain leakage with irradiation up to several tens of Mrd and a negligible change in the V_{th}. The main problem with PMOS transistors, that instead do not require any special layout, is the increase of V_{th} with dose (and decrease of mobility and transconductance). For the specific application of the DC-DC converter, the best high-voltage transistor appears to be the vertical NMOS. Compared with the PMOS, it allows for smaller on-resistance, more stable performance with dose (the PMOS has a significantly larger V_{th} shift and increase in on-resistance) and additionally also smaller gate capacitance.

B. Inductors

The magnetic elements within a switching power supply play a cornerstone role in its operation. The very high external magnetic flux density (up to 4 T) strongly limits the choice of the inductor because it prevents the possibility to use conventional magnetic cores. This is due to the saturation of all ferromagnetic materials. In Tab. 1 some properties of ferromagnetic materials with high value of saturation flux density are shown ([5], [6] and [7]).

Ferromagnetic materials as permendur and iron can reach values of saturation flux density up to 2 T (2.45 T and 2.15 T respectively), but at 4 T all the magnetic domains align their dominant magnetic orientation in the direction of the applied magnetic field. In this case the core can make no further contribution to flux growth and any increase thereafter is limited to that provided by the air permeability (roughly three orders of magnitude smaller). Therefore unless new ferromagnetic core materials are found, it will be necessary to use an air core inductor. Clearly air core inductrs are limited in the total inductance that can be reached with reasonable physical dimensions. In addition long coils obviously have higher parasitic resistance.

Material	μ **at B=2 mT**	**Max.** μ	**Sat B (T)**
Cold rolled steel	180	2,000	2,1
Iron	200	5,000	2,15
Purified iron	5,000	180,000	2,15
4% Silicon-iron	1,500	30,000	2,0
45 Permalloy	2,500	25,000	1,6
Hipernik	4,500	70,000	1,6
Monimax	2,000	35,000	1,5
Permendur	800	5,000	2,45
2V Permendur	800	4,500	2,4
Hiperco	650	10,000	2,42

Table 1: *Permeability (μ) and saturation flux density of magnetic materials*

Air core inductors between 500nH and 1μH are foreseen as a good balance between these constrains. They are commercially available with a range of resistance that can vary between 6 mΩ to 90 mΩ with a volume of 39 cm^3 and 0.27 cm^3 respectively (obviously smaller inductors have bigger resistance).

C. Efficiency evaluation

After having characterized the technology and the inductors it is now possible to carefully investigate the power losses of the circuit due to the presence of non-ideal components. After having found the analytical formulae for each source of power loss, a model of the power losses in the circuit which takes into account the major components responsible for these losses has been written. The program computes the overall efficiency as a function of the most important system parameters such as the resistances of the transistor and inductor, the large gate capacitance of the power transistors, the controller and driving circuits.

For example the use of this program is illustrated in Figure 6 with V_{in}=24 V and V_{out}=2.5 V and for different values of output current. In the following W is the width of the transistor, L the value of the inductance, R_{ind} the resistance of the inductor. Choosing an inductor with L=538 nH and R_{ind}=6 mΩ we can estimate the efficiency of the DC-DC converter as a function

of W. Some other parameters as the switching frequency or the duty cycle are automatically calculated by the program.

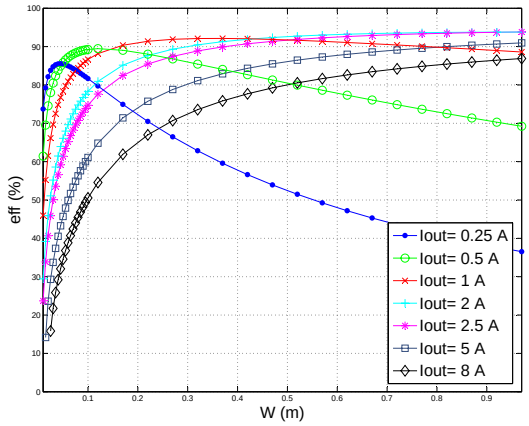

Figure 6: Efficiency vs W with V_{in}=24 V, V_{out}=2.5 V, R_{ind}=6 mΩ and L=538 nH, and for different values of I_{out}

From Figure 6 it is possible to conclude that an efficiency close to 90% could ideally be achieved, in particular for output current larger than 1 A, but this would requires very large transistors (the dimension of W is expressed in meters!). Figure 6 also shows that the parasitic resistance and capacitance of the power transistor have a big impact on the overall efficiency of the converter. If the dimension of the transistor is small (less that 0,1m) the dominant power dissipation is on the R_{on}. Increasing W, we can see that the efficiency increase till a certain value (for $0,1 < W < 0,2$) and than it remains constant or decreases, depending on the output current value. This is due to gate capacitance that is increasing as well, determining a bigger power dissipation on it during the switching phase.

In the next section, a practical integration of the switch transistors is described, where a W of 0.1 m was chosen as the best compromise between efficiency and occupied area.

III. Design of the power transistors

Power transistors have to be especially designed in order to be radiation tolerant; additionally their area is limited by yield-related considerations. Given the large current flowing (up to 4 A) its layout was studied to minimize the resistance between input and output terminals. The layout was also estimated to maintain low gate resistance.

Multiple unit cells have been used for the design of these large transistors. This allows a more uniform distribution of the current over the different cells, hence a more efficient use of each cell. It also has the benefit that many more drain contacts are available, which improves the possibilities for routing and increases substantially the yield of the circuit.

The choice of the dimensions of the unit cell is driven by the necessity to compromise the occupied area and the time propagation of the gate signal. With this technology the resistance of the polysilicon and the gate capacitance set the maximum dimensions of the width of each transistors finger at 50 μm in order to have a gate rise-fall time below 1ns. The optimum choice of 8 fingers for the unit cell, each with W=50 μm, yields a W of 400 μm and an area of around 5451 μm^2 (69 μm$\times$79 μm) for the cell. The 0.1 m width transistor is hence composed of 264 unit cells. This gives a dimension of 1656 μm $\times$ 869 μm.

This rectangular shape was chosen because two switching transistors are necessary for the buck converter, and the stack of two transistors of the chose shape occupies a nearly square area of 1656 μm $\times$ 1739 μm. To minimize parasitic drain and source resistance all four metal layers have been used. The foreseen R_{on} resistance is around 330 mΩ and the foreseen gate capacitance is 150pF. To prevent ESD damage to the gate oxide, protection diodes have been added to the gate pad. Adding the external wells and pads, the occupied area is around 4 mm^2. The resulting layout is shown in Figure 7.

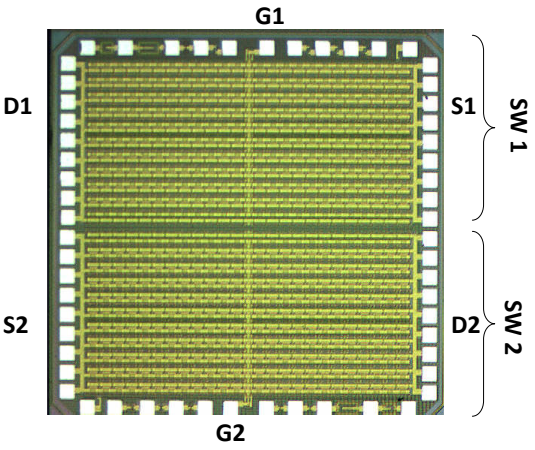

Figure 7: Layout of the two power transistors

IV. Power transistors tests

The designed transistors were fabricated in a Multi-Project Wafer (MPW) run. Measured electrical parameters and irradiation results are presented in this section. The measured R_{on} resistance, one of the most important parameters for these devices, has been estimated to about 350 mΩ, value closed to the nominal 330 mΩ. The estimate took into account the parasitic resistance introduced by bonding wires, ceramic package and measurement socket, since measurements were performed on packaged parts.

Transistors were irradiated in the same conditions described before, but at a larger dose rate of 68 krd/min. The maximum TID level reached during this tests was 170 Mrd. Three different bias conditions were used during irradiation of the different samples exposed to X-rays. In the first condition the source and drain are grounded and 3.3 V applied to the gate (MOS 1 in the figures). In the second condition (MOS 2) the drain is instead connected to a 0.5 A current generator, hence a current is flowing in the device. In the third condition (MOS 3) the gate and source are grounded and 20 V are applied on the drain.

Leakage current, threshold voltage shift and on-resistance versus the total ionizing dose are reported in the following figures. The points indicated as “post-rad” refer in fact to measurements taken after annealing of, respectively, 9 hours,1 day, 1 week and 2 weeks after the end of the irradiation sequence. It should be noted that the second week of annealing took place at a temperature of 100^O C. This procedure, common practice in

the study of radiation effects on semiconductor devices, allows to estimating the long-term annealing of the radiation-induced defects. It is in fact commonly assumed that this procedure simulates annealing for 10 years at room temperature.

Figures 8 to 10 evidence that the switch transistor does not suffer significant degradation after irradiation. The leakage current does not increase (Figure 8), the threshold voltage shift is always limited below 50 mV (Figure 9), a value well acceptable for our design, and the on-resistance does not increase after a dose of 170 Mrd (Figure 10). This is a very good result indicating that the layout modifications we implemented are effective in eliminating any leakage current path, and confirming that these vertical transistors are excellent candidate for the integration of the switching transistors of the buck converter.

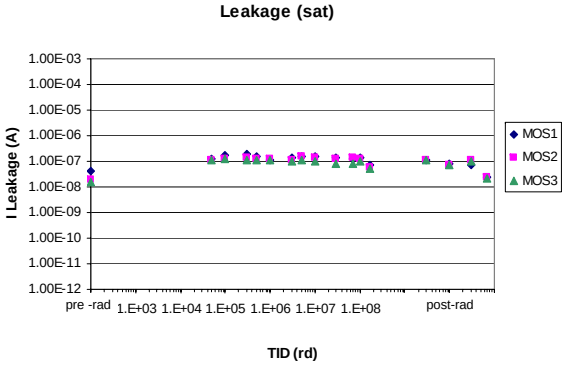

Figure 8: Evolution of the leakage current for 0,1m NMOS transistors with modified layout

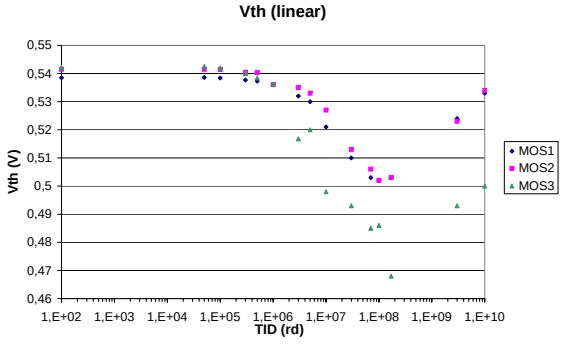

Figure 9: Evolution of the threshold voltage for 0,1m NMOS transistors with modified layout

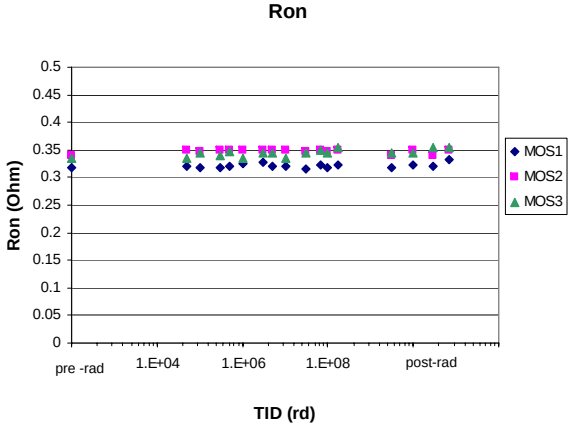

Figure 10: Evolution of the on-resistance for 0,1m NMOS transistors with modified layout

V. Conclusions

In view of power distribution in the SLHC detectors, we have studied the possibility to integrate a simple DC-DC step-down converter to achieve an efficiency above 75-80%. In this paper, we addressed the research of solutions leading to a converter able to cope with the radiation and magnetic field requirements of the SLHC environment.

Only air-core inductors can operate in the 4T magnetic field. Such components are commercially available and imply an increase of the switching frequency of the converter to about 1 MHz, which is compatible with the performance of the high-voltage technologies available today. The radiation response of different devices in a CMOS high-voltage technology originally developed for automotive application has been measured. With dedicated layout techniques, the high-voltage transistors in this technology demonstrated tolerance to TID levels exceeding 170 Mrd.

The full circuit design is now ongoing aiming at a monolithic solution including the control circuit.

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