A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips readout at the ILC

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on behalf of

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Outline

- Silicon strips data
- Goals in 130nm CMOS
- Present results
- Chip 2 and further tests
- Next chip

Silicon strips data at the ILC

- Pulse height: Cluster centroid to get a few µm position resolution
  10cm-1m long strips, possibly strixels
  Shaping time of the order of the microsecond

  Detector pulse analog sampling at 10-20MHz
- Time: 150-300 ns for BC identification,
- Buffering: Occupancy implies a few events per strip
  8-16 deep event buffer/strip
- Power cycling: 1 ms data taking at 5 Hz

Millions of channels:
Integration of k-scale channels readout chips

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Goals and Status

Full readout chain integration in a single chip including digitization

	This chip
- Preamp-shaper	yes
- Zero-suppression decision (threshold analog sums)	yes
- Pulse sampling: Analog pipe-lines	yes
- On-chip digitization: ADC	yes
- Multi-event Buffering and pre-processing: Centroids, least squares fits	no
- Lossless compression and error codes	no
- Calibration and calibration management	no
- Power switching (ILC timing)	no
	4 channels

Future:

CMOS 90nm 128 ch.	2008
512-1024 channels planned	2009

Targeted numbers

- Amplifier: 30 mV/MIP gain
- Shaper: 700ns-3 μs
- Sparsifier: Threshold on analog sum
  auto-zero

- Sampler: 16-deep
- Event buffer 16-deep
- ADC: 10-bit, 10KHz

- Noise:

Measured with 180nm CMOS:
375 + 10.5 e-/pF @ 3 μs shaping, 210μW power

Front-end in 130nm

130nm CMOS:

- Smaller
- Faster
- Less power
- Will be (is) dominant in industry
- (More radiation tolerant)

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Noise slightly increased (1/f)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date

UMC CMOS Technology parameters

	180 nm	130nm
3.3V transistors	yes	yes
Logic supply	1.8V	1.2V
Metals layers	6 Al	8 Cu
MIM capacitors	1fF/mm^2	1.5 fF/mm^2
Transistors	Three Vt options	Low leakage option

Used for analog storage during < 1 ms

2006-7 Chips

130nm CMOS

Both under test

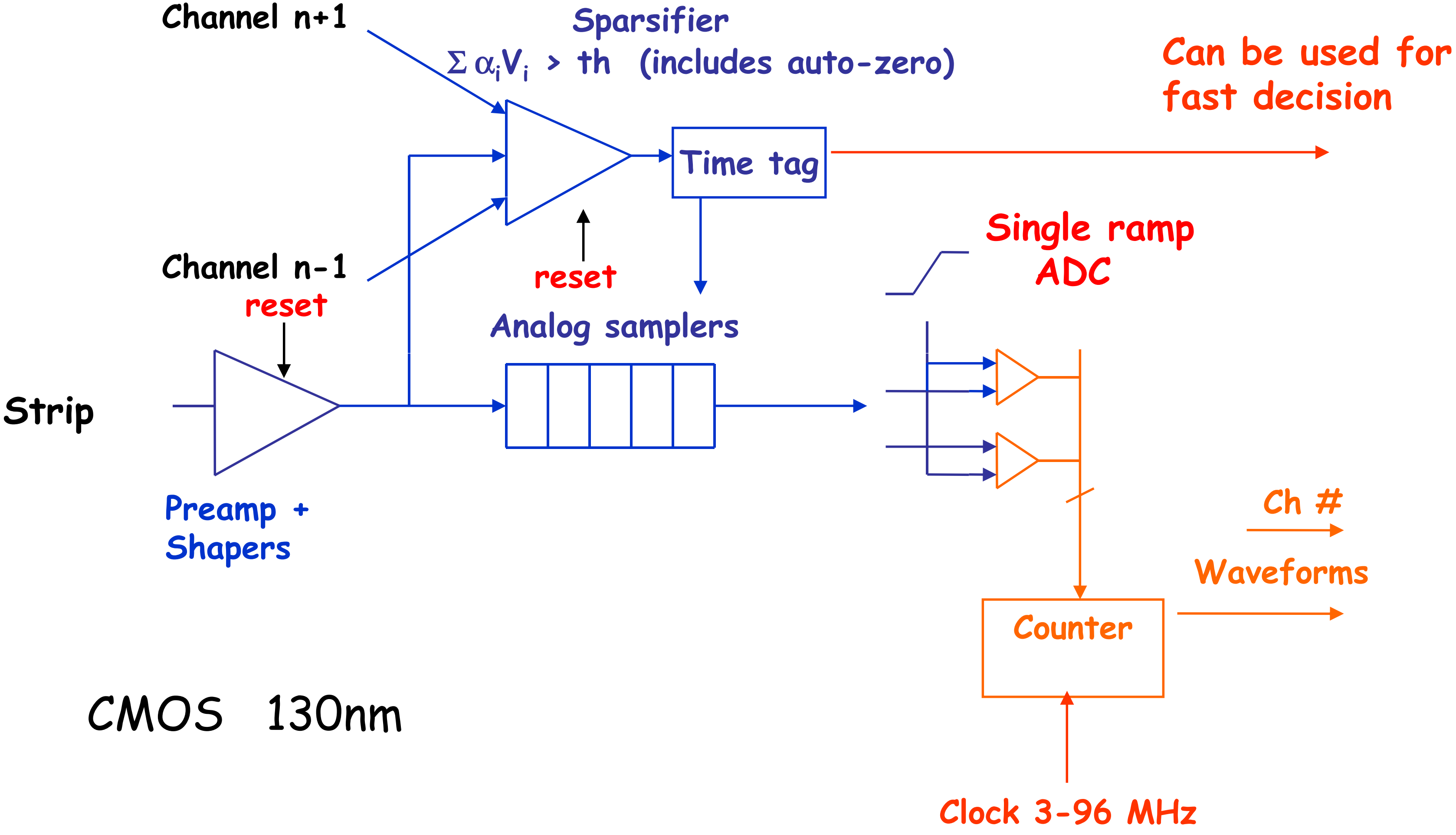
Chip #1 (4 channels)

- Preamp-shapers + Sparsifier
- Pipeline 1
- ADC
- Digital

Chip #2 (One channel)

- Preamp-shapers + Sparsifier
- DC servo
- Pipeline 2 (improved)
- DAC
- Test structures: MOSFETS, passive

4-channel Chip



Channel n+1

Sparsifier

$\Sigma \alpha_i V_i$ > th (includes auto-zero)

Can be used for fast decision

Time tag

Single ramp ADC

Channel n-1

reset

reset

Analog samplers

Strip

Preamp + Shapers

Ch #

Waveforms

Counter

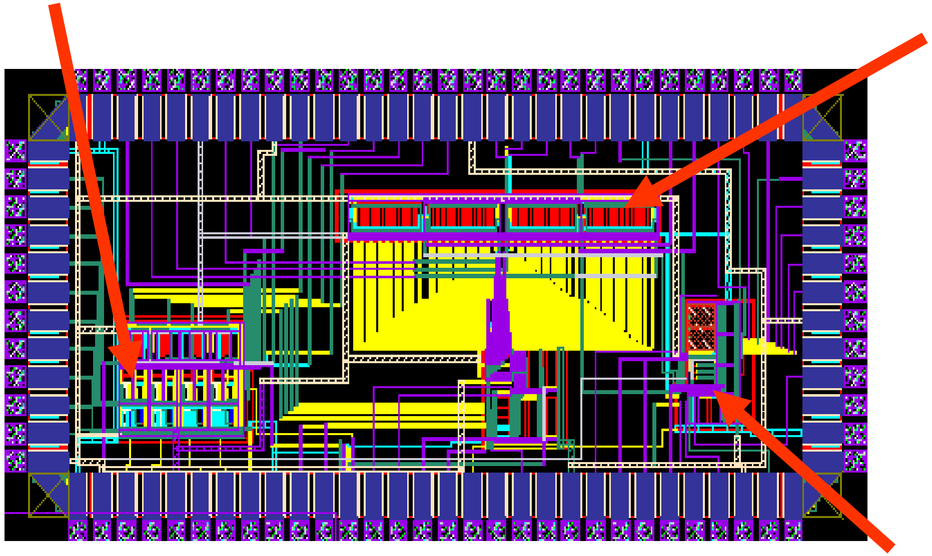
Clock 3-96 MHz

CMOS 130nm

4-channel chip layout

Amplifier, Shaper, Sparsifier 90*350 µm^2

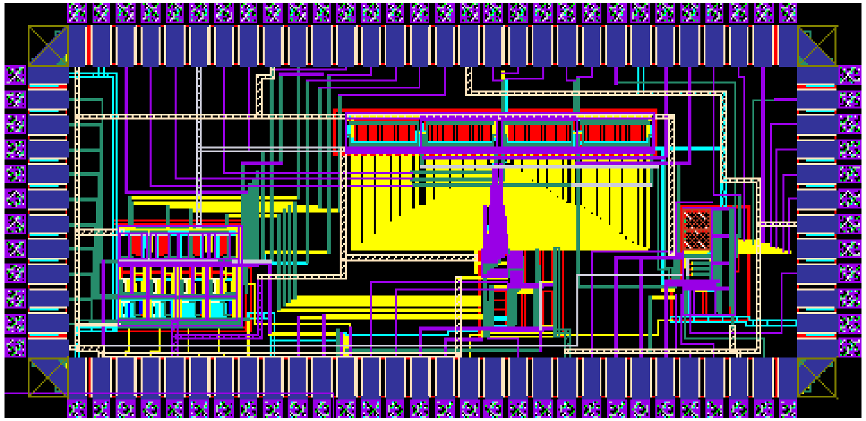
Analog sampler 250*100 µm^2



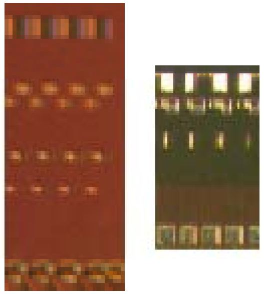
A/D 90*200 µm^2

Layout of the 130nm chip including sampling and A/D conversion

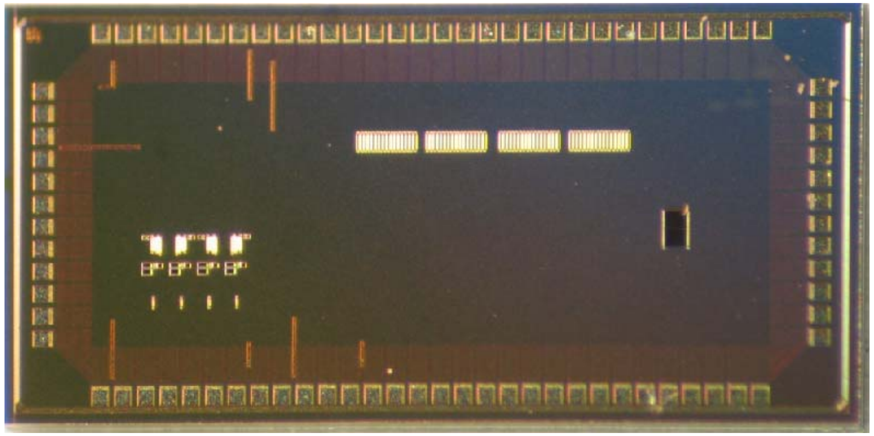
4-channel 130nm Silicon



Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm



Picture

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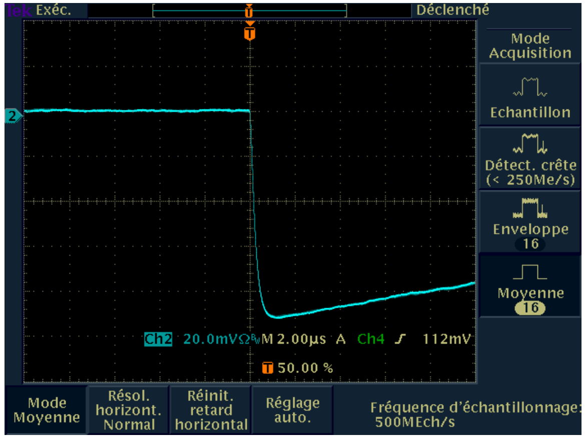
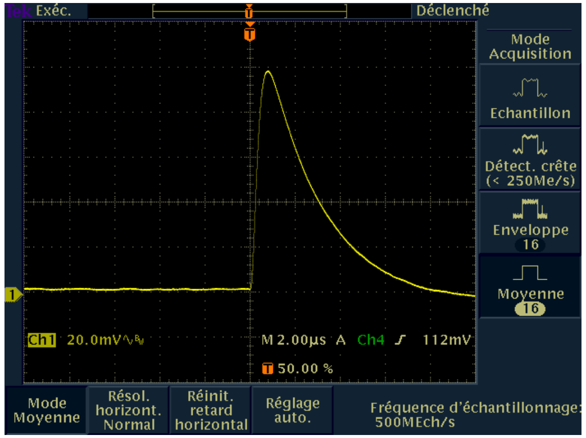
Results

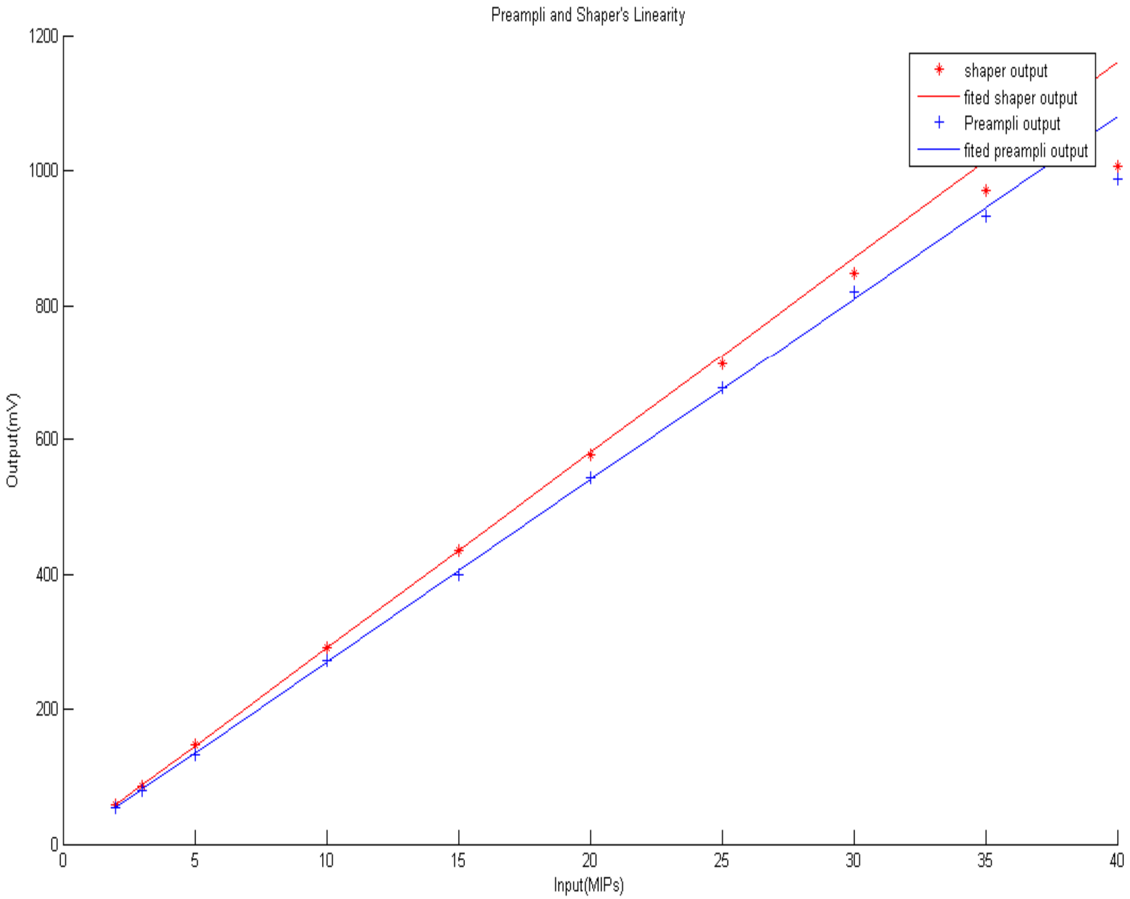
Measured gain - linearities

Preamp output





Shaper output

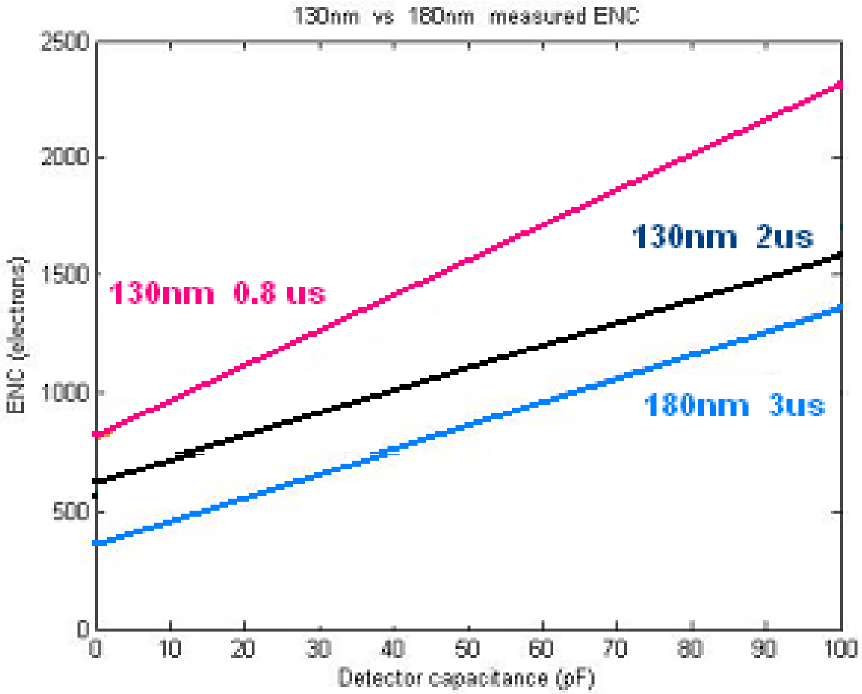


Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

130nm vs 180nm chip noise results

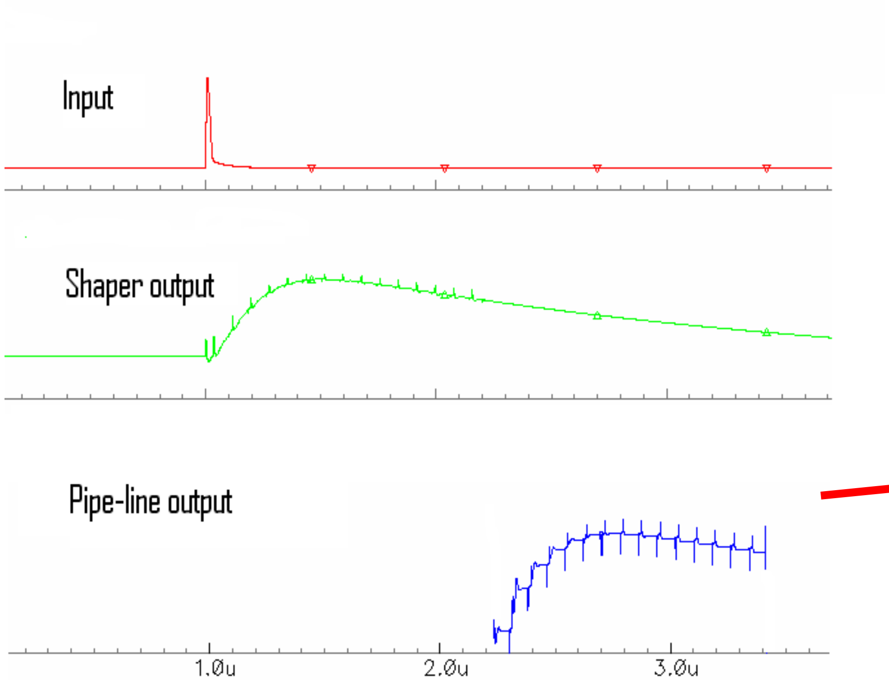
Gain OK:	**29 mV/MIP**	**OK**
Dynamics:	**30 MIPs @ 5%, 20 MIPS 1%**	**OK**
Peaking time:	**0.8 – 2.5 µs**	**(0.7 – 3 µs targeted)**



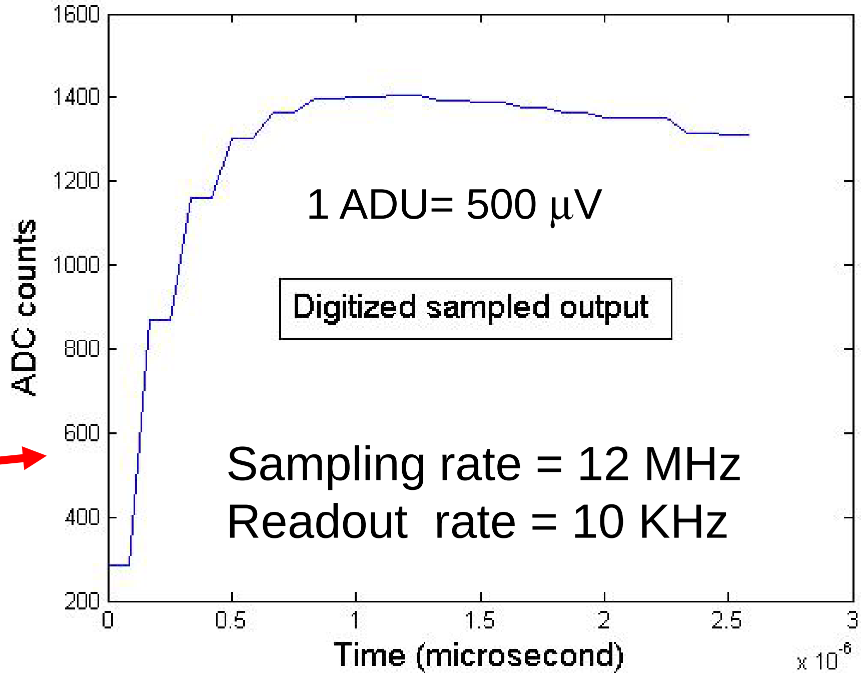
Power (Preamp+ Shaper) = 245 µW

Noise:	130nm @ 0.8 µs :	850 + 14	e-/pF	245 µW	(150+95)
	130nm @ 2 µs :	625 + 9	e-/pF		
	[180nm @ 3 µs :	375 + 10.5	e-/pF	210 µW	(70+140)]

Digitized analog pipeline output



Simulation of the analog pipeline (analog)



Measured output of the ADC (pulser)

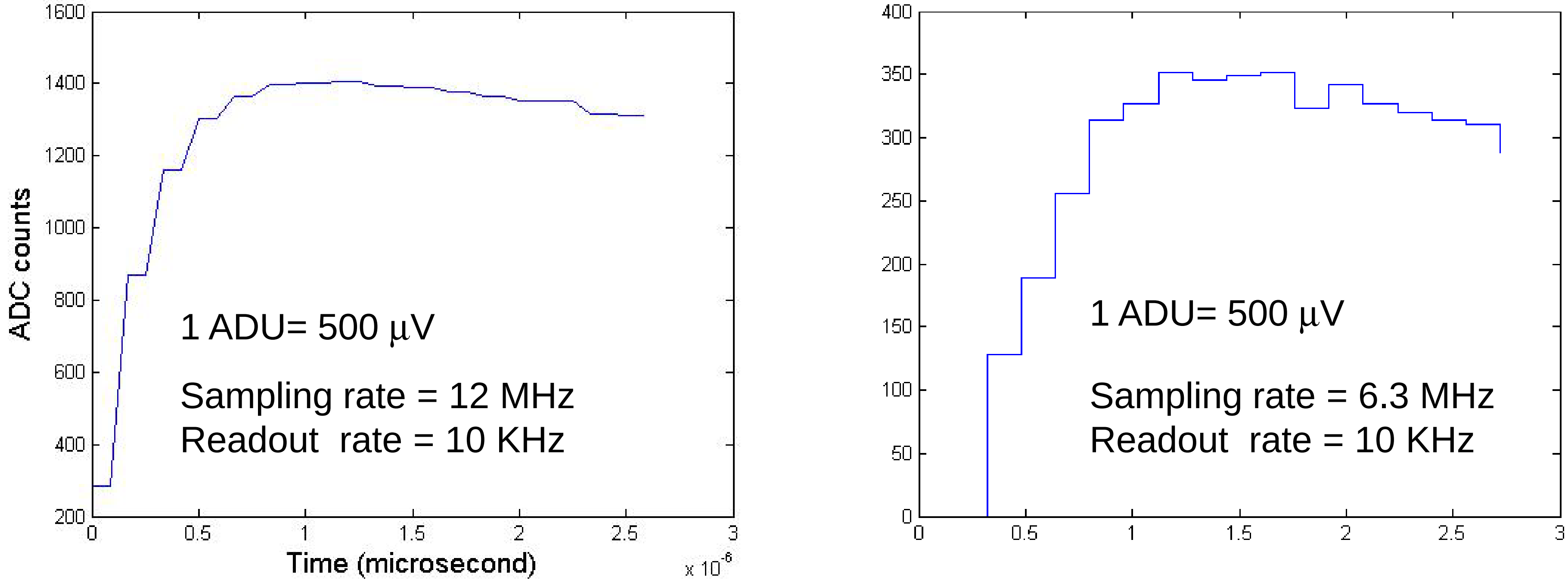
Waveform distorted due to 1pF parasitic capacitance of the output pad connected for analog diagnostics on 2 out of four channels

Traces cut using IFB to get all shaper channels operational to ADC for beam tests

Chip 2 includes a voltage buffer between shaper and ADC

Digitized analog pipeline output
Laser response of detector + 130nm chip

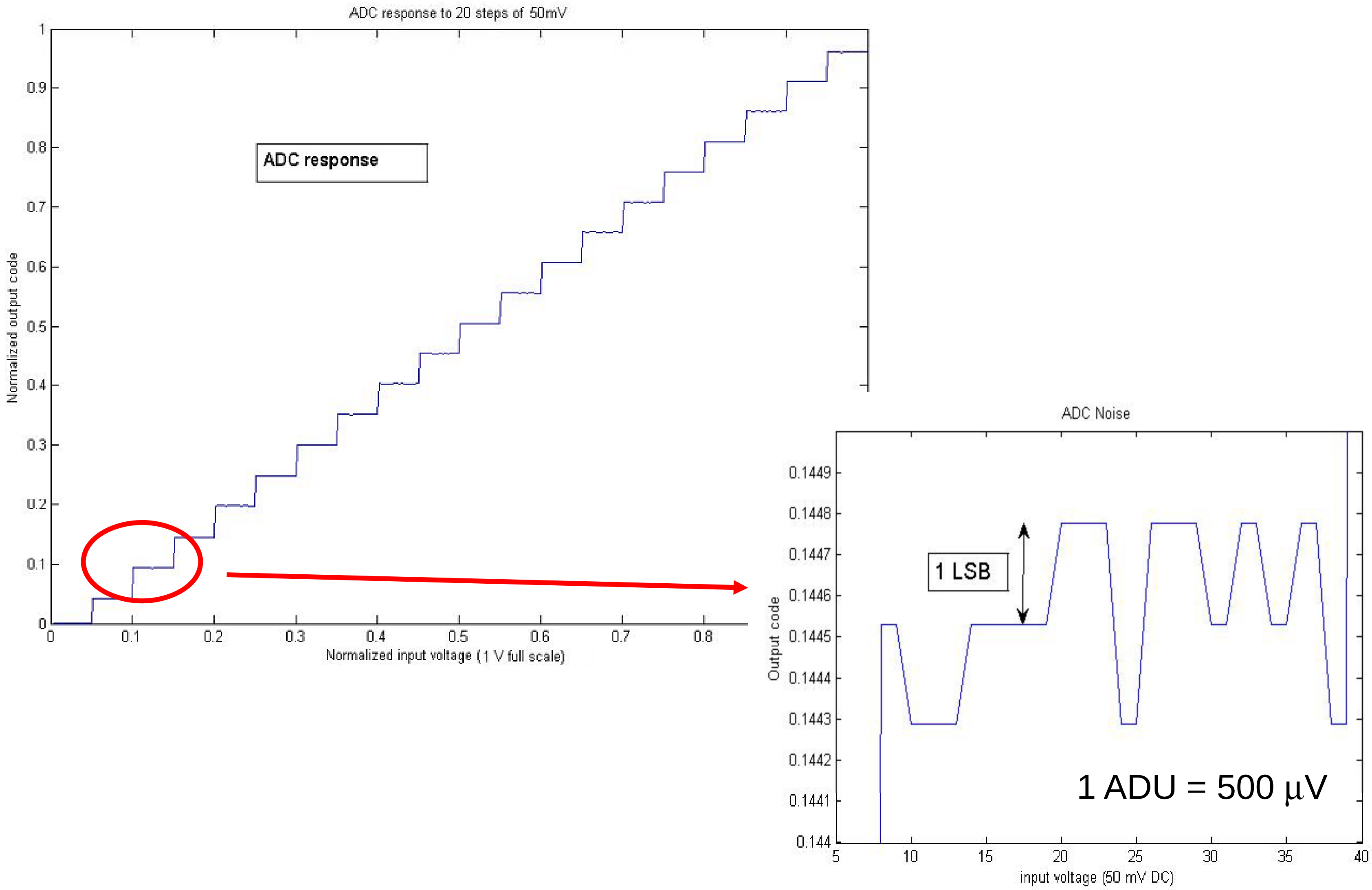
Digitized shaper output



From pulser

From Laser diode + Silicon detector

ADC first look…



1 ADU = 500 µV

130nm Chip 2

LAPP Annecy le Vieux (R.Hermel, D. Fougeron)

One channel test version in 130nm including:

- Preamp + shaper
- Improved pipeline (output buffer)
- Calibration channel (calibration caps)
- Calibration DAC

Chips 2 presently under test

If OK, all analog blocks will be validated for a multi-channel version in 130nm aiming to read a real detector in 2008

130-1 chip's tests to come

- Lab tests: Measure ADC extensively

Linearities	Integral, differential
Noise	Fixed pattern, random
Speed	Maximum clock rate
Accuracy	Effective number of bits

- Next beam tests at CERN end October

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130-2 tests under work (LAPP Annecy)

Measure improved pipeline extensively

Denis Fougeron's (LAPP) design

Linearities	
	Integral, differential
Noise	
	Pedestal fixed pattern, random noise Maximum clock rate
Droop	
	Hold data for 1 ms at the ILC

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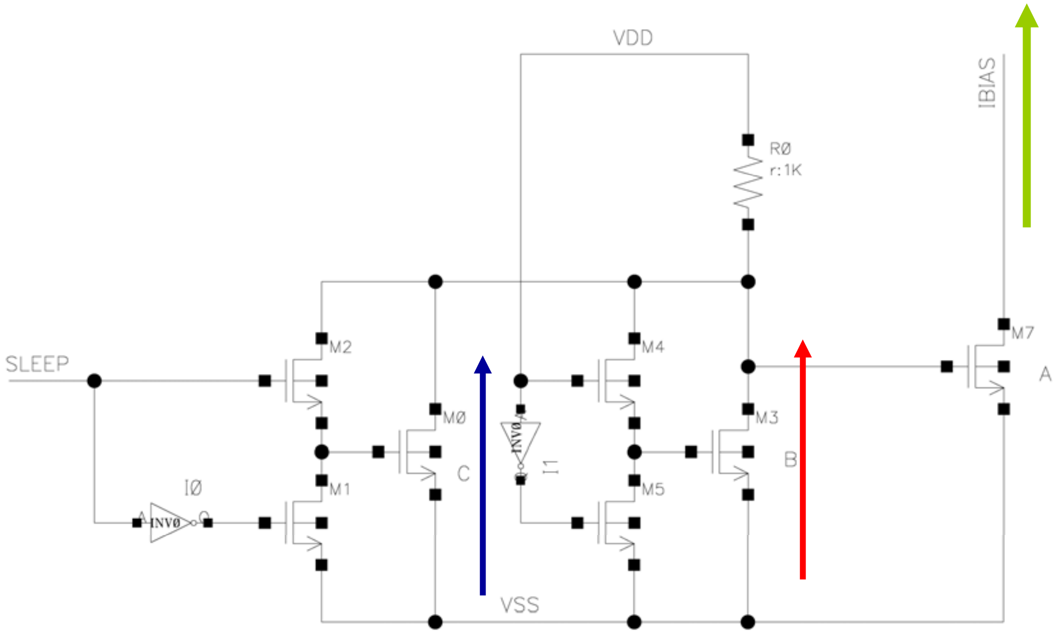
Chip 130nm-3

Equip a detector

- Experience from lab test bench (laser + source) and 2007 beam-test
- 128 channels with :
  - Preamp-shapers + sparsifier
  - Pipeline
  - ADC
  - Digital
  - Calibration
  - Power cycling

Power cycling

Switch the current sources between zero and a small fraction (10^{-2} to 10^{-3}) of their nominal values



This option switches the current source feeding both the preamplifier & shaper between 2 values:

Zero or a *small fraction* (0.1% - 1%) of biasing current is held during « power off ».

Zero-power option tested on 180nm chip

Planned Digital Front-End

- Chip control

- Buffer memory

- Processing for

  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data lossless compression

- Tools
  - Cadence DSM Place and Route tool
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs

Need for a mixed-mode simulator

Some issues with 130nm design

- Noise likely modeled pessimistic, but measured quite acceptable

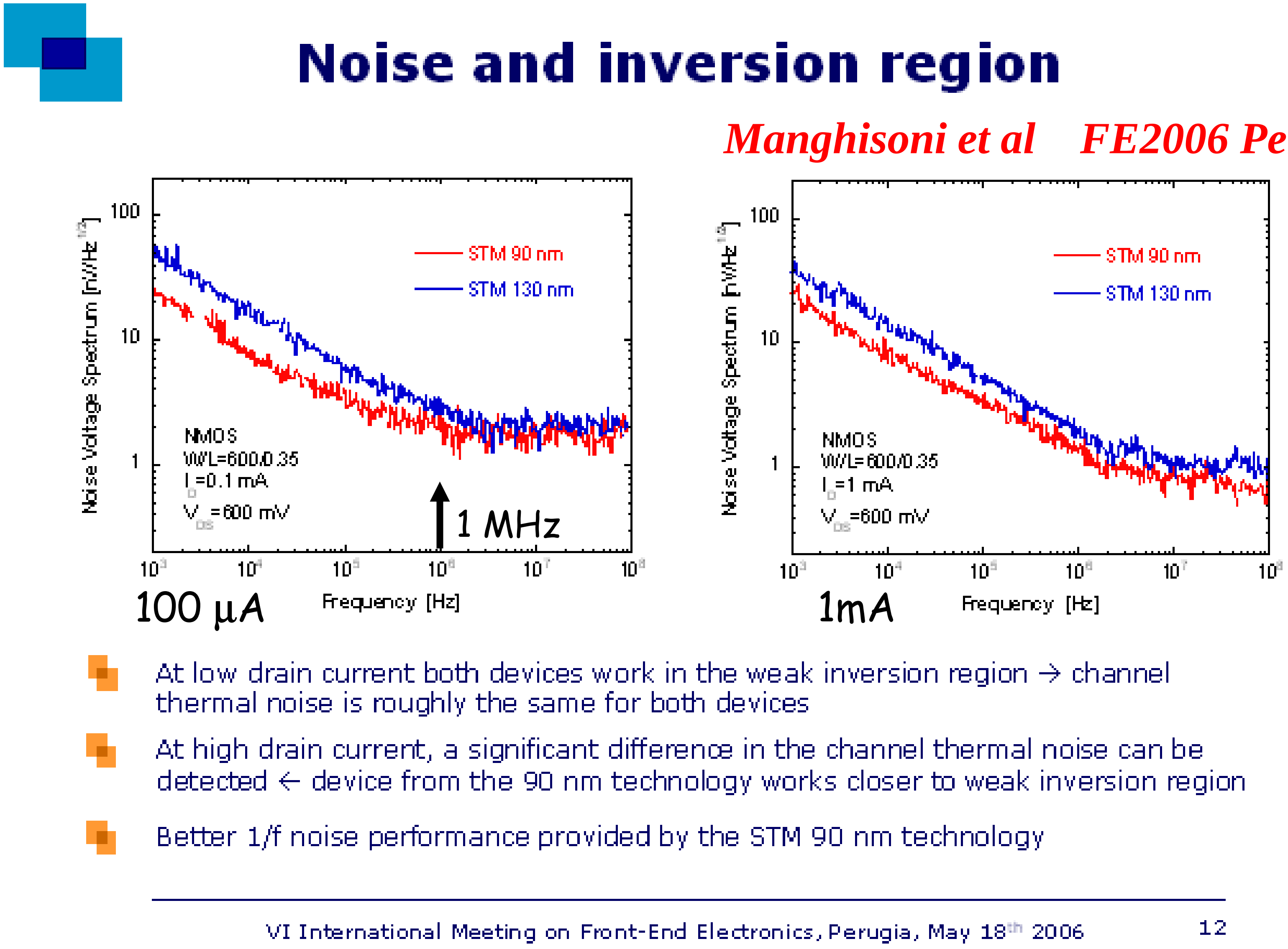
  90nm could be less noisy (Manghisoni, Perugia 2006)
- Lower power supplies voltages reducing dynamic range
- Design rules more constraining
- Some (via densities) not available under Cadence

  Calibre (Mentor) required.
- Low Vt transistors leaky (Low leakage option available at regular Vt)

Manageable, UMC design kits user friendly,
Europractice very helpful.

130-90nm noise evaluation (STM process)

Manghisoni et al FE2006 Perugia



Noise and inversion region

- At low drain current both devices work in the weak inversion region → channel thermal noise is roughly the same for both devices
- At high drain current, a significant difference in the channel thermal noise can be detected ← device from the 90 nm technology works closer to weak inversion region
- Better 1/f noise performance provided by the STM 90 nm technology

Conclusion

These CMOS 130 designs and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels) with

- DC power under 500µW/ch
- Silicon area under 100 x 500 μ^2/ch

The End …