A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips Readout at the ILC.

Wednesday, 5 September 2007 15:30 (25 minutes)

A CMOS 130nm evaluation chip intended to read Silicon strip detectors at the ILC has been designed and successfully tested. Optimized for a detector capacitance of 10 pF, it includes four channels of charge integration, pulse shaping, a 16 deep-analog sampler triggered on input analogue sums, and parallel analog to digital conversion. Tests results of the full chain are reported, demonstrating the behavior and performance of the full sampling process and analog to digital conversion. Each channel dissipates less than one milliwatt static power.

Summary

Deep Sub-Micron integrated technologies allow implementing readout chips at low power operation, low material budget, high channel count, and last but not least, fair radiation hardness.

A first 180nm CMOS readout chip for Silicon strips detector has been designed and tested in 2006, and a 130nm improved version has been received and successfully tested recently, taking benefits of the first chip experience.

The 130nm circuit comprises a low-noise charge amplifier with 20mV/MIP gain, a pulse shaper operating between 0.5 and 2 microseconds in order to match various detector lengths and operation conditions, a 16-deep analogue sampler at speeds up to 20 MHz triggered by a sparsifying analogue section, and a 12-bit parallel analogue to digital converter. This structure fits conveniently the ILC timing where data taking occurs for one millisecond, followed by a 200 millisecond time for digitization and readout.

The preamplifier is a folded-cascode structure where the PMOS input transistor is biased at 70 microamperes, providing enough gain to ensure an input stage noise less than $625 + 9e-/pF$ at 2 microseconds shaping time. The shaper is a CR-RC active filter. Power dissipation is 510 microwatts for the preamplifier and shaper that can be switched up and down in less than 1 millisecond.

The sparsifier block has been designed, setting a threshold over the analogue sum of three adjacent channels. In this way, only channels reacting to this selection are sampled in a circular analogue sampler clocked to store sixteen samples of the shapers outputs, including pedestals. Therefore, digitization of relevant data only is achieved in parallel on 12 bits after data taking using a ramping shared ADC.

A single channel including the analogue sampler fits in a 100 x 800 square micrometers area.

Tests results are reported for all blocks, as well.as Signal to Noise ratio when the chip is wire-bonded to an actual Silicon strips detector and stimulated with actual high energy particles.

Primary author: Dr GENAT, Jean-Francois (CNRS/IN2P3/LPNHE)

Co-authors: Dr SAVOY-NAVARRO, Aurore (CNRS/IN2P3/LPNHE Paris); Mr FOUGERON, Denis (CNRS/IN2P3/LAPP Annecy); Mr LEBBOLO, Herve (CNRS/IN2P3/LPNHE Paris); Mr DAVID, Jacques (CNRS/IN2P3/LPNHE Paris); Mr

HUPPERT, Jean-Francois (CNRS/IN2P3/LPNHE Paris); Mr SEFRI, Rachid (CNRS/IN2P3/LPNHE Paris); Dr HER-MEL, Richard (CNRS/IN2P3/LAPP Annecy); Mr PHAM, Thanh Hung (CNRS/IN2P3/LPNHE Paris)

Presenter: Dr GENAT, Jean-Francois (CNRS/IN2P3/LPNHE)

Session Classification: Parallel session B5 - ASICs 2 ILC