CSC DAQ for CMS

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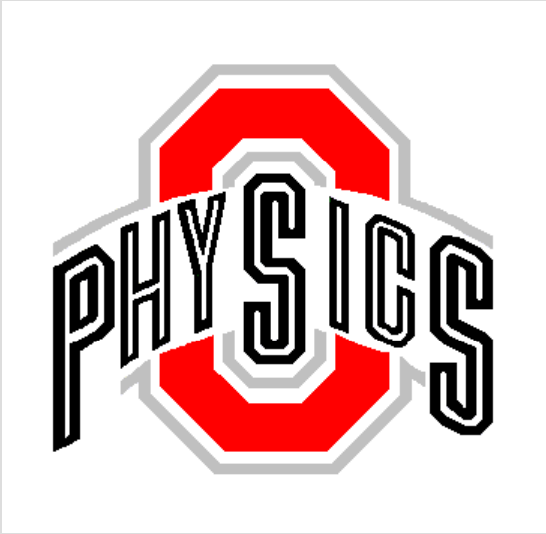
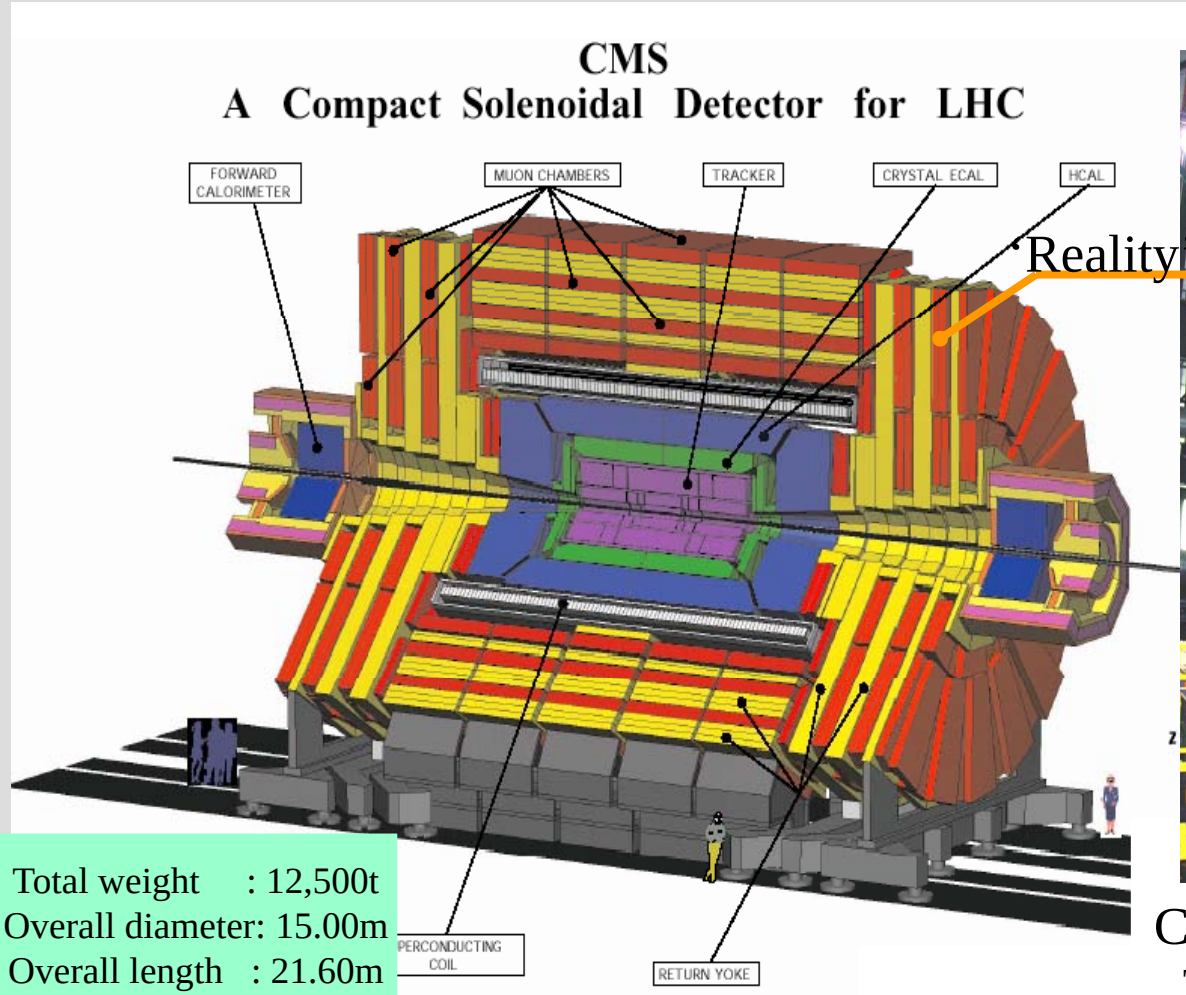
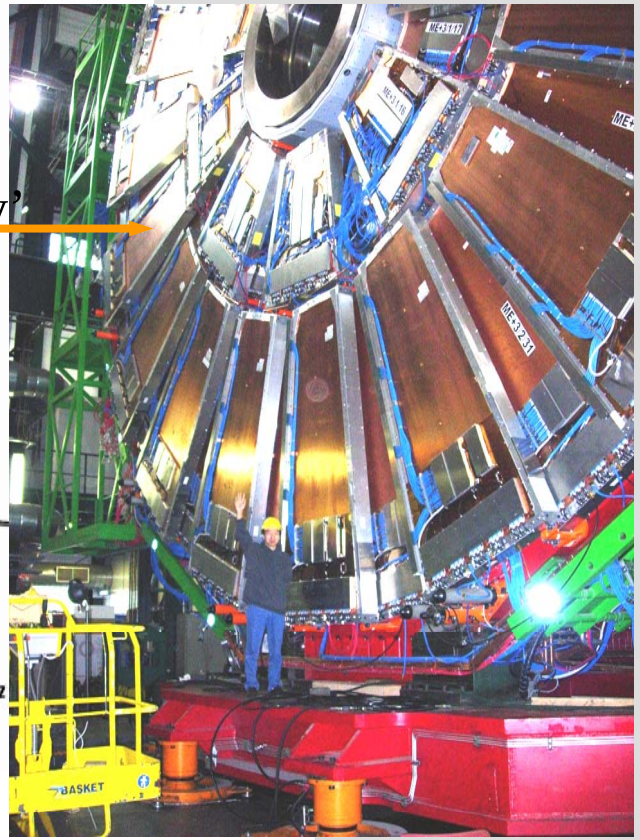
1. Introduction
2. CSC DAQ
    1. On chamber electronics
    2. Off Chamber electronics
    3. Local DAQ farm
    4. Interconnect
    5. CSC DAQ General Issues
3. System test
4. Summary



Introduction: Compact Muon Solenoid (CMS)



'Reality'



Total weight : 12,500t
Overall diameter: 15.00m
Overall length : 21.60m
Magnetic field : 4 Tesla

CSC
Two ends
Eight disks
468 chambers

readout channels:
217,728 Cathode
183,168 Anode

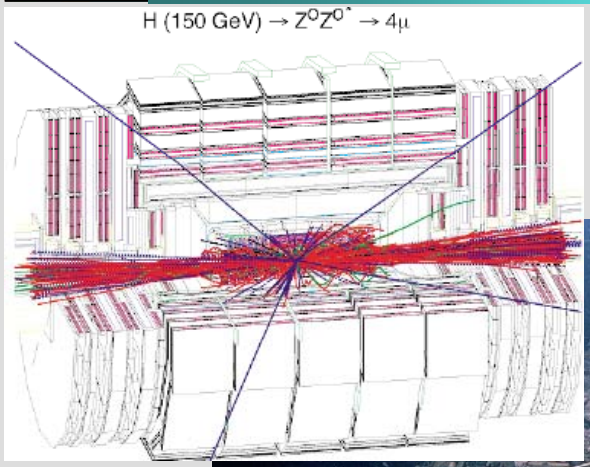
Introduction: Cathode Strip Chambers (CSC)

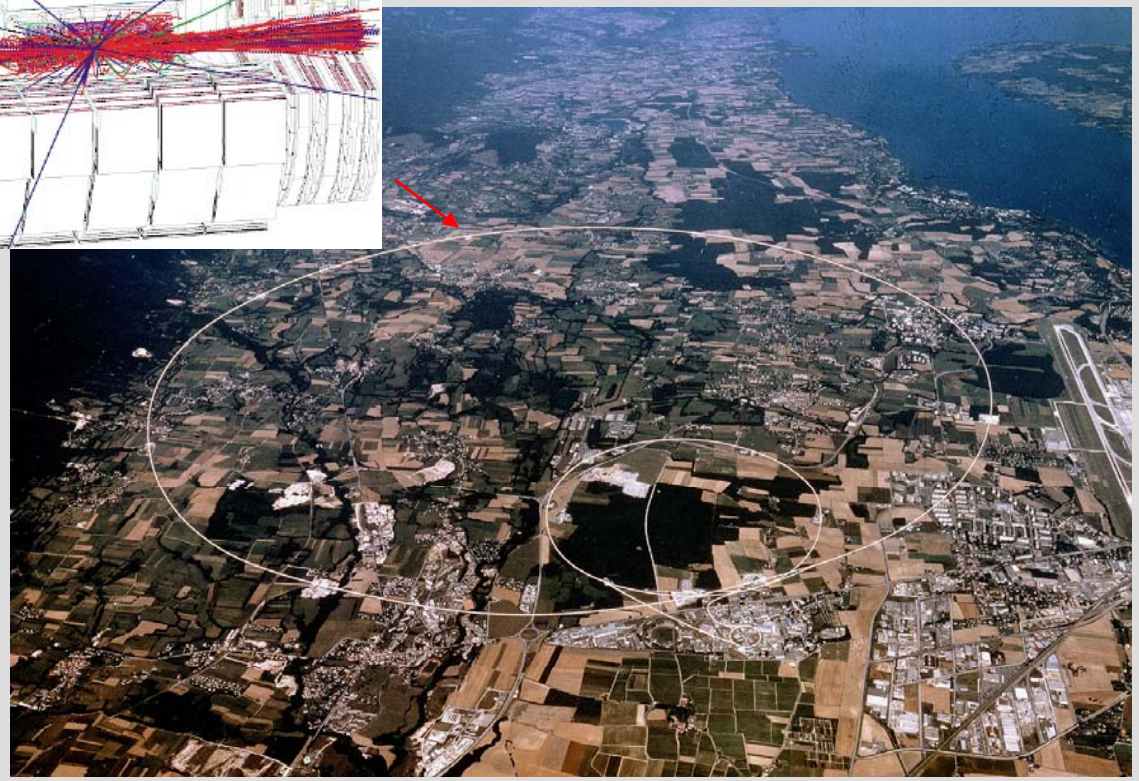
Plus Endcap underground

CSC Statistics

- 468 Cathode Strip Chambers with 6 sensitive planes each
  - 6,000 m^2 sensitive area
    - About 1 football field
  - 218K strip channels
  - 183K wire group channels
- Offline spatial res. ~100 μm
- 4 ns timing resolution

Introduction: Large Hadron Collider (LHC)





- Proton + Proton
- E: 7 TeV + 7 TeV
- Period 25ns
- Rate 20/collision
- Lum: 10**34 $cm^{-2}s^{-1}$
- L: 26.7 km
- D: ~100 m

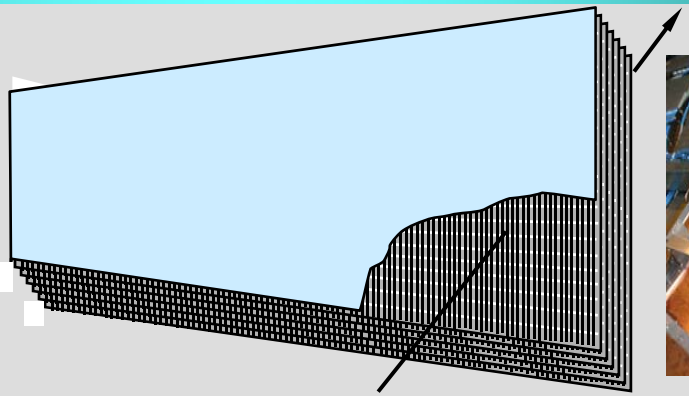
Higgs <~ 1 TeV
New particles: 0.05~5TeV
New physics

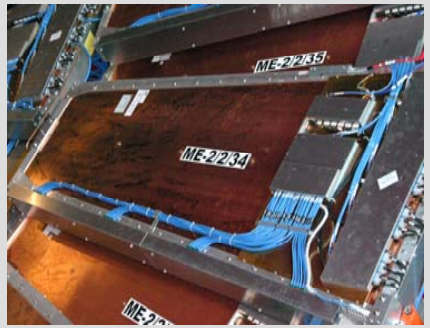
CMS
ATLAS
LHCb
ALICE

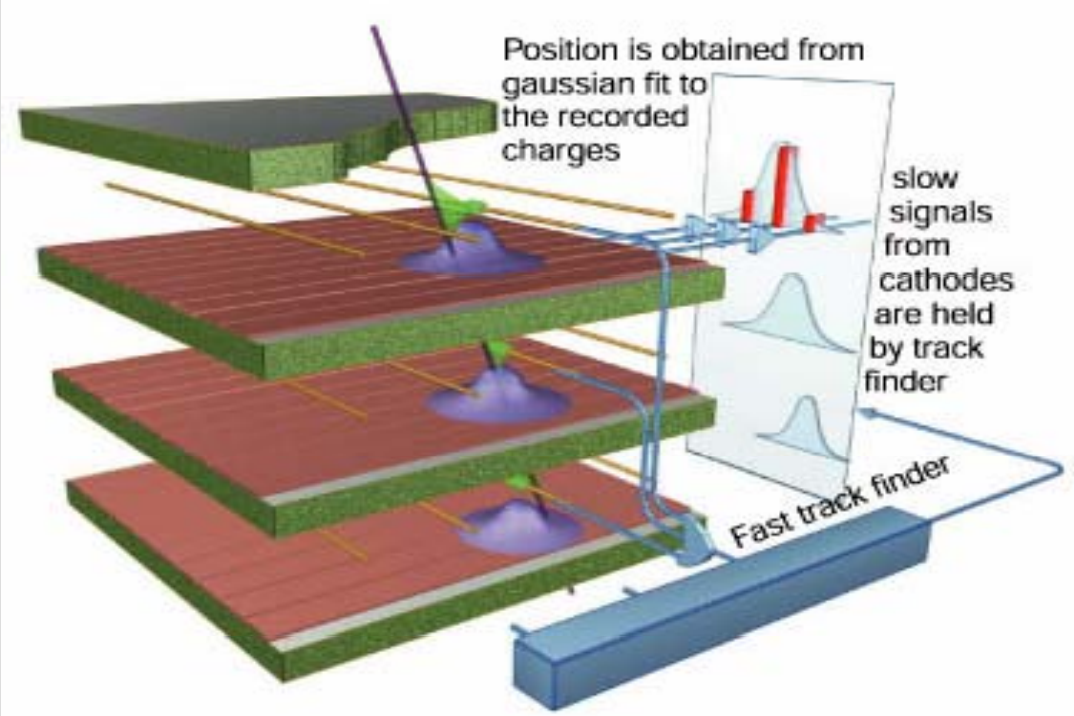
CERN, Geneva, Switzerland; France

Introduction: Cathode Strip Chambers (CSC)

- 6-layer trapezoidal chambers
- Radial cathode strips
- Azimuthal anode wires
- Induced charges on strips - precise φ coordinate
- Closely spaced wires - fast timing
- Wires ganged in groups of 5 - 16 for r coordinate



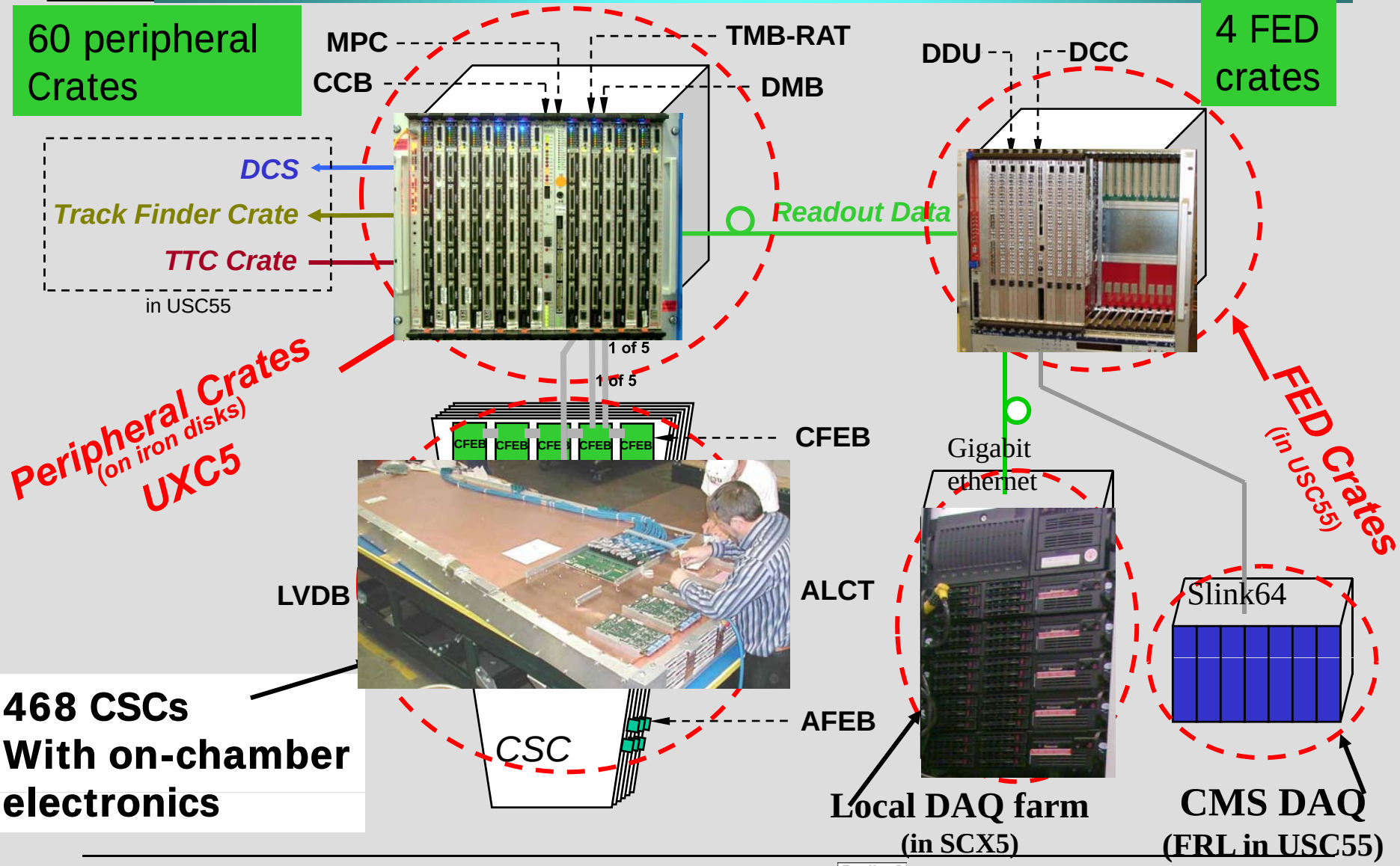




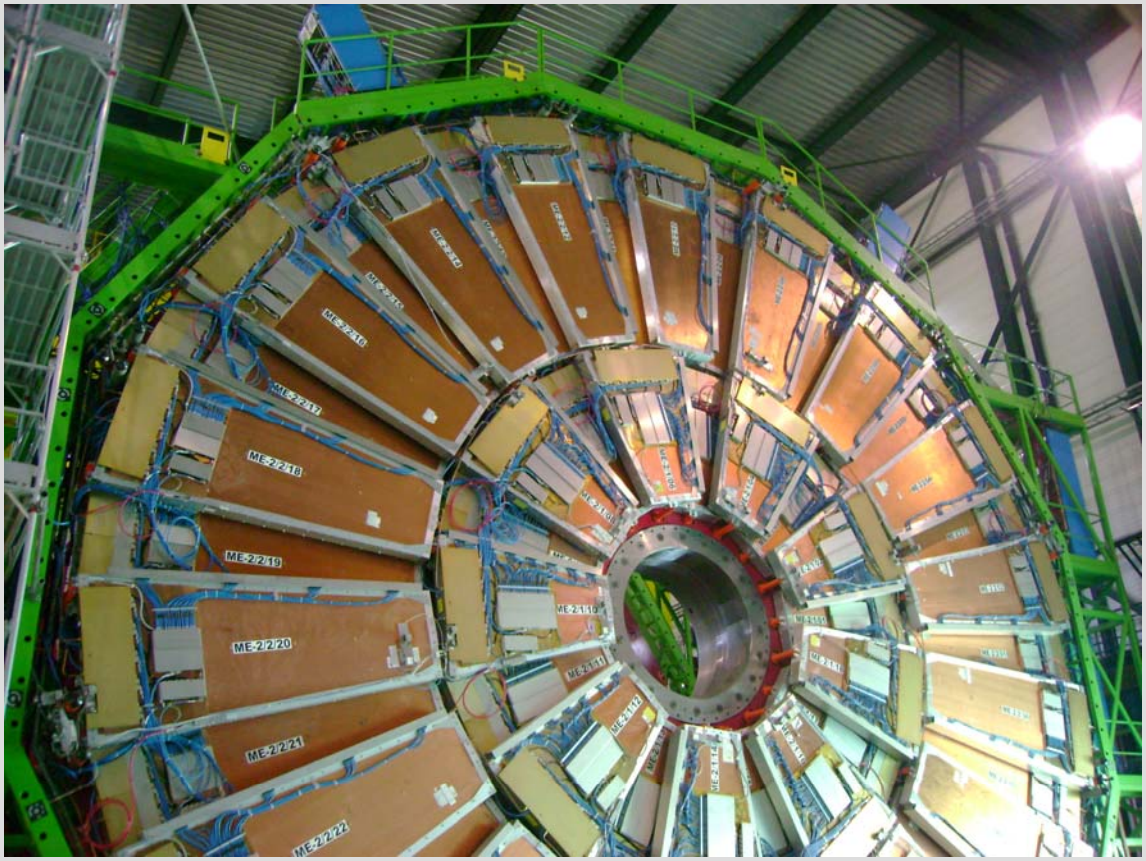
CSC DAQ: General Requirements

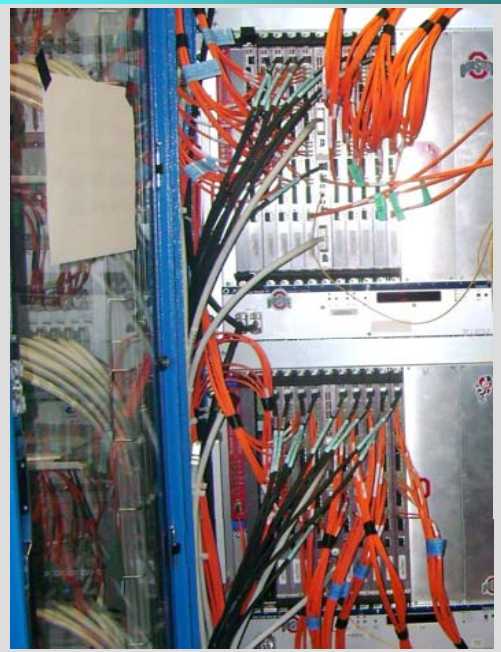
- High precision charge measurement on Cathode;
  ~1%, for 100um resolution with ~cm strip width
- High data rate and high data bandwidth;
  100KHz L1A,
  Upto 70 KHz per strip,
  Negligible dead-time;
  Reliable data transmission over long distance;
- Can withstand radiation levels ($2x10^{12}$ cm^{-2} neutrons, TID of 5 kRad);
- Compact in size for on-chamber electronics;
- Inexpensive on a per channel basis.

CSC DAQ: Electronics layout

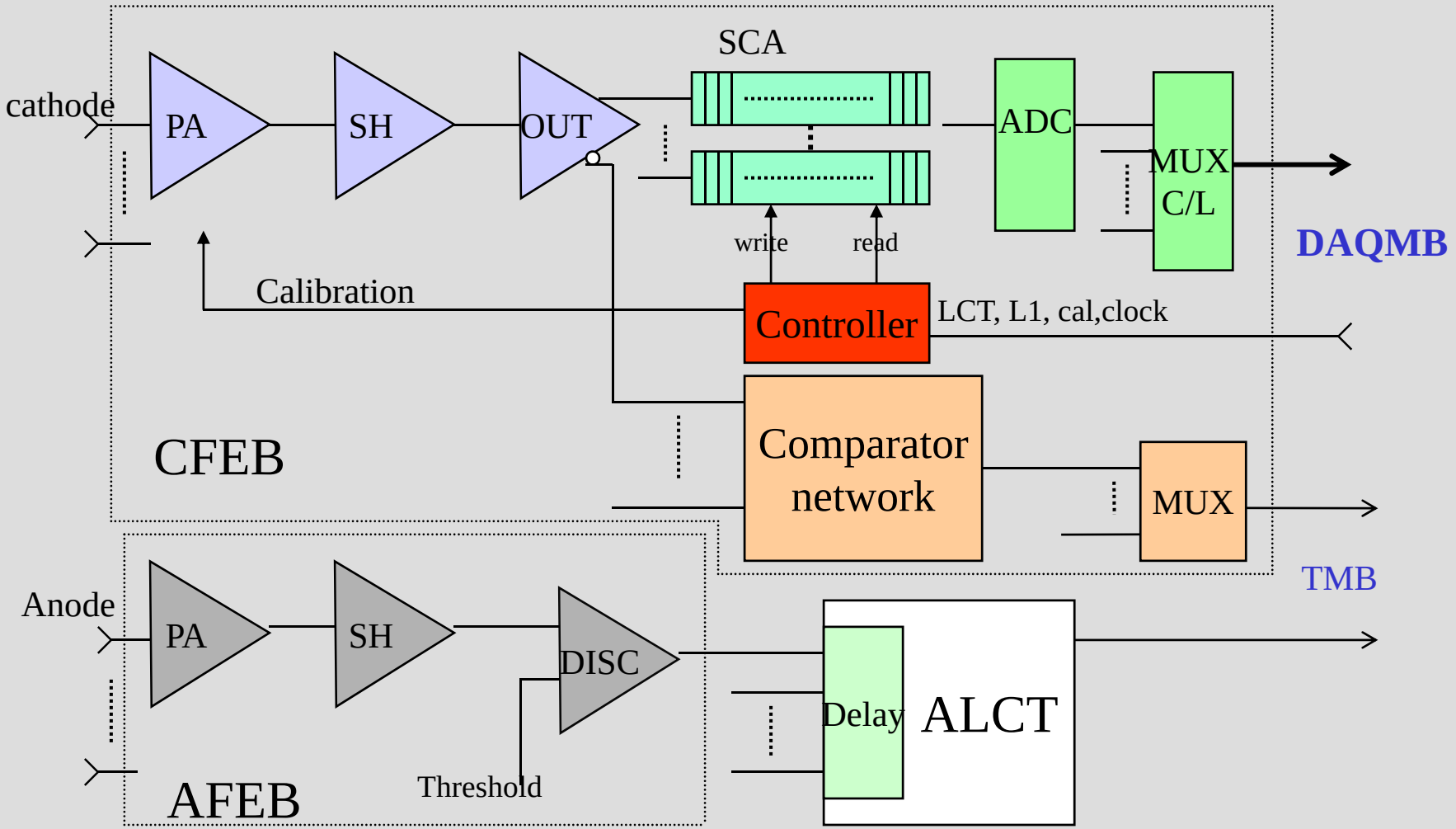


CSC DAQ: Electronics layout

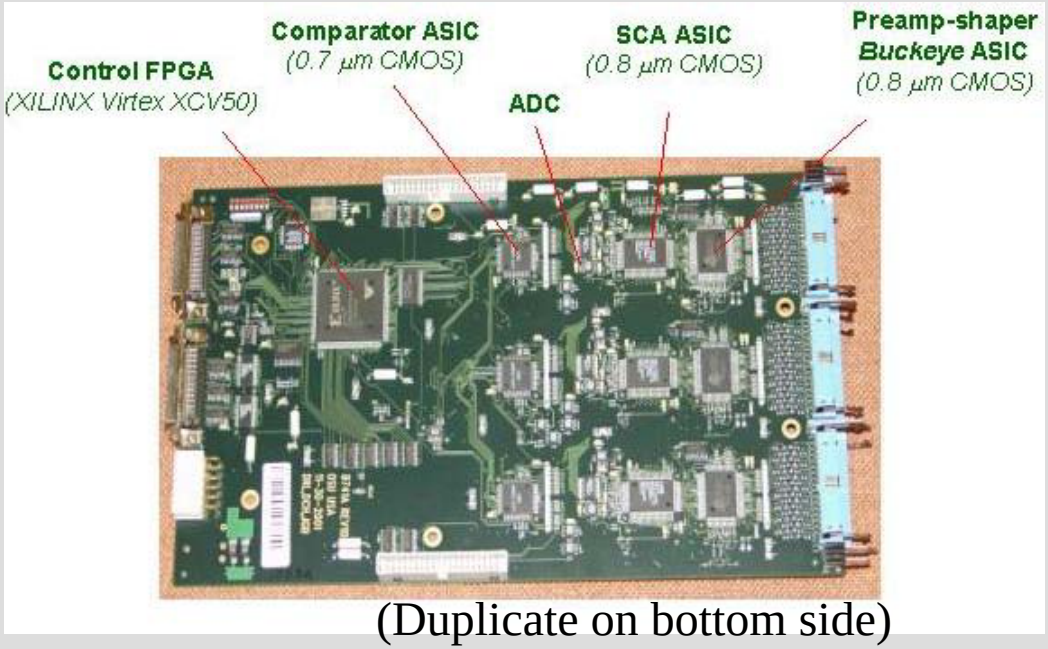




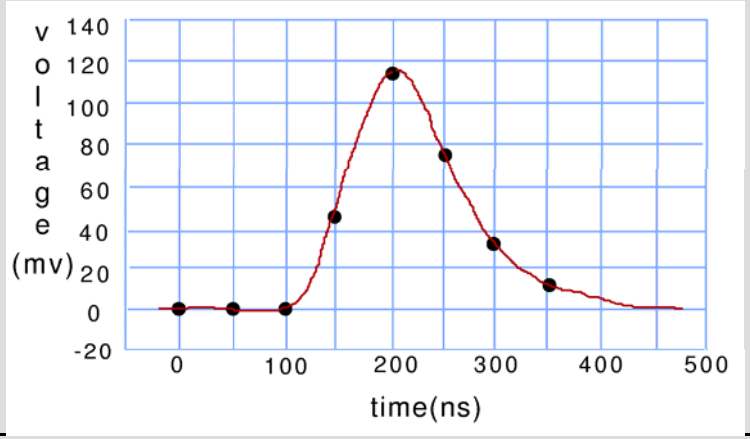
On-chamber electronics: Diagram (CSC readout)



On-Chamber Electronics: Cathode Front-End Board (CFEB)



(Duplicate on bottom side)



Function:

- 96 channel low noise amplifier and analog storage;
- High speed, high precision digitization

Requirements:

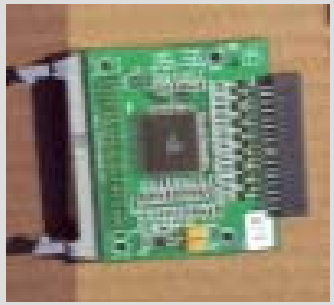
- signal/noise: 100/1
- peaking time of shaped pulse: 100 ns
- digitization precision: 12 bits
- dynamic range: 15 MIPs
- non-linearity: < 1%
- Dead time free for normal run

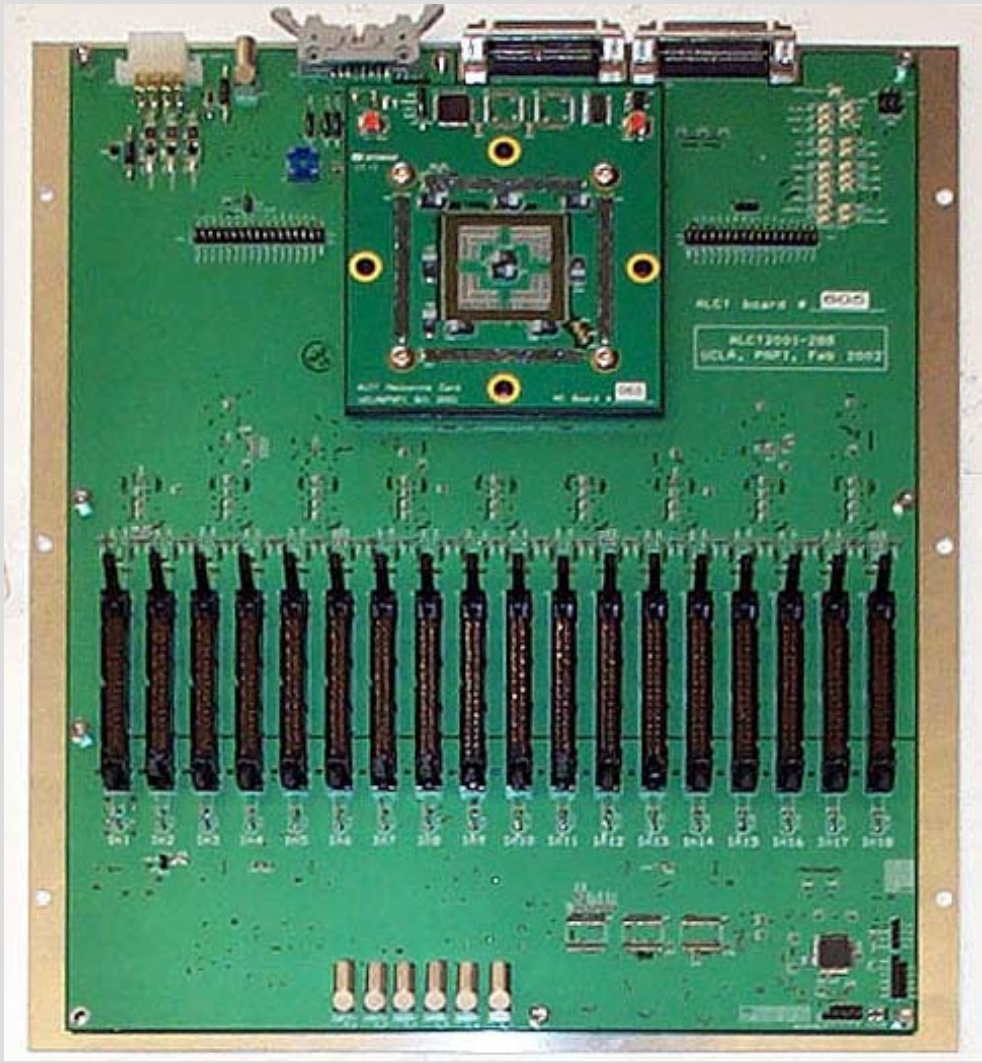
ASICs:

- Six 16-channel shaper/amplifier
- Six 16-channel 96-cell SCA
- Six 16-channel comparator

2268 CFEBs mounted on CMS
On 468 Chambers

On chamber electronics: AFEB and ALCT

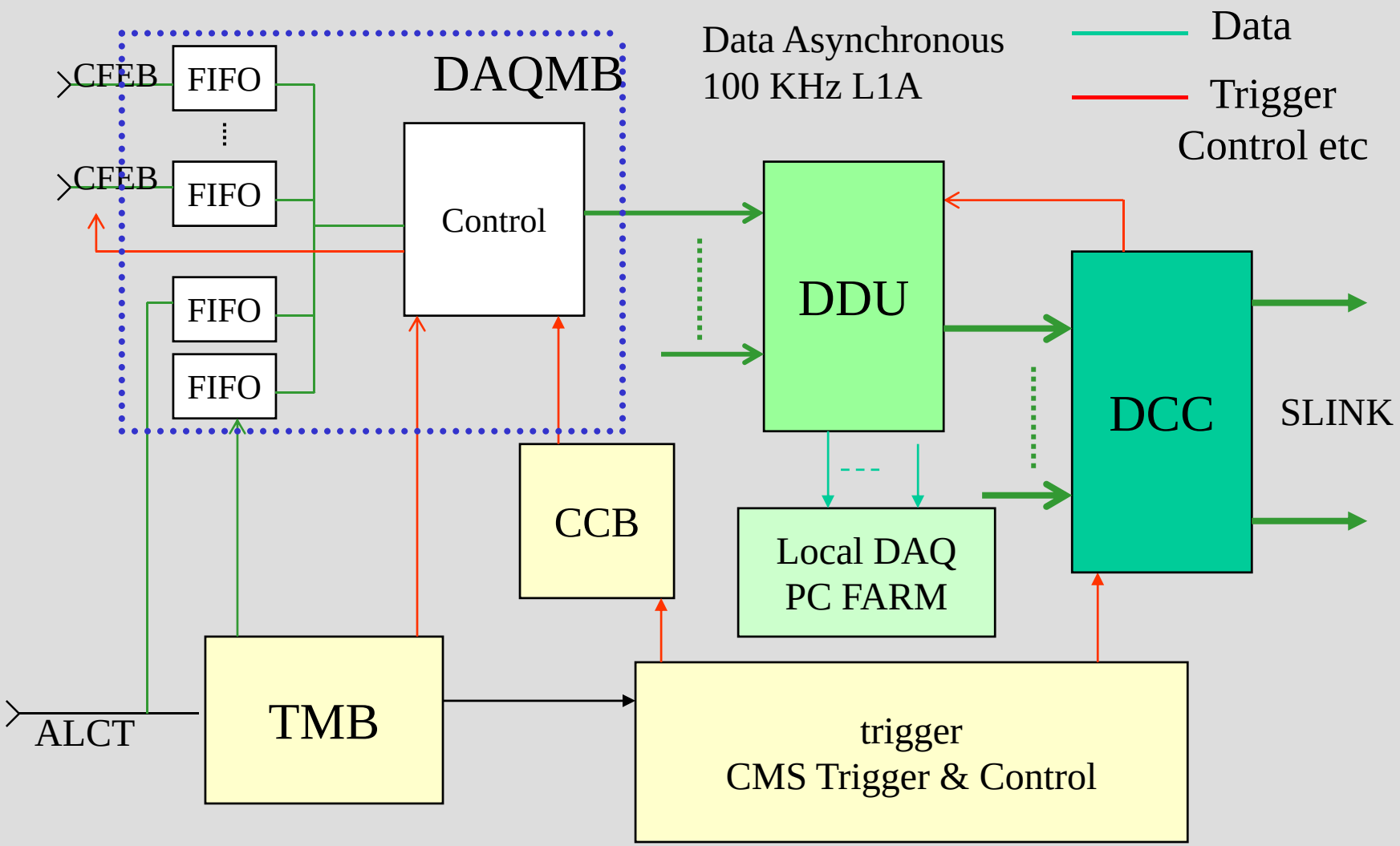




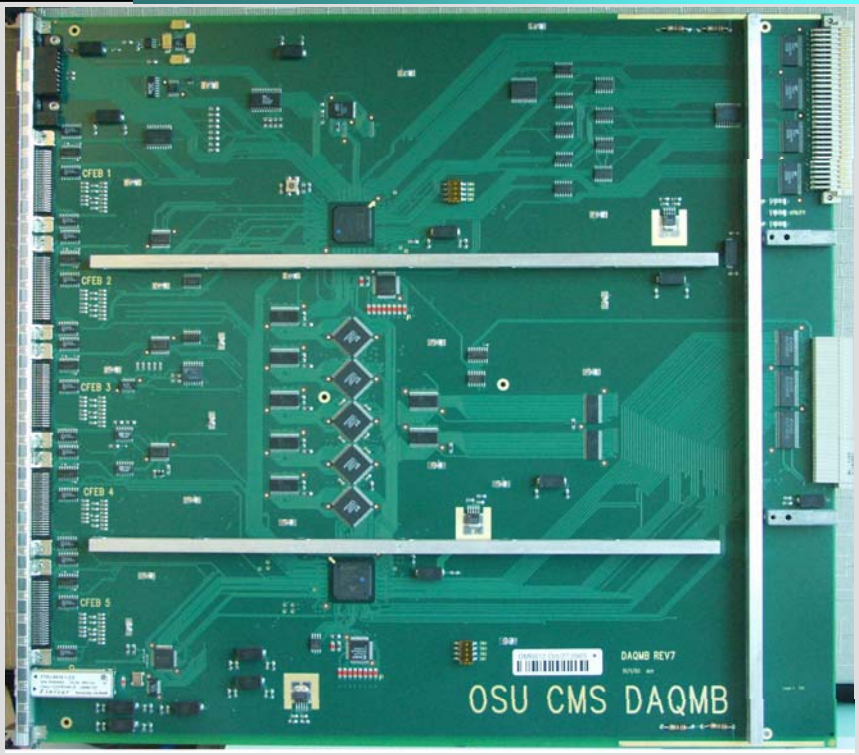
- Amplify, discriminate and delay the anode signals
- Output to ALCT boards for trigger
- Readout through ALCT when ALCT match with L1A

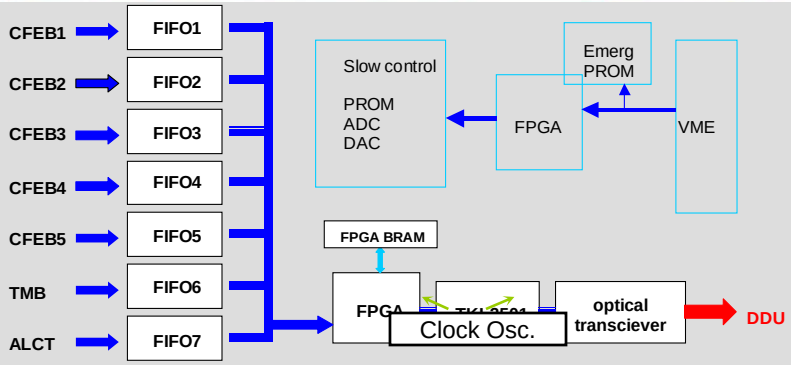
11,448 AFEBs &
468 ALCTs mounted on CMS

Off-chamber electronics: Diagram (Periphery & FED)



Periphery: DAQ Motherboard (DAQMB)





9Ux400mm VME boards

Function:

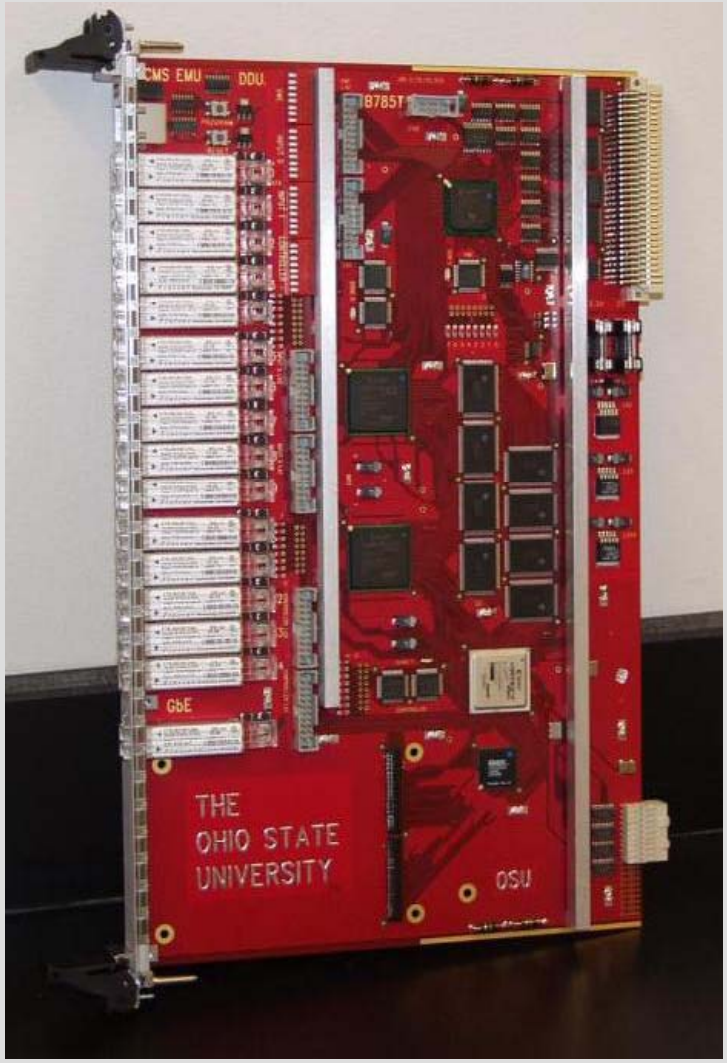
- Receive, assemble and send data;
- Initiates CFEB digitization and readout;
- CFEB calibration;
- Slow control (VME → JTAG)
- LV monitoring VME interface

COTS:

- Seven IDT 18-bit FIFO
- Two XILINX FPGA
- Five channel link
- Four serial ADC
- One optical transceiver

468 DAQMBs mounted on CMS In 60 Peripheral Crates

FED Electronics: DDU Board



9Ux220mm VME boards

Functions

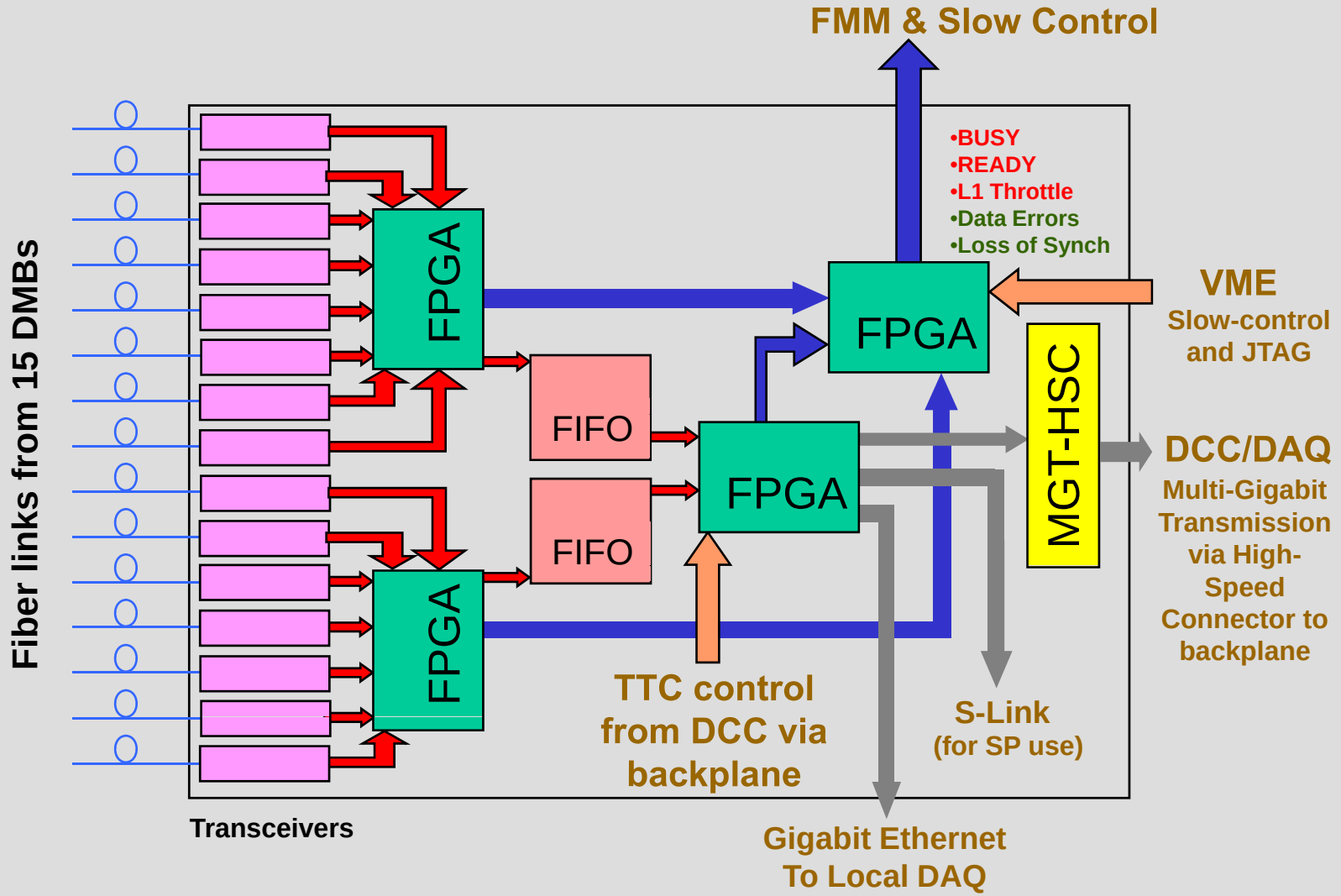
- Merge data from 13 DAQMB's
- Send data to DCC / SLINK
- Send data to local farm
- first 'safe' place to perform on-line error checking and status monitoring (CRC, word count, L1 number, BXN, overflow, link status)
- Error logging and VME interrupt
- Communicates: aTTS, sTTS

COTS:

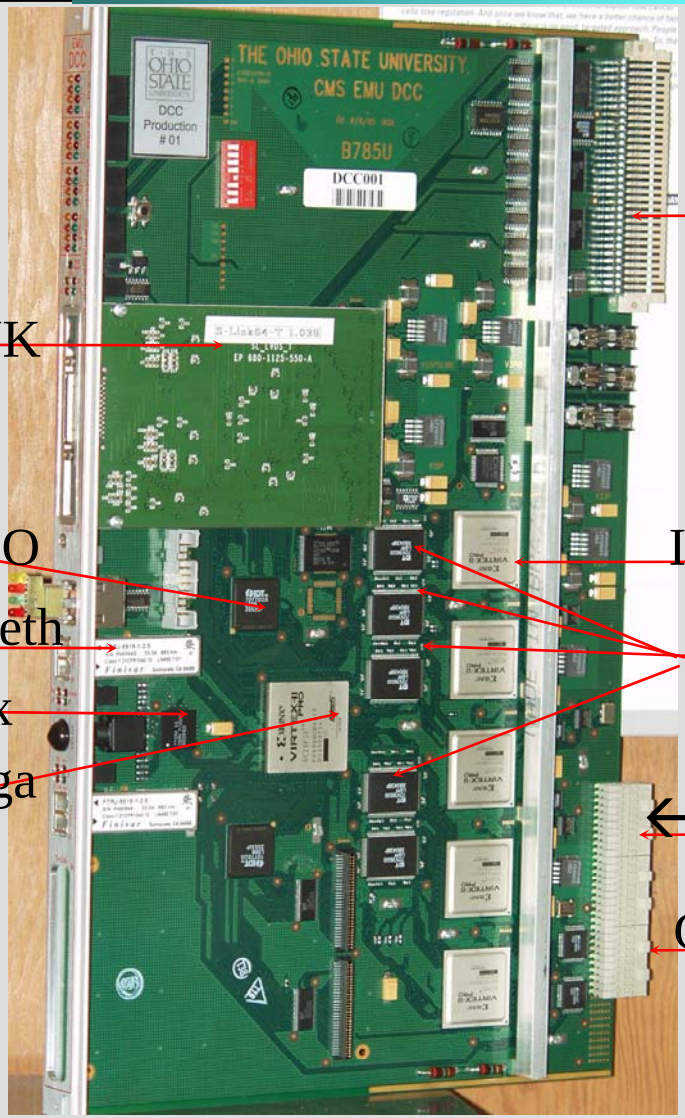
- Two XC2VP20 for Input and fast buffer
- One XC2VP7 for outputs
- 8+1 deep FIFO for main buffer (>2000 events)

36 DDUs mounted on CMS in 4 FED crates

FED Electronics: DDU Diagram



FED Electronics: Data Concentrator Card (DCC)



9Ux220mm VME boards

Function:

- Collect up to 10 DDU data, assemble the data into events, and send to Slink (CMS readout);
- Fan out TTC control to the FED crate;
- EMU DAQ data flow control

Some features:

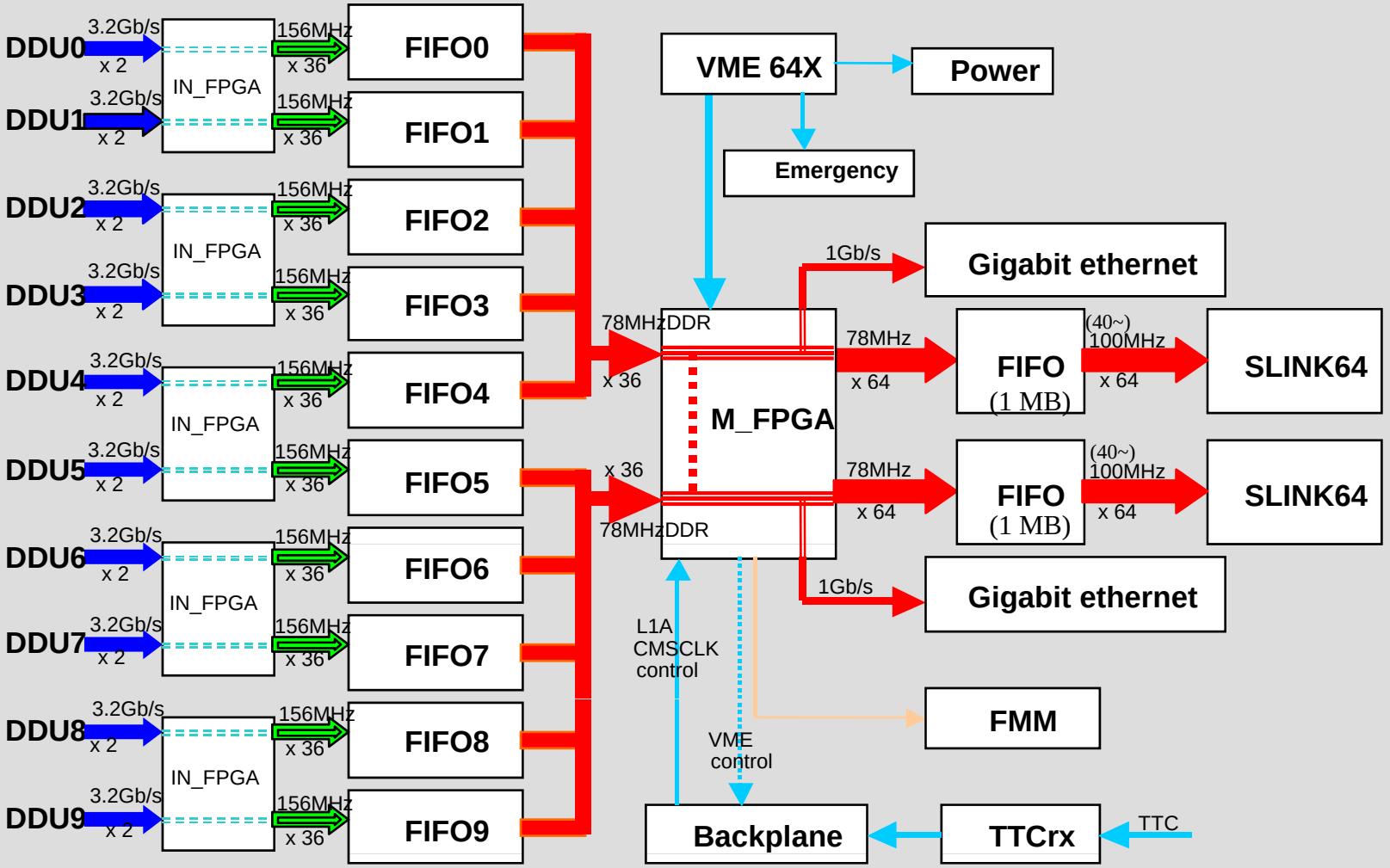
- DDU in 625 Mbyte/s each
- Data processing 625 Mbyte/s *2
- Output (upto) 800 Mbyte/s *2
- Two Fiber Gigabit Ethernet

COTS:

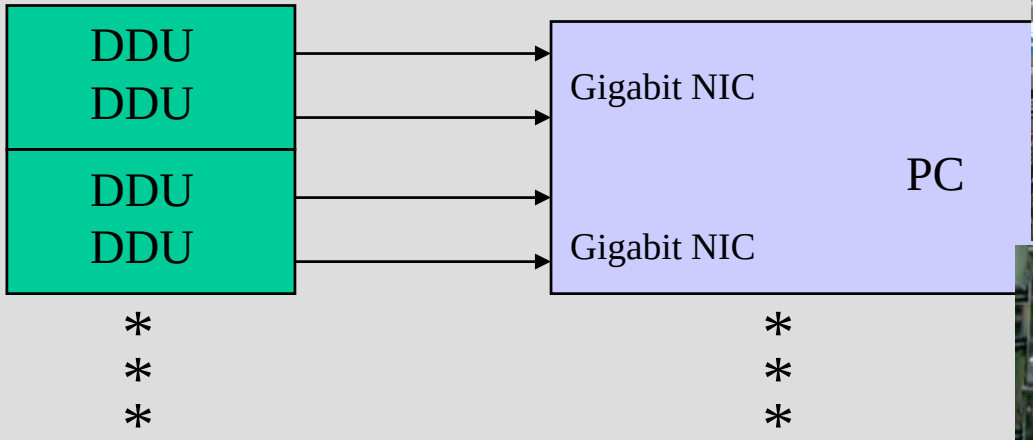
- Xilinx virtex2-pro FPGA
- IDT FIFO (hold ~2,000 events)

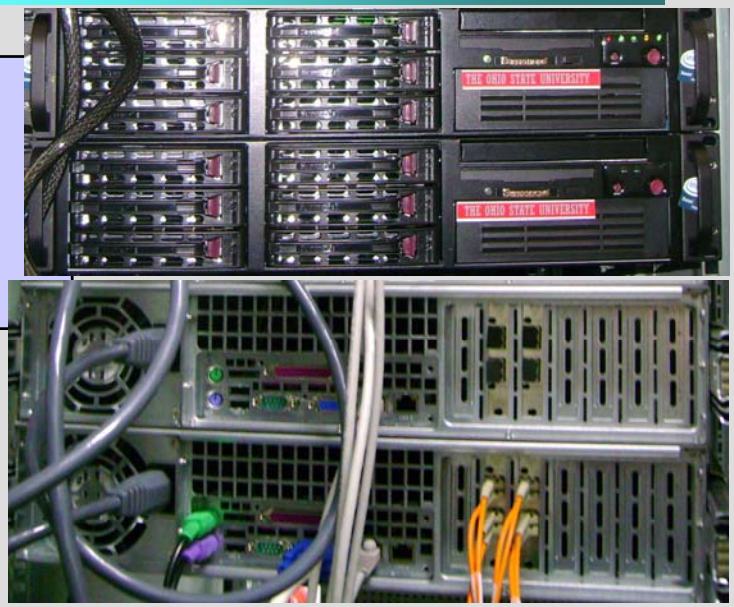
4 (8) DCCs mounted on CMS
In 4 FED crates

FED Electronics: DCC Diagram



Local DAQ Farm: Local DAQ farm interface





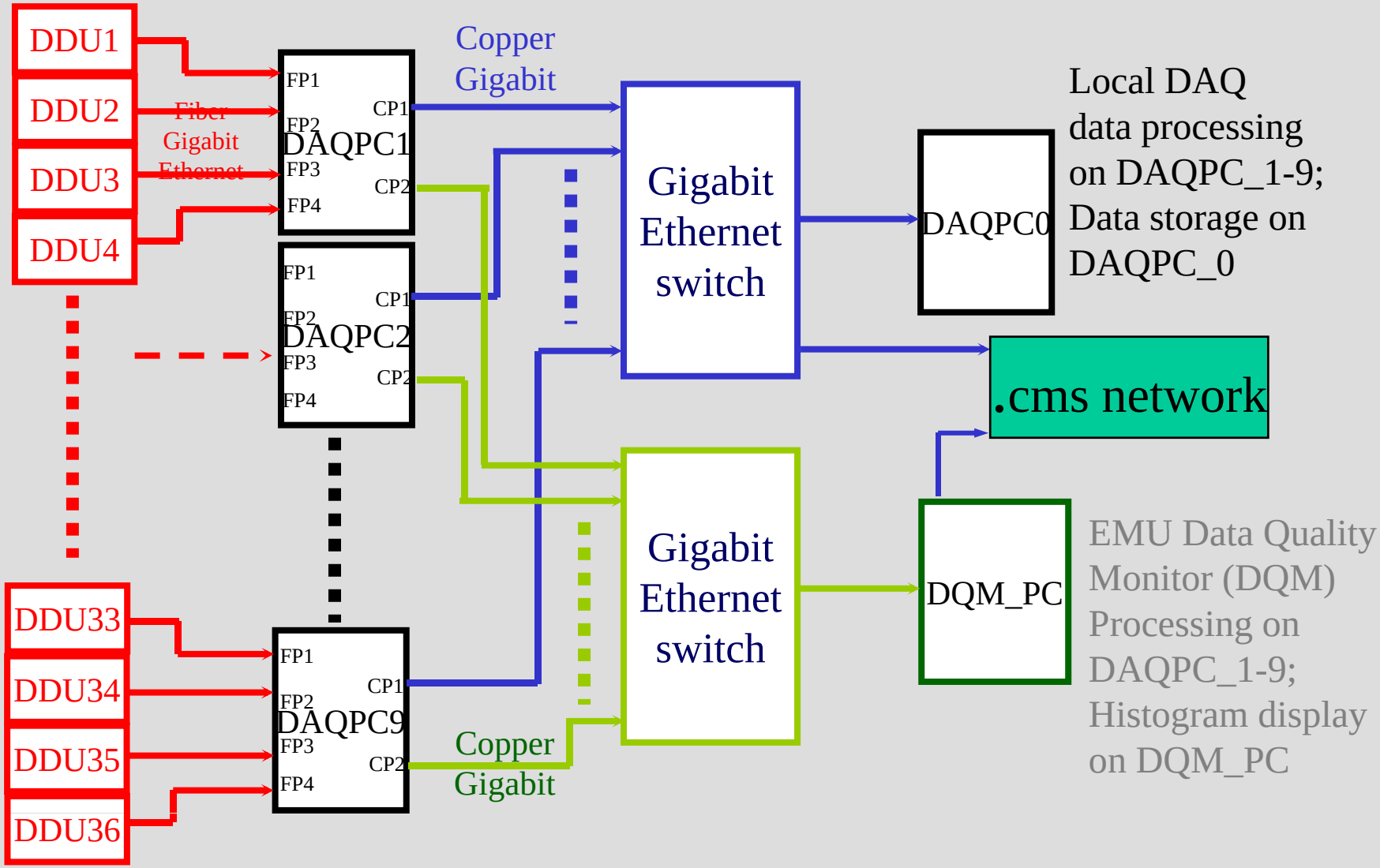
Usage:

- CSC Calibration;
- Data readout:
  - o EMU system debug;
  - o Independent of CMS readout system;
  - o Data sampling and data quality monitoring.

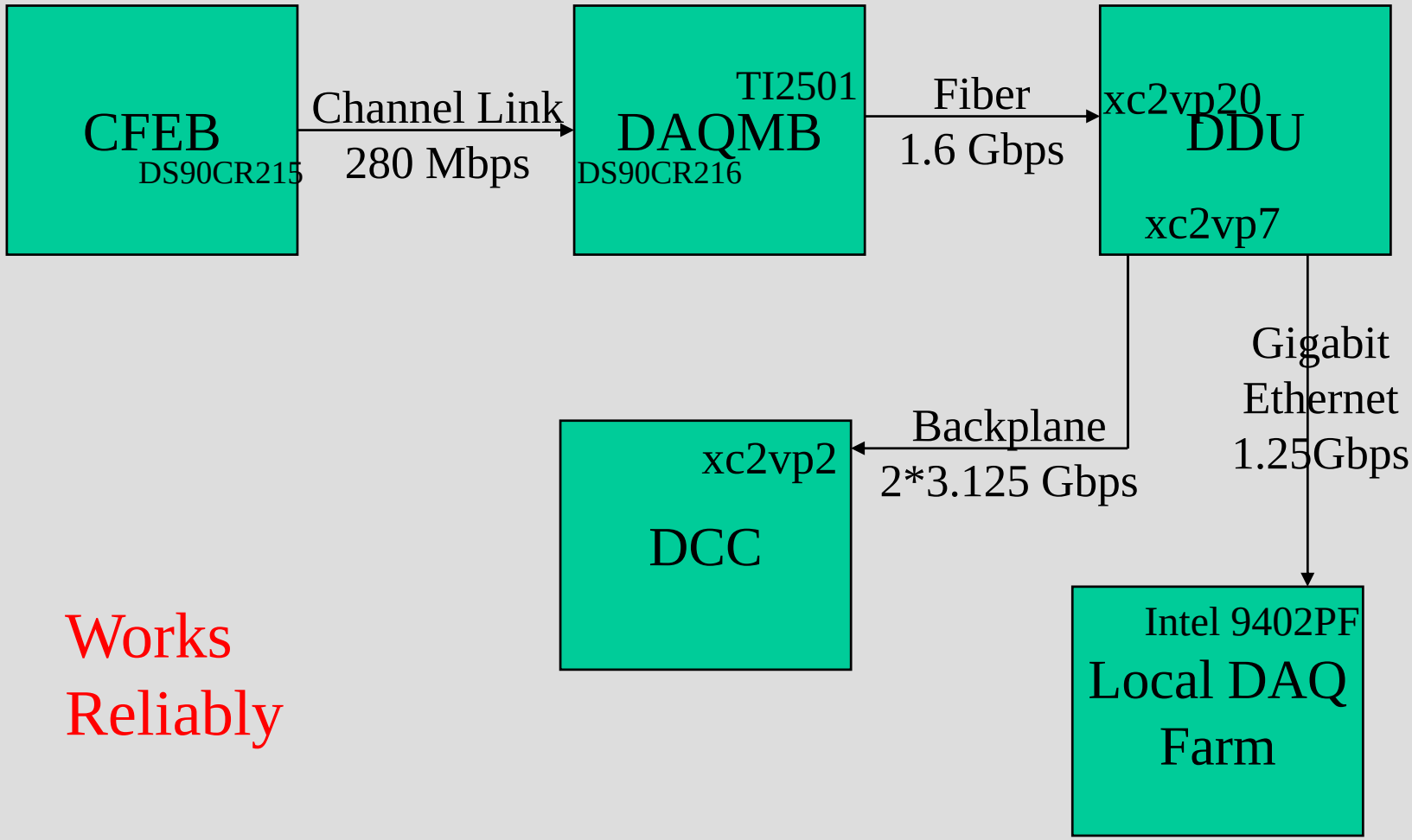
Hardware:

- 10 SuperMicro X7DBE;
- Two Intel dual-core, hyperthreading XEON CPUs;
- Two Intel Dual-port fiber PCI-express, direct connection with MCP.

Local DAQ Farm: Connections

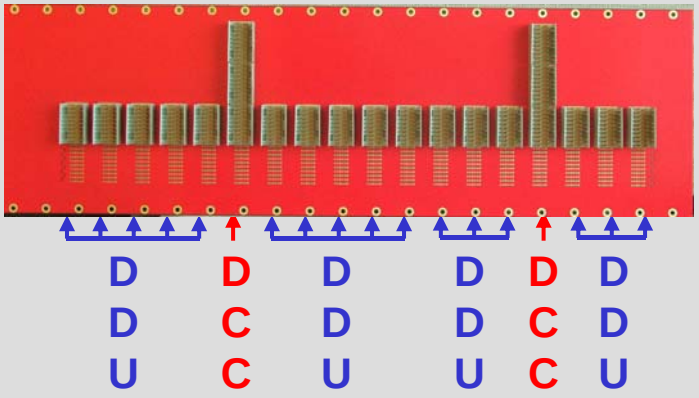


CSC DAQ: interconnect



Works
Reliably

CSC DAQ: Front-End Driver (FED) Crate



Requirement:

- output ~200MByte/s on SLINK
- Input 468 fiber
- output: baseline 1.5 Gbyte/s
- Flexible configuration
- High speed data transmission

Design:

- Four FED crates, Standard VME64x J1 , custom J3 backplane
- Nine DDU, one or two DCC per crate, (13 DMB → DDU, DCC → 2 SLINK)

Various (flexible) concentration ratios:

9 DDU to 1 SLINK	-	EMU data on 4 SLINK
5 / 4 DDU to 1 SLINK	-	**8 SLINK**
3 / 2 DDU to 1 SLINK	-	16 SLINK
1 DDU to 1 SLINK	-	36 SLINK

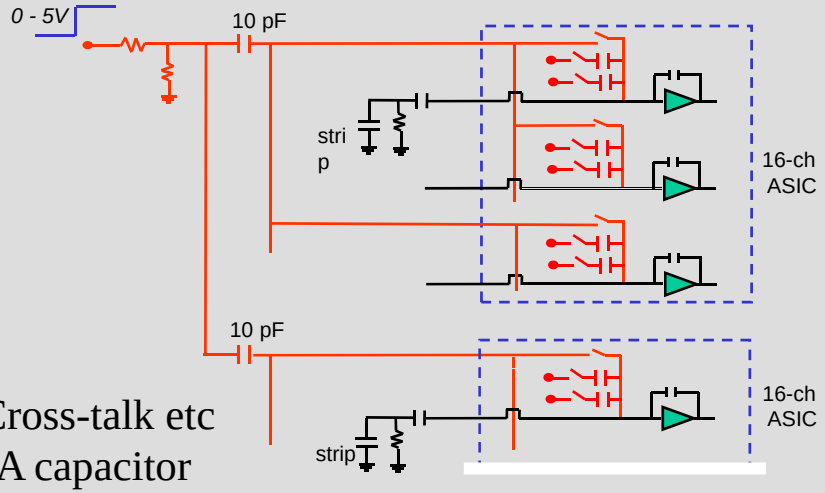
CSC DAQ: General issue I: Calibration

Cathode Calibration:

Amplifier ASIC on CFEB has internal shift register which controls calibration

JTAG Shift Register Modes

- Normal
- Precision Ext. Cap (<1%)
- Int. Cap Small (1x)
- Int. Cap Medium (2x)
- Kill



Buckeye Calibration:

→ Gain, Linearity, Noise, Cross-talk etc

→ Dead channel check, SCA capacitor pedestal and noise,

Anode Calibration:

- Test pulse (by ALCT cards) on the built-in amplifier input capacitor
  - Determine the threshold and the delay setting
- Pulse a spare strip and fires all channels of AFEB
  - quick dead channel check etc

The calibration constant will be saved in a central area, and applied on offline analysis

CSC DAQ: General Issue II: Sync & zero suppress

- CSC daq synchronization

  Event transfer are synchronized with Level_1_trigger, marked with Level_1_trigger number and beam crossing number. On the Slink data, the DCC also pack the orbit-counter number:

  – CFEB/ALCT/TMB send Data_Available mark with/out data on every Level_1_trigger;

  – DAQMB/DDU/DCC send data on every Level_1_trigger, book keeping with FIFO

- Zero suppression;

  – CFEB/DAQMB level: Local_Charged_Track matches with Level_1 trigger

  – DDU level: Only the DAQMB with data are passed on.

CSC DAQ: General Issue III: Data Integrity

- Data integrity check

Parallel CRC for data integrity check (first hardware implementation);

Why? High speed data transmission; Serializer and de-serializer; Radiation (SEU).

•History: Early 1999: First parallel CRC implementation on CFEB

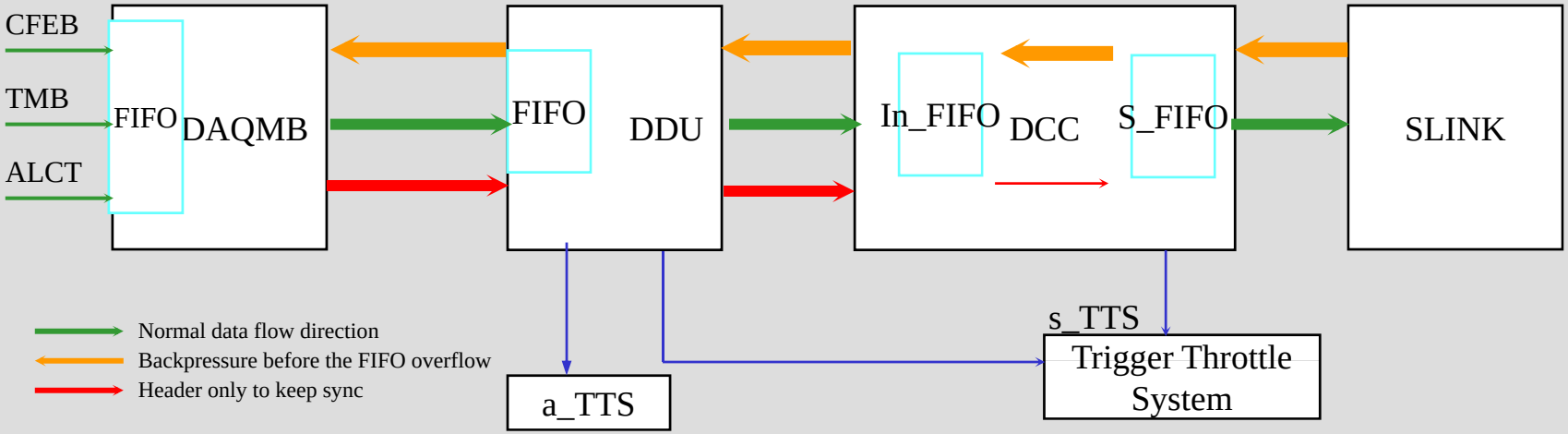
40 MHz / 13-bit data / 15-bit CRC; Later: DAQMB data:

80 MHz / 16-bit data / 22-bit CRC; 2003: CMS SLINK standard

125 MHz / 64-bit data / 16-bit CRC

CSC DAQ: General issue IV: Backpressure

•Backpressure;



Both DDU and DCC can send signals to Trigger Throttle System to reduce trigger rate

When Slink is full, the DCC will stop sending data to Slink, the data will be buffered at the DCC S_FIFO,

When the DCC S_FIFO is 'Almost_full', it will stop the DCC data processing. The data will backup on the IN_FIFO;

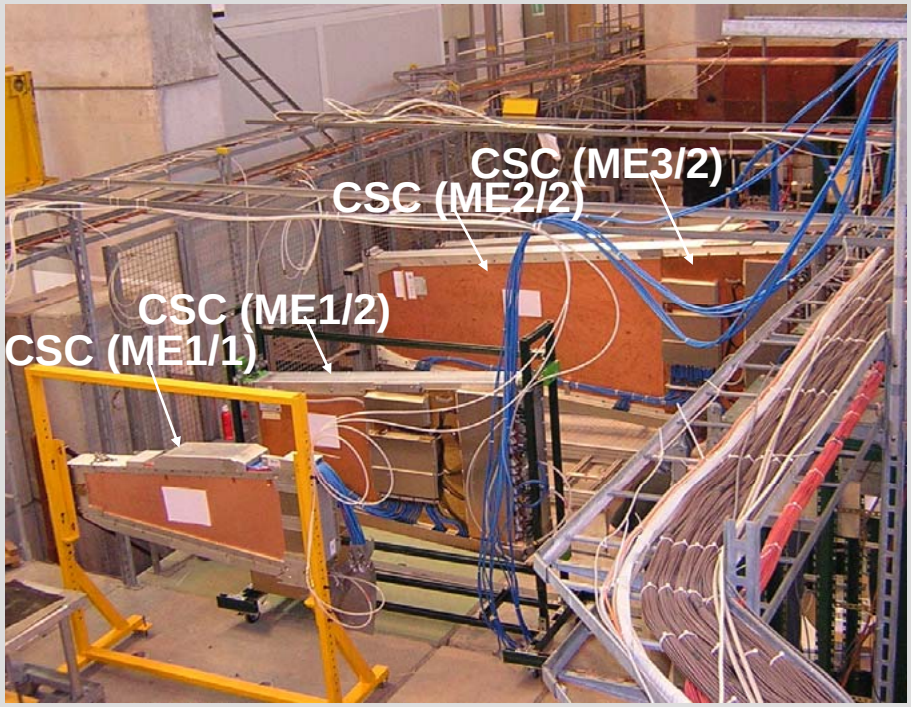
When the IN_FIFO gets to a certain level, it will backpressure on DDU, the DDU will stop, data will be backup;

When DDU FIFO gets to a certain level, it will backpressure the DAQMB;

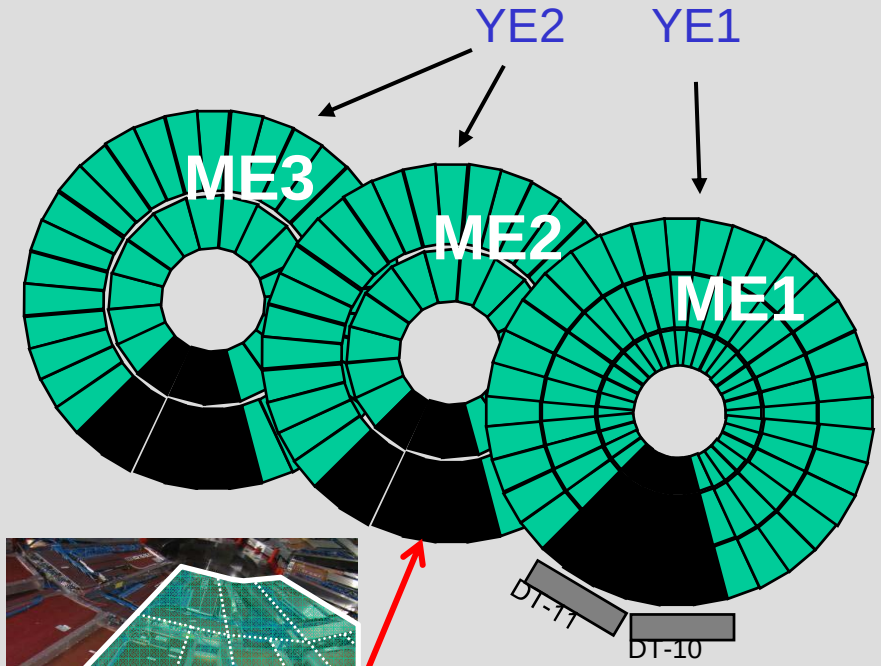
DAQMB can also disable the trigger sending to CFEB, or ignore the backpressure in case the DAQMB FIFO close to full;

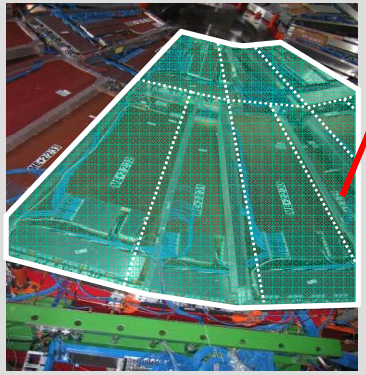
DCC can dump the data, retain the header to keep sync if DDU ignore the backpressure

System Test: Beam test & MTCC system test



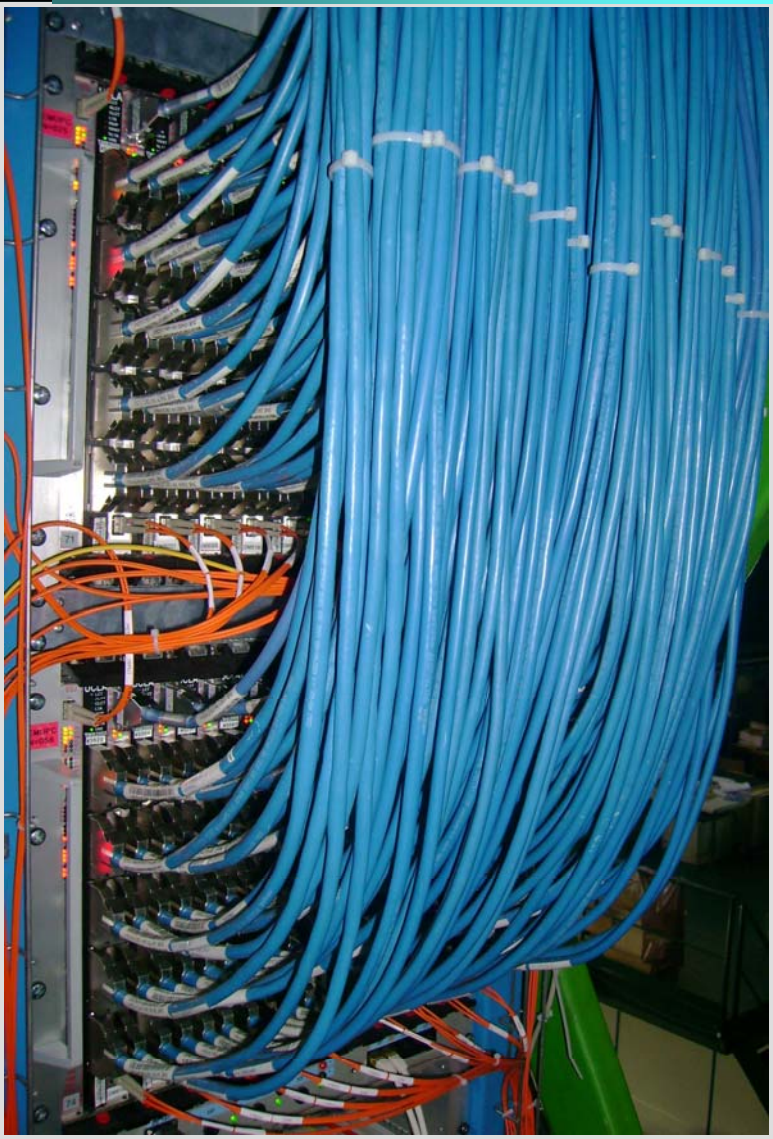
LHC-similar structured beam test
1998, 1999, 2003, 2004 at CERN



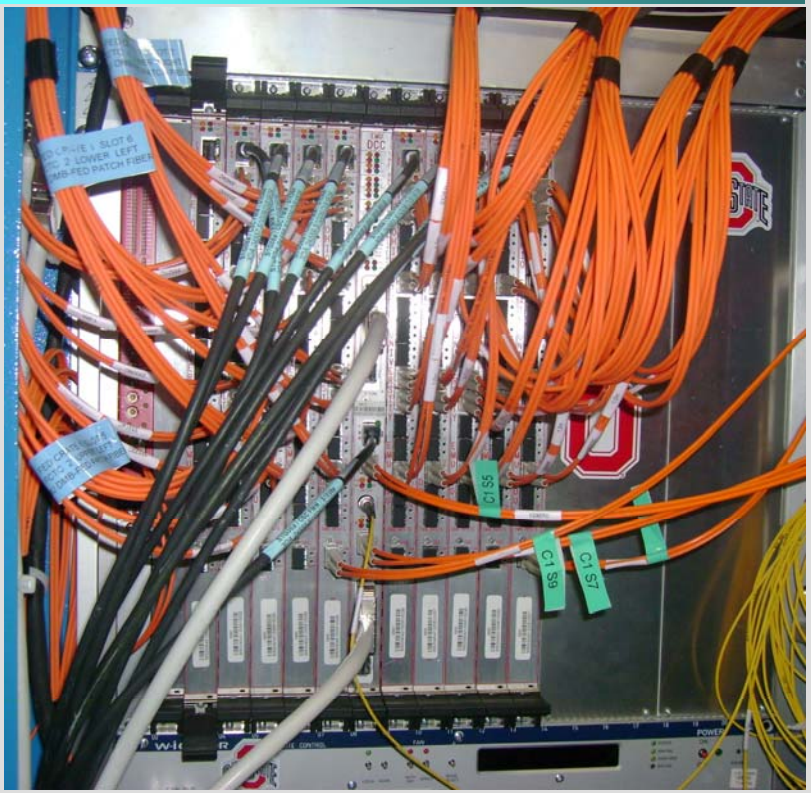


CSC Slice test: 36 CSCs participated
Full system chain execised

System Test: Beam test & MTCC system test

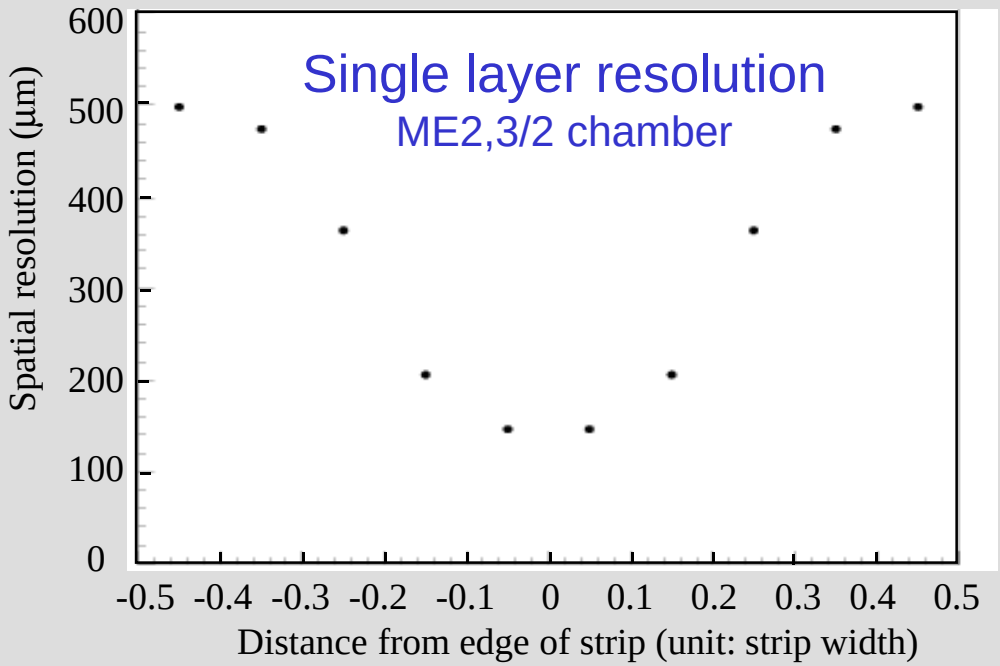


Peripheral crates



DDU/DCC
In FED crate

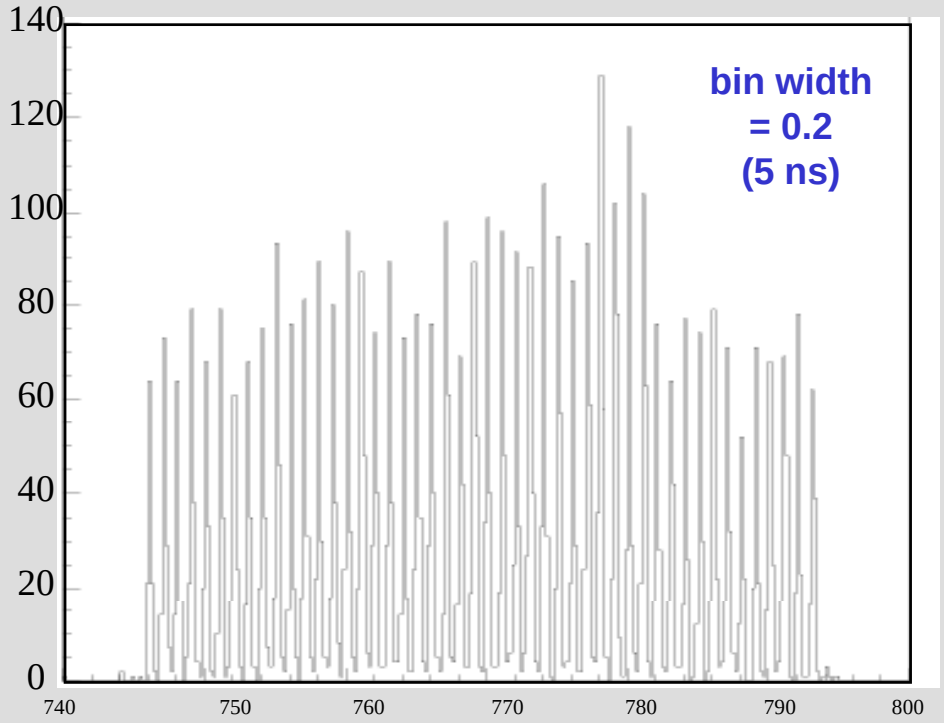
System Test: Cathode strip spatial resolution



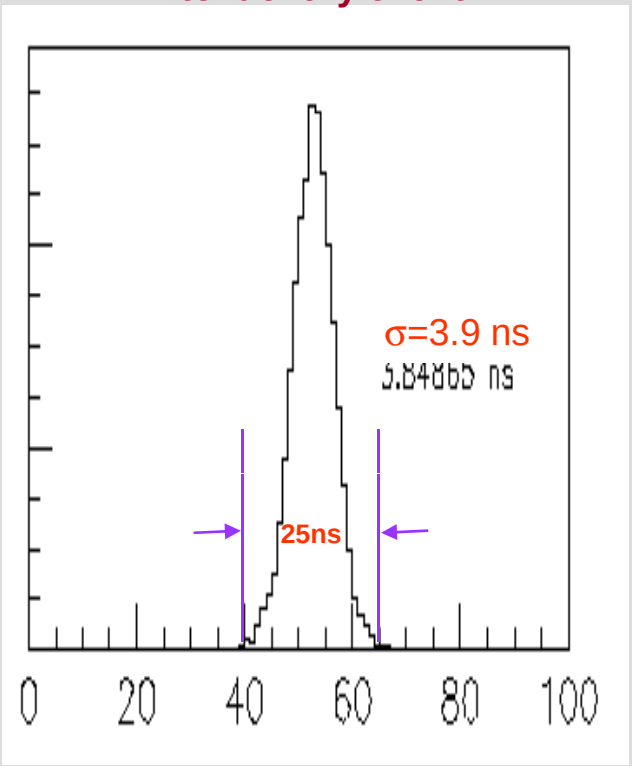
- Resolution is best for hit near the edge of strip, worst at the center.
- In a CSC, the 6 layers are staggered alternately by ½ strip width. The combined resolution is ~ 100 μm per chamber

System test result I: Timing resolution

Cathode pulse timing (6 layer average) relative to L1A (beam scintillators)



Anode timing can be used to identify event

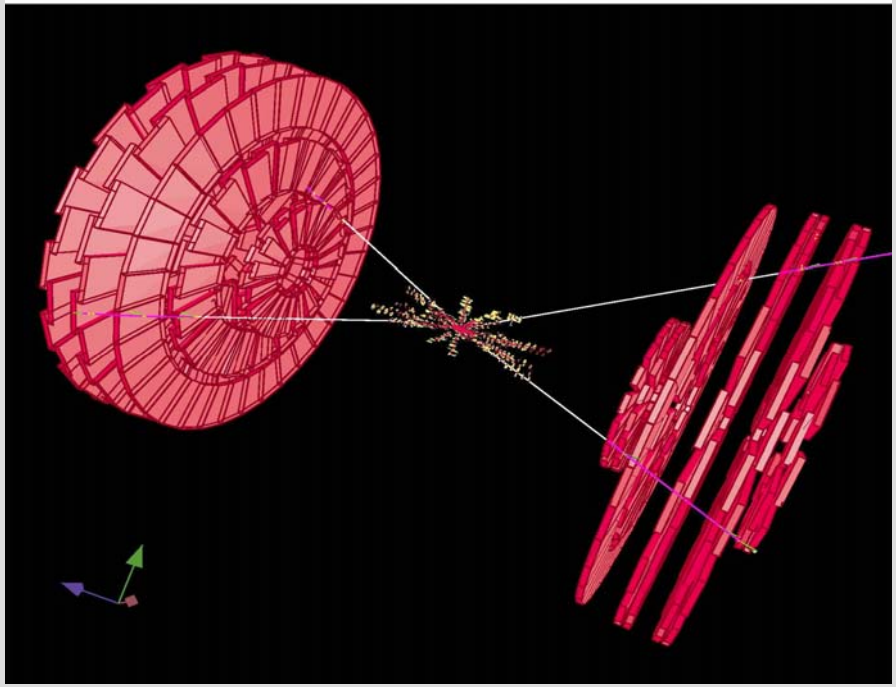


System Test result II: Rate test

- EMU DAQ system (CFEB → DAQMB → DDU → DCC) works reliably at the designed trigger rate (100 KHz L1A and >100 KHz LCT trigger rate);
- Event synchronization tested at >100 KHz random trigger rate,
- The CFEB, DAQMB and DDU works (tested) at more than five times the expected LHC data rate;
- DCC to SLINK achieved 240 Mbyte/s average data rate (requires 200 Mbyte/s);

Summary: Current status & Summary

- ✓ Time-structured beam at CERN:
  - Integrated EMU Data acquisition system with multiple CSC's successfully tested several times in 25 ns.
- ✓ MTCC at CERN:
  - Successful; Satisfies or surpasses the design requirements.
- ✓Electronics
  - Production finished
  - Electronics installed



➢Commissioning progressing

FED integrated with CMS;

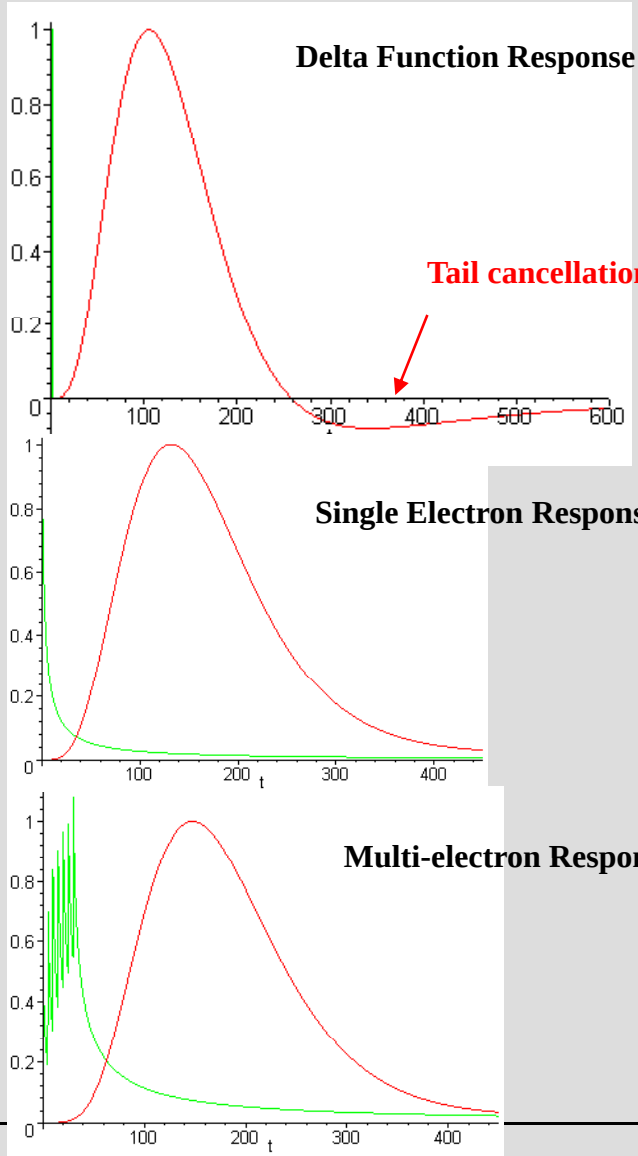
Local DAQ: up and running

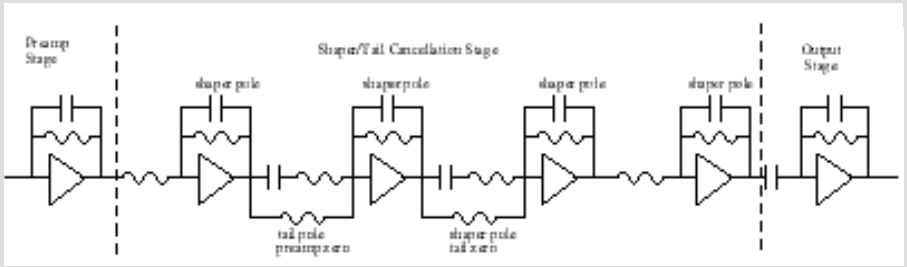
4 Peripheral Crate, 18 CSCs lighted up last week !

System will be ready for LHC collision in 2008

Thank you !

On chamber electronics: Buckeye Amplifier/Shaper ASIC





0.8 μm AMI CMOS with Linear Capacitor

- 2 outputs per strip:
  - 1 trigger path, 1 DAQ path
- 5 pole semigaussian
- 1 pole 1 zero tail cancellation
- 100 nsec peaking time (delta function)
- 170 nsec peaking time (real pulse)
- Gain .9 mV/fC
- Equivalent Noise 1 mV
- Nonlinearity < 1 % at 17 MIPS
- Rate 3 MIPs at 3 MHz with no saturation
- Two track resolution 125 nsec