The Cathode Strip Chamber Data Acquisition System for CMS

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Abstract

The Cathode Strip Chamber (CSC) [1] Data Acquisition (DAQ) system for the CMS [2] experiment at the LHC [3] will be described. The CSC system is large, consisting of 218K cathode channels and 183K anode channels. This leads to a substantial data rate of ~1.5GByte/s at LHC design luminosity ($10^{34}cm^{-2}s^{-1}$) and the CMS first level trigger (L1A) rate of 100KHz. The DAQ system consists of three parts. The first part is on-chamber Cathode Front End Boards (CFEB)[4], which amplify, shape, store, and digitise chamber cathode signals, and Anode Front End Boards (AFEB)[5], which amplify, shape and discriminate chamber anode signals. The second part is the Peripheral Crate Data Acquisition Motherboards (DAQMB), which control the on-chamber electronics and the readout of the chamber. The third part is the off-detector DAQ interface boards, which perform real time error checking, electronics reset requests and data concentration. It passes the resulting data to a CSC local DAQ farm, as well as CMS main DAQ [6]. All electronics in the system employ FPGAs allowing programmability. In addition, several high-speed serial interface technologies are employed.

I. Introduction

CMS is one of the major experiments on LHC at CERN. First data is expected to be taken in the summer of 2008. At the heart of CMS sits the 13 meter long, 6 meter in diameter, 4 Tesla superconducting solenoid. The bore of the magnet coil is large enough to accommodate the silicon inner tracker, lead tungstate ($PbWO_4$) crystal EM calorimeter, and the brass/scintillator sampling hadron calorimeter. The return magnetic field saturates 1.5 meters of surrounding iron, interspersed with 4 muon 'stations'. Each muon station consists of several layers of aluminium drift tubes in the barrel region and cathode strip chambers (CSC) in the endcap region, complimented by resistive plate chambers.

There are in total 468 CSCs, forming eight disks covering the two endcaps. Figure 1 displays the third disk of CMS plus-side endcap. Each CSC is trapezoidal in shape and consists of six gas gaps, each gap having a plane of radial cathode strips and a plane of anode wires running perpendicularly to the strips. The gas ionisation, drift, electron avalanche, and subsequent avalanche ion drift caused by a charged particles traversing each plane of the chamber produces induced charges on the anode wire and on a group of cathode strips. The signal on the wires is fast (σ ~3 nsec) and is used in the Level-1 Trigger timing determination. However, it leads to a coarser position resolution. A precise position measurement is made by determining the center-of-gravity of the charge distribution induced on the cathode strips. Each CSC measures up to six space coordinates. The spatial resolution provided by each chamber from the strips is typically 100 μm. The angular resolution in φ is of order 10 mrad.

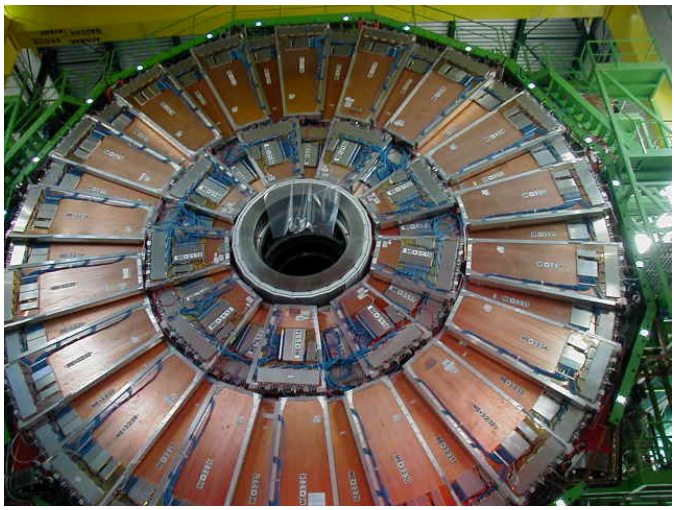

Figure 1: ME+3 CSCs

II. Description of CSC DAQ System

In this section, the CSC DAQ design requirements, hardware, system calibration and error monitoring are introduced.

A. Design Requirements/Considerations

According to simulation, the total data rate is about 1.5GByte/s at the nominal LHC luminosity with design CMS L1A trigger rate. Because of the uncertainty of the simulation though, the system should be able to handle larger or smaller data rates, and requires high flexibility.

To achieve cathode position precision of 100 μm using strips of ~1 cm width, this requires cathode charge precision of ~1%. This dictates very low noise amplifiers and front-end boards.

The on-chamber electronics are also required to work in a high magnetic field and moderate radiation environment.

The data are synchronous with the CMS first level trigger signal, L1A. On every L1A, each DCC will send one event packet to CMS global DAQ; each DDU will send one event packet to the local DAQ farm. In the current CMS design,

the DAQMB, DDU and DCC are expected to process event packets at ~100KHz, which is the CMS L1A trigger rate. Each event's data is marked with the L1A number and the beam crossing number for event synchronization check and event assembly.

There is natural zero suppression built into the CSC DAQ system. CFEB data will be readout only when there is a local charged track trigger in coincidence with a L1A. Similarly for the anode readout and the comparator readout. This reduces the front–end readout to less than one KHz per chamber at the 100KHz L1A rate.

The DDU performs further zero suppression. The DMB will not show up in the data stream if there is no CFEB, ALCT and TMB readout in that chamber.

In order to work at high rates, the CSC DAQ system buffers the data at many levels. The CFEB data are buffered in FIFOs on the DAQMB. The DAQMB data are buffered in FIFOs on the DDU, and the DDU data are buffered in FIFOs on the DCC. There is FIFO status monitoring logic built into the electronics. The DAQMB FIFO status is transferred to DDU along with data readout. The DDU and DCC will monitor the FIFO status and set the proper sTTS (Trigger Throttling System) state, informing the TTS to slow down or disable the trigger if necessary. If the trigger rate is still too high, the data will backed up in the DCC, then in succession the DDU and the DAQMB. If the FIFOs at all levels are full, the DAQ system will throw out data in an attempt to keep events synchronized.

With several levels of serializing and deserializing, data bit loss needs to be monitored. The data integrity is checked by parallel CRC at all levels. The first 15-bit parallel CRC logic was implemented on CFEB FPGA in 1999. A 22-bit CRC is used for anode data, comparator data, and DAQMB data. A 16-bit CRC is used by DCC and DDU for slink data transfer. The CRC proved to be very robust, and reliable.

Figure 2 shows the diagram of CSC DAQ electronics.

B. CSC DAQ Hardware overview

1) On-chamber electronics:

The On-chamber electronics consists of Cathode Front End Boards (CFEB), Anode Front End Boards (AFEB) and Anode Local Charge Track (ALCT) boards.

The CFEBs amplify, shape and digitise the CSC cathode strip charge signals. The cathode charge is collected by a precision custom designed ASIC amplifier[7]. The analog data is sampled every 50ns, and stored in a custom designed ASIC Switched Capacitor Array (SCA)[8]. The SCA is controlled by an FPGA and addressed in blocks of eight capacitors. On receipt of a local charge trigger (LCT), indicating that there is a charged track in the chamber, a block of capacitors is saved. If not, the capacitors are marked for reuse. A fixed time later, if a L1A signal arrives, indicating that there is an interesting event in the beam crossing, and an LCT matches with the L1A, the capacitor data is digitised by a 12-bit ADC and passed through skewclear cable to the DAQMB in the peripheral crate. This parallel data is serialized by a channel link device[9] to minimize the size of the skewclear cable. The SCA can buffer at least six full events; at the LHC design luminosity the dead time due to fully occupied SCAs is negligible.

Four to five CFEBs are mounted on each chamber depending on CSC chamber type. There are a total of 2,268 CFEBs in the system. Each CFEB services 96 Cathode strips. There are a total of 218K cathode channels in the complete system.

The Anode Front End Boards (AFEB) amplify and discriminate the anode signals and send logic pulses to a delay ASIC on ALCT boards. The anode has more precise timing information than the cathode signal, and also provides coarse radial position and angle of the passing particle. Twelve to forty-two AFEBs are mounted on each chamber depending on the CSC type. There are 11,448 AFEBs in the system. Each AFEB services 16 anode channels. There are a total of 183k anode channels in the complete system.

Both the CFEBs and AFEBs were tested in high magnetic field (>3T), and a moderate radiation field, to a fluence five times the expected total ionisation dose (TID) expected in ten years of LHC run at the design luminosity.

The ALCT board generates an anode local charge track trigger using the AFEB information. This anode trigger track in coincidence with a cathode trigger track and a L1A signal controls the readout of the CFEB, AFEB and trigger data.

2) Peripheral Crate electronics:

The Trigger Motherboard (TMB) reconstructs cathode local charge tracks using the CFEB comparator data. The LCT is passed to the CFEB through its DAQMB to control the CFEB capacitor storage. After a fixed delay, if a coincidence is found with the L1A and the AFEB track, a signal is passed through its DAQMB to initiate digitisation. Additionally, upon this coincidence the TMB sends the CFEB comparator information to its DAQMB for readout.

The Data Acquisition Mother Board (DAQMB) controls the on-chamber electronics and read out of a single chamber. This includes collecting raw data from CFEBs and AFEBs, as well as the local CSC trigger information. The DAQMB also serves as the controller performing chamber slow control, calibration, and CFEB monitoring. The DAQMB is designed around seven FIFOs which, upon receipt of a L1A signal, receive data from five CFEBs, one Trigger Mother Board, and one ALCT Board. The DAQMB assembles the data from the seven FIFOs associated with an L1A and assigns header and trailer words containing event summary information such as the L1A number, the beam crossing number when the L1A occurred, and the status of on-board FIFOs. The data is serialized using Texas Instruments TLK2501[10] and transferred at 1.6Gbit/s, through optical fibre to the FED crates in the counting room.

Since each DAQMB services one chamber, there are 468 DAQMB in the full system.

3) Off-detector electronics:

The CSC Front End Driver (FED) electronics includes 36 Detector Dependent Units (DDU) and 4 Data Concentrator Cards (DCC), which reside in four VME crates. The FED

assembles the data from the 468 DAQMBs for transfer to CMS main DAQ via SLINK64. The FED also performs real time error checking, electronics reset requests, and data concentration. Lastly, a fraction of the data is sent to a local computer farm for real time monitoring of the CSC system.

FED crates have custom designed high-speed backplanes. Each DDU receives and deserialises data from 13 DAQMBs by channelling through a Xilinx FPGA's RocketIO[11]. Data from the 13 input fibers are concatenated and header and trailer words added. As the events are assembled, the DDU checks the data for hardware error flags, CRC words, DAQMB/CFEB status, and the L1A number and beam crossing number synchronization. In all, over 150 checks are made on each event received. Thus detector hardware problems can be recognized within 100μsec of their onset. Each DDU sends its data on a pair of FPGA RocketIO communication links (over Gbits/s each) via the custom backplane to the DCC. A fraction of the data is also sent via a custom designed gigabit Ethernet interface to the CSC local DAQ farm.

The main function of the DCC is to further concentrate the data. A single DCC services each FED crate, with four FED crate in total. Each DCC receives data from nine DDUs in the crate through eighteen custom serial links on the backplane. Each DCC outputs the data to CMS main DAQ via two SLINK64 paths. The DCC also receives (via a TTCrx[12] chip) and distributes the LHC clock and CMS control signals to its FED crate via the custom backplane. This permits emulation of the clock and control as needed for debugging purposes if the LHC clock is not available.

4) Local DAQ farm:

The CSC local DAQ farm consists of ten computers. The farm is used for CSC data monitoring during normal LHC data taking, and is also used as the main system for CSC calibration. Nine of the PCs serve as data acquisition computers. Each computer is equipped with two dual-port optical gigabit Ethernet cards to read out data from four DDUs through the custom designed gigabit Ethernet ports. The tenth PC serves as the manager and provides data storage.

5) DAQ system interconnect:

Serial technologies are widely used in the CSC DAQ system design to reduce the number of cables connecting the electronics. From the CFEB to DAQMB, a channel link is used. The data is transferred at 280Mbps for up to 15 meters through skew-clear copper cables. From the DAQMB to the DDU, commercial gigabit serializers and FPGA de-serializers are used. The data is transferred at 1.6Gbps 100 meters through optical fibre cables. Since the DDU and DCC are located in the same VME crate, a serial mesh backplane is used for data connections between DDUs and DCCs. The single serial line has a data rate up to 3.12Gbps. The Xilinx Virtex_RocketIO are used as data transmitters and receivers.

C. DAQ System Calibration

Each CSC Cathode readout channel can be calibrated individually. Each amplifier ASIC (16-channels) is attached to one precision capacitor paired with a fast FET switch. Pulsing is achieved by applying a DC voltage to this capacitor and nearly instantaneously switching the capacitor to a given ASIC channel or group of channels. This allows measurement of each amplifier's linearity, gain, offset, cross talk and noise level. These constants are used in the offline analysis for track reconstruction. The calibration precision is better than one percent.

The CSC anode readout is calibrated by similarly pulsing a built-in capacitor on each AFEB readout channel. The threshold and delay constant are loaded back to the electronics for optimum operation of anode readout electronics.

III. Current Status

The CSC DAQ system has been extensively tested both in beam tests and MTCC test[13]. It performed successfully within design limits during these tests. The system is currently being commissioned for the LHC run at CERN.

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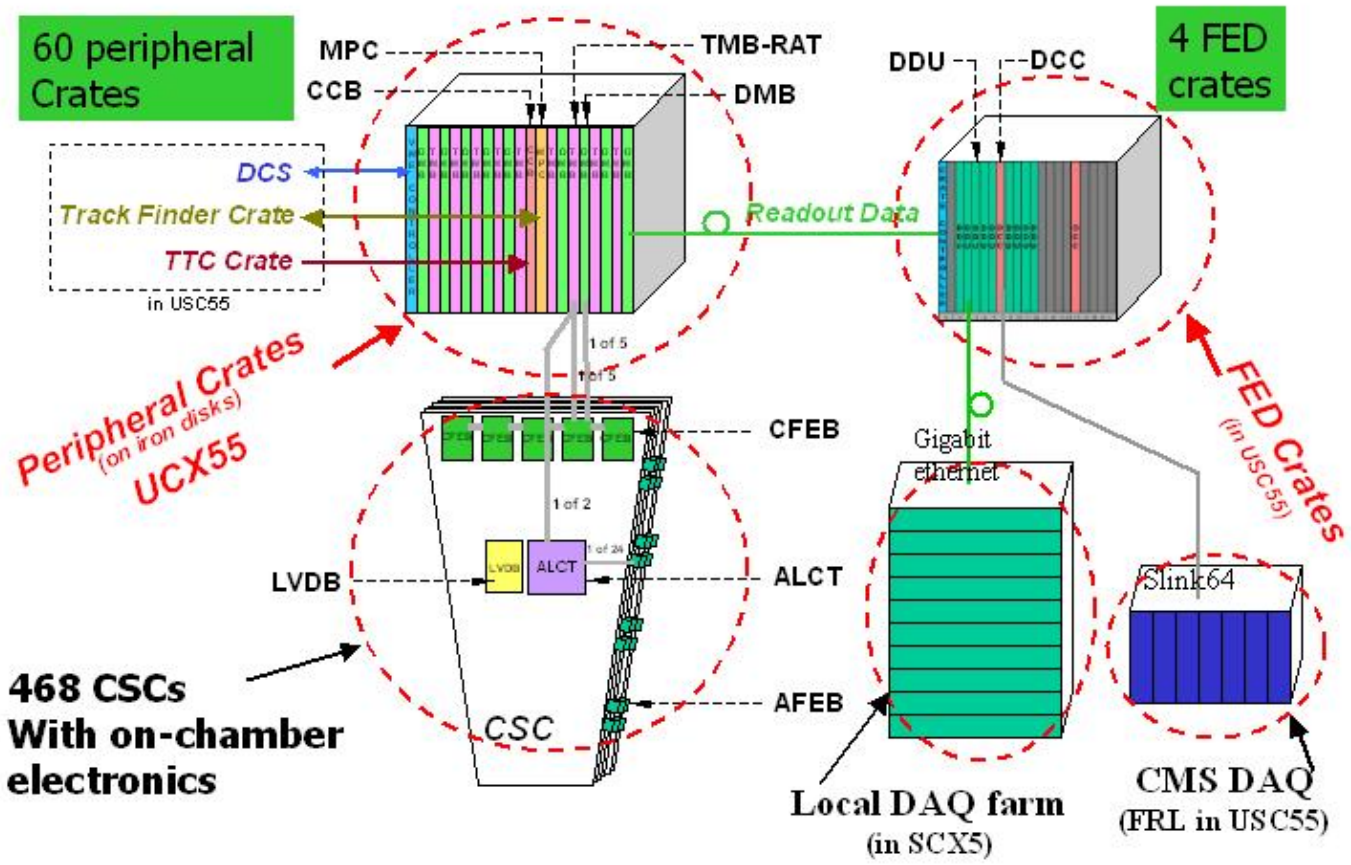

Figure 2: CSC Data Acquisition System Diagram