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CSC Data Acquisition System for CMS

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Details of the Cathode Strip Chamber (CSC) Data Acquisition (DAQ) system for the CMS experiment at the LHC will be described. The CSC system is large, consisting of 218K cathode channels and 183K anode channels. This leads to a substantial data rate of ˜1.5GByte/s at LHC design luminosity (1034cm-2s-1) and the CMS first level trigger (L1A) rate of 100KHz. The DAQ system consists of three parts. The first part is on-chamber Cathode Front End Boards (CFEB), which amplify, shape, store and digitize chamber cathode signals, and Anode Front End Boards (AFEB), which amplify, shape and discriminate chamber anode signals. The second part is the on-detector Data Acquisition Motherboards (DAQMB), which control the on-chamber electronics and the readout of the chamber. The third part is the off-detector DAQ interface boards, which perform real time error checking, electronics reset requests and data concentration. It passes the resulting data to a CSC local DAQ farm, as well as CMS main DAQ. All electronics in the system employ FPGAs allowing programmability. In addition, several high-speed serial interface technologies are employed.

Summary

The Cathode Strip Chamber (CSC) system is one of the major components of the Compact Muon Solenoid (CMS) experiment at Large Hadron Collider (LHC) at CERN. The system is large, consisting of 468 chamber modules, forming eight disks to cover the three magnetic yoke iron stations at each end of the detector. Designed to work at high rates in a high magnetic field and moderate radiation field, the CSCs provide hit position precision measurements of accuracy ˜100μm in the bending coordinate, and timing to better than a single beam crossing (25ns). The electronics system for the CSC is large, consisting of 218K cathode channels and 183K anode channels. The CSC DAQ system reads out data in response to CMS First Level Trigger (L1A) at an event rate of 100KHz. The data enters the CMS main DAQ system through an SLINK64 data path, which builds and filters the events, and writes the data to tape at an event rate of 100Hz.

The CSC DAQ system is naturally divided into three parts. The first part consists of the Cathode Front End Board (CFEB) and Anode Front End Board (AFEB) mounted directly on the chambers. The second part is the Data Acquisition Motherboard (DAQMB) situated in VME crates (Peripheral Crates) on the periphery of the magnetic yoke iron. The third part is the Front End Driver (FED) crates and a CSC local DAQ farm situated in CMS counting rooms. The CSC DAQ system is asynchronous. Events are marked with L1A numbers. Custom parallel Cyclic Redundancy Check (CRC) is heavily used throughout the system to assure data integrity.

The CFEBs amplify, shape and digitize CSC chamber cathode charge signals. Each CFEB services 96 cathode strip channels. Five or four CFEBs are mounted on each chamber, with a total of 2268 boards in the system. A hit in the chamber produces induced charge on cathode strip that is amplified and shaped by BUCKEYE ASIC chips. The output voltage is sampled every 50 ns, and stored in a 96 cell/channel Switch Capacitor Array (SCA) ASIC chips. The chamber electronics is self-triggering. Voltages are stored in the capacitor and digitized only if the CFEB receives a local charge track trigger in coincidence with the L1A. The CFEB utilize commercial 12 bit ADCs. The resulting digital data from the 96 channels are multiplexed at 40MHz, and sent through Channel

link via skew-clear cables (6 to 14.5 meters) to the DAQMB in the crates located on the iron disk periphery.
The Data Acquisition Mother Board (DAQMB) controls the on-chamber electronics and the readout of a single chamber. This includes collecting data from CFEB and AFEB, as well as the local CSC trigger information. The DAQMB also serves as the controller performing slow control, calibration, and CFEB monitoring. The DAQMB is built around seven FIFOs, which upon receipt of L1A, receive data from five CFEBs, one Trigger Mother Board (TMB), and one Anode Local Charge Track Board (ALCT). The DAQMB concentrates the data from the seven FIFO's, assigns header and trailer words containing error information, a CRC check, and a unique L1A number. The data is sent at 1.6Gbit/s using Texas Instruments TI2501 serializer through optical fibers to the FED crates in the counting room. Since each DAQMB services one chamber there are 468 DAQMB in the system.
The CSC Front End Driver (FED) electronics assembles the data from the 468 DAQMBs for transfer to CMS main DAQ via SLINK64. The FED also performs real time error checking, electronics reset requests and data concentration. Lastly, a fraction of the data is sent to a local computer farm for real time monitoring of the CSC system.
The four FED crates include 36 Detector Dependent Units (DDU) and 4 Data Concentrator Cards (DCC). Each crate contains a high speed custom designed backplane. Each DDU receives data from 13 DAQMBs that are channeled through Xilinx FPGA's RocketIO. Data from the 13 input fibers are concatenated with header and trailer words added. As the events are assembled, the DDU checks the data for hardware error flags, CRC words, DAQMB/CFEB status, and the L1A number and beam crossing number synchronization. In all, over 150 checks are made on each event received. Thus detector hardware problems can be recognized within 100μsec of their onset. The DDU outputs its data via FPGA RocketIO communication with two 3.1Gbit/s links on a custom backplane to a Data Concentrator Card (DCC). A fraction of the data is also sent via a custom designed gigabit Ethernet interface to the CSC local DAQ farm.
The main function for the DCC is to further concentrate the data. There is a single DCC in each of the four FED crates. Each DCC receives the data from 9 DDU in the crate through eighteen serial links with 3.1Gbit/s each. The DCC outputs the data to CMS main DAQ via two SLINK64. The DCC also receives (via a TTCrx chip) and distributes the LHC clock and CMS control to its FED crate via the custom backplane. This allows simulation of the clock and control for debugging purposes if the LHC clock is not available.
The CSC local DAQ farm consists of ten computers. Nine of them are served as the data acquisition computers, each equipped with two PCI-express dual-port optical gigabit Ethernet interface cards. One computer serves as the manager and data storage. The farm is used for CSC data monitoring and checking during normal LHC data taking, and is also used as the main system for CSC calibration.
The CSC DAQ system had been extensively tested. It performed successfully during last year's MTCC test. The system is currently being commissioned for the LHC run at CERN.
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