

# Proposal of a readout technique for low-pitch pixel devices

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## *Abstract*

The up-to-date radiation position pixel detectors designed and constructed for high-energy physics, as Large Hadron Collider experiments at CERN, share comparable on-chip readout electronics. They implement full-custom 2D matrixes of sensitive elements, which are basically readout via token-based techniques, according to trigger signals. As the readout phase is one of the crucial points of large matrix devices, here it is described a novel readout architecture of pixel devices, which exploits the features of the state-of-the-art deep-submicron CMOS technologies and could be applied to low-pitch pixel circuits. This allows for future applications not only to general pixel detectors but also to trackers and trigger systems, wherever an on-line data reduction is required.

## I. INTRODUCTION

Over the last years the particle colliders have reduced the bunch crossing time distance and the electronics used for the data acquisition chains of the experiments have followed the deepest sub-micron technologies available on the market. In order to make comparisons with the to-date microelectronics implemented in the latest High-Energy Physics Experiments (HEPE) at CERN, some of the most common features of pixel detectors are below summarized. For example, the Large Hadron Collider intersecting beams are structured into bunches, whose minimum time distance between two collisions is 25 ns. An event is the collection of the information originated from the particles of a given collision. To unambiguously assign the data to the event they belong, the readout electronics must be able to measure the released charge with a time resolution of 25 ns. This can be reached in several ways but some basic rules may be extracted from all experiments. Some HEPE have equipped their front-end electronics with integrated circuits that use similar CMOS technologies [1], the same clock frequency, i.e. 40 MHz of the bunch crossing, and have been designed by making similar layout choices. In particular, for silicon pixel detectors, different experiments have implemented matrixes with a comparable number of pixels sized with similar dimensions. The estimated average of number of pixels is of the order of some thousands (2880 for ATLAS [2-5]), 4160 for CMS [6-10], 8192 for ALICE [11]). These pixels are arranged in bidimensional rectangular matrixes of rows and columns (256 by 32 for ALICE, 80 by 52 for CMS, 160 by 18 for ATLAS). These arrays of pixels are bump bonded over other silicon dies that house the readout electronics. In any case, the hit information of a given event must be readout as fast as possible to reduce the dead time, when it is frozen and blind to new striking particles. During the readout phase the spatial

coordinates and the time information of the hits are sent to output [12-13]. This readout organization depends on the way the pixels are designed, arranged and connected. Some basic considerations can be affirmed in any case:

- the more the number of pixels, the longer the readout phase and hence, the longer the dead time,
- the more the number of wires routed among rows and column of pixels, the larger the pixel's pitch and hence, the lower the spatial resolution of the detector,
- the number of wires in the layout of a pixel device cannot be reduced under a given threshold as it follows the readout architecture.

This latter point has been investigated and the paper presents a novel digital readout scheme to extract the time and position information of the hits, wherever they are spread out over the matrix of pixels. This solution may be implemented in hardware by exploiting the up-to-date computer-aided-design tools to project digital circuits. Moreover, in conjunction with the full-custom design of the sensitive pixel cells, the proposed architecture may lead to the design of mixed-mode ASICs with fast readouts if compared to those applied today. As pointed out above, the matrixes implemented on the main HEPE today are comparable in terms numbers of pixels, rows and columns. In addition, also the average expected occupancy might be estimated in a few percentage points. Moreover, in the past years the digital readout circuits were mostly designed and implemented via either quite simple full-custom specific solution, or based on digital cell mainly arranged and placed by hands. In any case the ASICs have not been in-depth studied to provide on-line efficient sparsification of the dataset. Today, the state-of-the-art CMOS technologies allow for future high-performance digital readout architectures.

## II. READOUT TECHNIQUE

The idea is to not use point-to-point wires from the border of the matrix to the single pixels or groups of pixels at all. All the pixels are driven via global wired-or nets and are readout via other row wires shared over the whole matrix. This work aims at simplifying the internal routing of pixels and moves outside the matrix, on the digital readout part, the sparsification logic. This leads to a matrix wire-density and to a pixel's pitch independent to the number of pixels and allows for future bigger detectors with respect to those recently used. The pixels do not own internal registers and there are no dedicated wires to freeze single pixels. To avoid data overlap

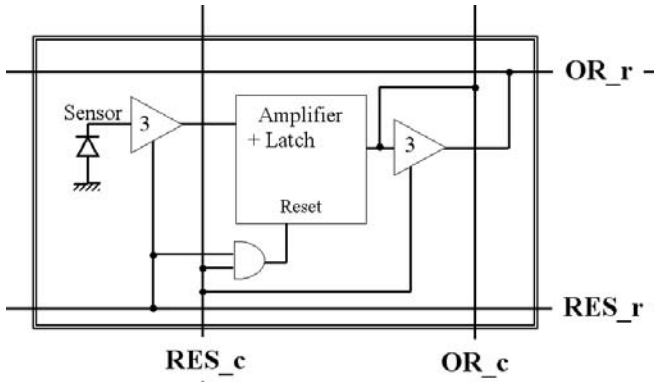


Figure 1: The pixel logic schema

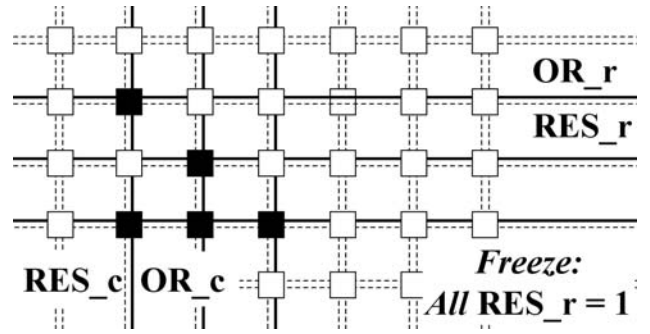


Figure 2: Columns and rows of the hits

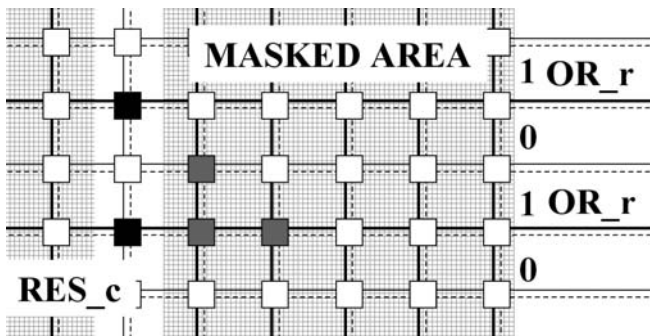


Figure 3: The readout starts on the first selected column

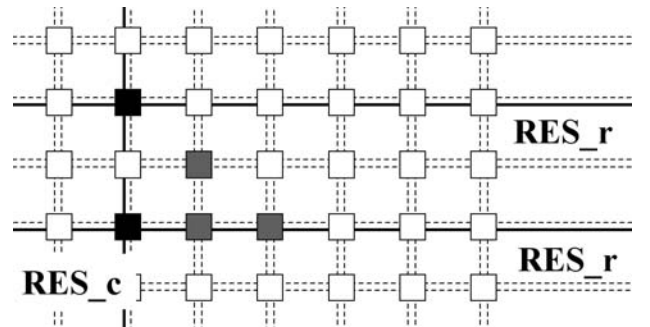


Figure 4: The first reset on the columns

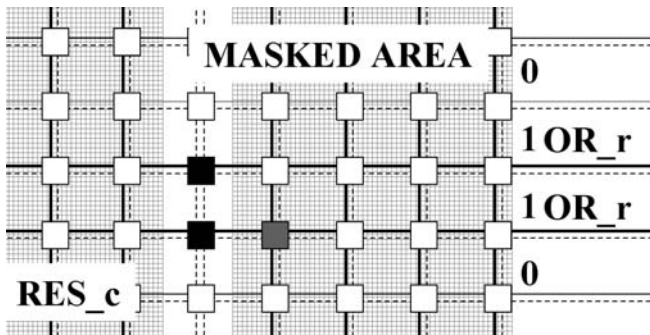


Figure 5: The second selected column

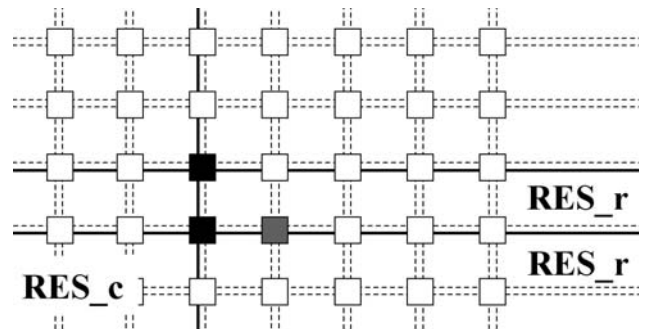


Figure 6: The second reset on the columns

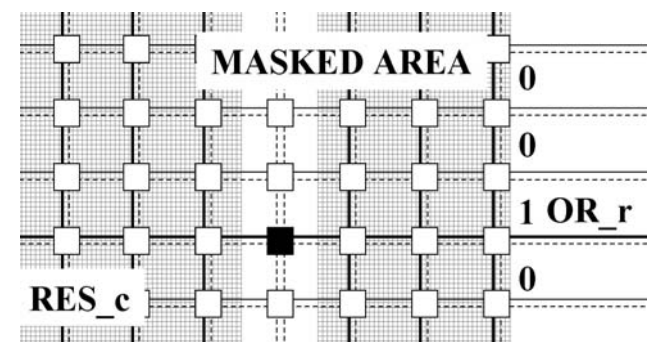


Figure 7: The last selected column

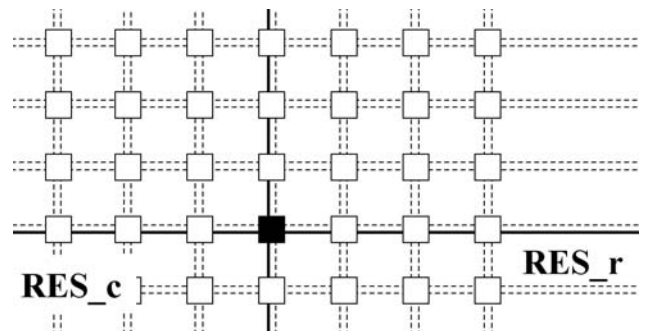


Figure 8: The last reset on the columns

of adjacent bunches the hits are frozen and set free, column by column (or row by row), at any read clock cycle.

The pixel, from the logic viewpoint, might be represented via the schema shown in Fig. 1. There are 4 wires shared with adjacent pixels over then entire matrix:

- OR\_r is a horizontal output wire that provides the hit state via a latch and an output buffer. When the buffer is enabled through the RES\_c vertical line, the pixel's output is read. This line is shared with all the pixels of the same row, by creating a wired-or condition: if only one pixel of the row is high, the wire is also high,

- RES\_r is a horizontal input wire that can freeze the pixel state by making it insensitive to the sensor. Moreover, in conjunction with the RES\_c line, it resets the pixel. This line is shared with all the pixels of the same row,
- OR\_c is a vertical output line always connected to the pixel's output. This is connected together with all the pixels in the same column, by creating a wired-or condition: if only one pixel of the column is high, the wire is also high,
- RES\_c is a vertical input line used alone to enable the output buffer or together with the RES\_r line to reset the pixel.

Let's give a brief functional description by following the figures from 2 to 8. For example, at a given time the hit situation is shown in Fig. 2. Five hits are present and, consequently, 3 OR\_r and 3 OR\_c wires are high thanks to the wired-or conditions. Now, only the most-left column that contains at least one hit is enabled. All the other columns are masked via the RES\_c lines. Fig. 3 shows this situation and the OR\_r lines indicate which pixels on the selected column have hits and which have not. Then this column can be reset via RES\_c and RES\_r combinations: the two pixels are reset at the same time. Fig. 4 shows this reset phase. Then the process moves to the right and the same steps are carried out until all the hits are read. This is shown through Fig. 5 to 8.

The potential drawback of this readout logic is that readout phase must be very fast to avoid freezing the entire matrix for a too long time. In fact, during the readout, the pixels must be frozen to avoid overlaps. On the other hand, it should be noted that the columns are read one at a time and all the pixels of one column are read in parallel. In principle, the readout phase takes as many clock periods as the number of columns that own hits. In other words, for low-occupancy devices, this technique could be considered for its simplicity.

Moreover, before the matrix readout starts, the coordinates of these hits must be associated with a time-stamp, whose registers can be located outside the matrix.

### III. CONCLUSION

The solution can be easily investigated and designed using and exploiting the state-of-the-art CAD tools (digital synthesis, place-and-route, etc.). Moreover, the approach might be associated with a custom-designed matrix to a final mixed-mode ASIC design.

The wiring complexity is independent of the number of pixels as there are no point-to-point wires: all the lines are global.

The proposed approach could match the requirements of future low-pitch pixel detectors that need robust on-chip digital sparsification and that may be also used in first level triggers on tracks in vertex detectors.

### IV. REFERENCES

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