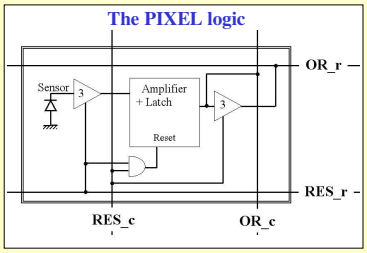
# Proposal of a readout technique for low-pitch pixel devices

**Alessandro Gabrielli**
INFN-Bologna & Physics Department University of Bologna
Viale Berti Pichat 6/2 40127 Bologna Italy
Tel: +39-051-2095052 Fax: +39-051-2095297
Email: alessandro.gabrielli@bo.infn.it URL: http://www.bo.infn.it/~gabriell

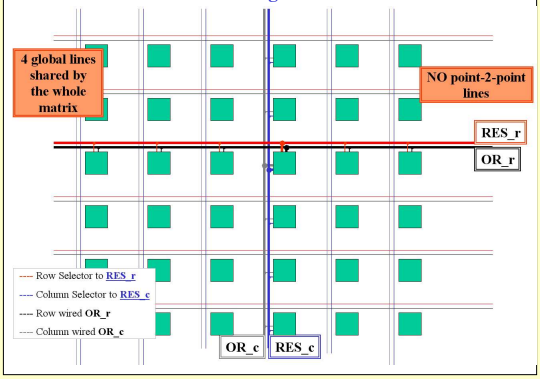

## Abstract

The up-to-date radiation position pixel detectors designed and constructed for high-energy physics, as Large Hadron Collider experiments at CERN, share comparable on-chip readout electronics. They implement full-custom 2D matrixes of sensitive elements, which are basically readout via token-based techniques, according to trigger signals. As the readout phase is one of the crucial points of large matrix devices, here it is described a novel readout architecture of pixel devices, which exploits the features of the state-of-the-art deep-submicron CMOS technologies and could be applied to low-pitch pixel circuits. This allows for future applications not only to general pixel detectors but also to trackers and trigger systems, wherever an on-line data reduction is required.

## The PIXEL logic



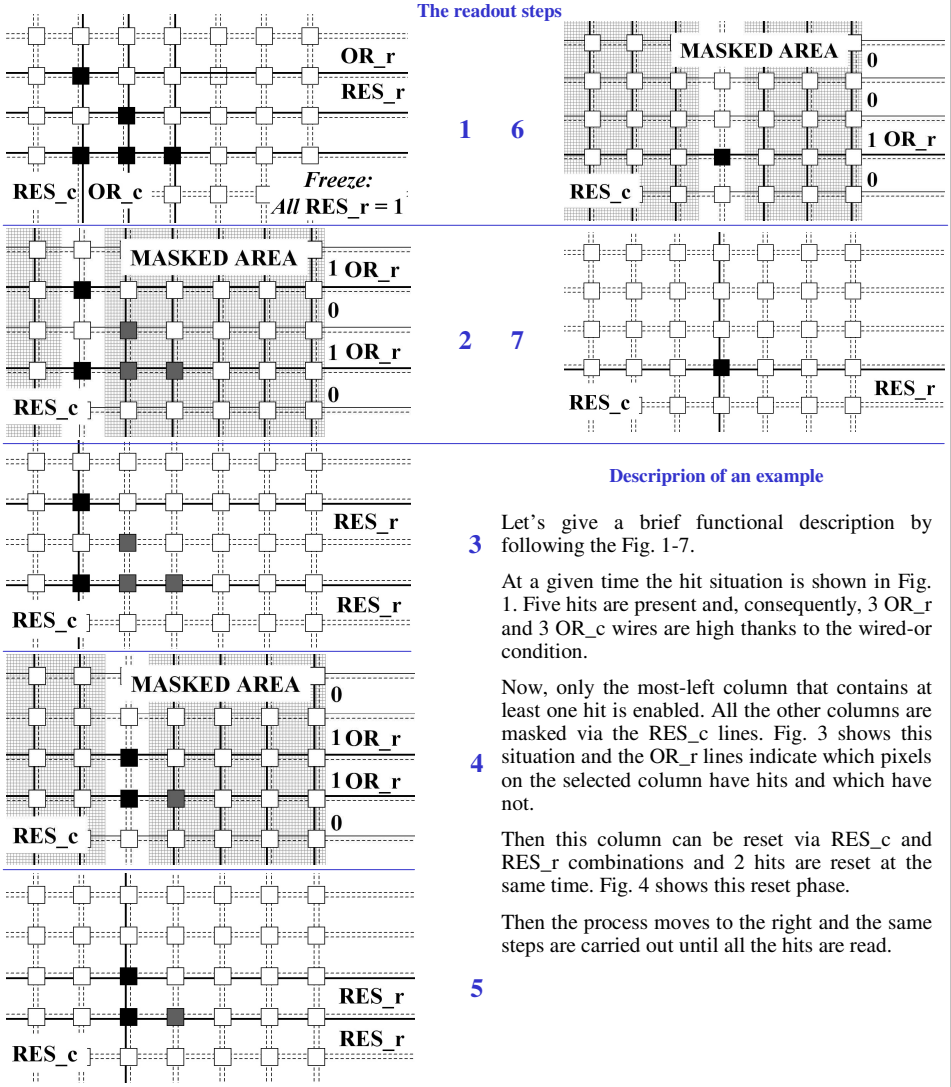

## The matrix organization




## Conclusions

The solution can be easily investigated and deigned using and exploiting the state-of-the-art CAD tools (digital synthesis, place-and-route, etc.). Moreover, the approach might be associated with a custom-designed matrix to a final mixed-mode ASIC design. The wiring complexity is independent of the number of pixels as there are no point-to-point wires: all the lines are global. The proposed approach could match the requirements of future low-pitch pixel detectors that need robust on-chip digital sparsification and that may be also used in first level triggers on tracks in vertex detectors.

## The readout steps




## Descriprion of an example

Let's give a brief functional description by following the Fig. 1-7.

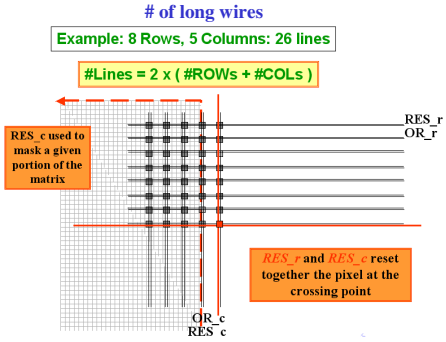
At a given time the hit situation is shown in Fig. 1. Five hits are present and, consequently, 3 OR_r and 3 OR_c wires are high thanks to the wired-or condition.

Now, only the most-left column that contains at least one hit is enabled. All the other columns are masked via the RES_c lines. Fig. 3 shows this situation and the OR_r lines indicate which pixels on the selected column have hits and which have not.

Then this column can be reset via RES_c and RES_r combinations and 2 hits are reset at the same time. Fig. 4 shows this reset phase.

Then the process moves to the right and the same steps are carried out until all the hits are read.

## # of long wires




Pixels ARE NOT point-2-point read, their state is deduced from these values:

- *OR_r* is the wired-OR of each single row,
- *OR_c* is the wired-OR of each single column,
- *RES_r* and *RES_c*, if activated at the same time, reset the pixel at the crossing point
- *RES_c*, if used alone, defines a MASK for the matrix

- Local Density of connecting lines (wires) is independent of the matrix dimensions
- Each pixel sees just 4 lines in any case

The idea is to not use point-to-point wires from the border of the matrix to the single pixels or groups of pixels at all. All the pixels are driven via global wired-or nets and are readout via other row wires shared over the whole matrix. This work aims at simplifying the internal routing of pixels and moves outside the matrix, on the digital readout part, the sparsification logic. This leads to a matrix wire-density and to a pixel's pitch independent to the number of pixels and allows for future bigger detectors with respect to those recently used. As the pixels do not own internal registers and there are no dedicated wires to freeze single pixels, to avoid data overlap of adjacent bunches the hits are frozen and set free, column by column (or row by row), at any read clock cycle. The pixel, from the logic viewpoint, might be represented via the schema shown in Fig. 1. There are 4 wires shared with adjacent pixels over then entire matrix:

- OR_r is a horizontal output wire that can provide the hit state via a latch and an output buffer. When the buffer is enabled through the OR_c vertical line, the pixel's output is read. This line is shared with all the pixels of the same row, by creating a wired-or condition: if only one pixel of the row is on, the wire is also on,

- RES_r is a horizontal input wire that can freeze the pixel state by making it insensitive to the sensor. Moreover, in conjunction with the RES_c line, it resets the pixel. This line is shared with all the pixels of the same row,

-- OR_c in a vertical output line always connected to the pixel's output. This is connected together with all the pixels in the same column, by creating a wired-or condition: if only one pixel of the column is on, the wire is also on,

-- RES_c is a vertical input line used alone to enable the output buffer or together with the RES_r line to reset the pixel.