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Proposal of a readout technique for low-pitch pixel devices

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The up-to-date pixel detectors applied to HEP in LHC experiments implement 2D matrixes of sensitive elements that are basically readout via token-based techniques, according to external trigger signals. As the readout time is one of the drawbacks of large matrix devices, because it implies long detector dead times, here it is described a novel readout architecture of pixel devices, which exploits the features of deep-submicron CMOS technologies and should be considered for low-pitch pixel devices. This allows for future applications not only on general pixel detectors but also on trackers and trigger systems, wherever an on-chip data reduction/sparsification is considered.

Summary

The readout electronics exploited for to-date pixel detectors mainly implement token-based techniques to readout the hits. The number of pixels per chip of the LHC experiments is of the order of some thousands. These pixels are designed with bidimensional rectangular matrixes and arranged in rows and columns. It can be affirmed that the more is the number of pixels, the longer is the dead time because the longer is the readout phase. In fact, the more is the number of wires routed among the rows and the columns of the matrix in the chip layout, the larger is the pixel's pitch. This latter plays a significant role in the spatial resolution of the pixel detector. As the number of wires used by the readout architecture specifies how the information of the hits is sent to the output, this number cannot be scaled under a given minimum threshold. This point has been in-depth investigated and simulated and the paper presents a novel digital readout scheme to extract the time and position information of the hits, wherever they are spread out over the pixels'area, via a non-token based technique. This solution may be implemented in hardware by exploiting the up-to-date CAD tools to project digital circuits and, in conjunction with the full-custom design of the sensitive pixel cells, it may lead to the production of mixed-mode ASICS with fast readout logic. The idea is to not use point-to-point wires from the border of the matrix to the single pixels or groups of pixels at all. All the pixels are driven via global wired-or nets and are readout via other row wires shared over the whole matrix. This work aims at simplifying the internal routing of pixels and moves outside the matrix, on the digital readout part, the sparsification logic. This leads to a matrix wire-density and to a pixel's pitch independent to the number of pixels and allows for future bigger detectors with respect to those recently used. As the pixels do not own internal registers and there are no dedicated wires to freeze single pixels, to avoid data overlap of adjacent bunches the hits are frozen and set free, column by column (or row by row), at any read clock cycle. Let's give a brief functional description. At a given time, for example when a bunch-crossing signal is given, the columns that own at least one hit are seen via wired-or nets and frozen. The coordinates of these columns are associated with a time-stamp, whose buffers are located outside the matrix. Then, one at a time, the columns are enabled and the pixels'out write the horizontal bus. In one period a full column of pixels is readout and set free. Then the process moves to another column. The proposed approach could match the requirements of future low-pitch pixel detectors that need robust on-chip digital sparsification and that may be also used in first level triggers on tracks in vertex detectors.

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