The ALICE trigger electronics

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On behalf of Trigger Project in the ALICE collaboration
Overview

- Introduction to Trigger system in ALICE experiment
- Central Trigger Processor (CTP) electronics
- Local Trigger Unit (LTU) electronics
- Newly developed TTCit board
- Software
- Status of project
ALICE experiment

CENTRAL TRACKER
Silicon pixel, Silicon Drifts, Silicon Microstrips, TPC, TRD, TOF

FORWARD DETECTORS
T0, V0, FMD, PMD

SPECIAL DETECTORS
ACORDE, PHOS, EMCAL, HMPID

DIMUON TRACKER
Absorber, Tracking chambers
Trigger chambers
3 HW trigger levels:

- **L0**: inputs to CTP up to 800 ns, time for making decision 100 ns, time for delivery to detectors up to 300 ns, together is max. 1.2 μs from interaction;
- **L1**: inputs to CTP up to 6.1 μs; time for making decision 100 ns, together is max. 6.5 μs from interaction;
- **L2**: delivered to detectors 88 μs from interaction.

60 trigger inputs

- **L0** 24; **L1** 24; **L2** 12.

Up to 24 detectors

- 6 independent partitions (*clusters*)
- 50 classes
- 4 past/future protection circuits
- Interaction record - a list of all the bunch-crossings in which the Interaction signal has been detected; for past-future protection check and pattern recognition

Rare event handling
Classes and clusters

- 50 classes
- Classes define requested physics i.e. which trigger inputs must be active for making decision
- Cluster inside classes define which detectors will receive trigger decision
- Past-future protection inside classes define number of interaction in time interval
- Rare event handling
Past-future protection

- Past-future protection circuits (at each trigger level) check number of interaction in certain time window $\Delta T$
- $\text{INT}_{a,b}$ – interaction inputs
- $\text{TH}_{a, b}$ – thresholds, number of interaction
- $\Delta T_{a,b}$ – protection time intervals
- $P_{x1}, P_{x2}$ – outputs
- Delay $a,b$ for alignment of result
Alice trigger system

- Central Trigger Processor (CTP): receives trigger detector inputs, makes decision
- Local Trigger Unit (LTU): interface between CTP and readout detectors
- Trigger and Time Control (TTC): transmits LHC clocks and delivers trigger signals to detectors
6U VME boards

Trigger inputs are LVDS

Outputs are sent to Local Trigger Units (LTUs) where conversion to output format occurs
Due to short time for L0 latency the CTP is in the experimental cavern.
CTP backplane
L0, L1, L2 boards

- Receives signals from trigger sub-detectors
- Compare received signals with defined classes
- Generate L0, L1, L2 triggers
- Serialize data and send them to the next level through VME backplane
- Past-future protection circuits
- Sampling memory for 26 ms
- Inside CTP is processing only classes and clusters
- In the Fanout board the clusters are converted into subdetector set of signals
BUSY board

- Receive BUSY signals from 24 sub-detectors
- Convert sub-detector BUSY signals to CLUSTER BUSY
- BUSY signals from sub-detectors that participate in a given cluster are all ORed together
- Generate CLUSTER BUSY for CTP
INT board

- Interface to DAQ –
  1. CTP readout
  2. Interaction record
- Trigger data are sent to DAQ System via SIU DDL module
- Reads SIU DDL busy and propagate it to the CTP
CTP connections

(The CTP trigger inputs and the RoI inputs not shown)
Each TTC partition contents:
- LTU board
- TTCvi board
- TTCex board
TTC partition in the experimental cavern

TTC partition:
- LTU board
- TTCvi board
- TTCex board
LTU board

- Serves as interface between CTP and detectors
- Global mode & standalone mode
- Emulation of CTP in the standalone mode – main functionality of LTU
- Each sub-detector can work on his own
- Receives BUSY from detector
- Sends BUSY to BUSY board (CTP)
- Sends L0 to detector through LVDS cable or through TTC system
- Sends L1 and L2 triggers through TTC system
LTU board

CTP
FAN-OUT board

CTP emulator

External inputs

Emulated inputs

Local BUSY

BUSY logic

Mode

Selector

LTU logic

Monitoring counters

Backplane copy

(to Roll)

LTU outputs

(to TICV/TIC/ex)

VME outputs

(to TICv1)

BUSY output

(to CTP)
Trigger data

- Trigger data are sent as TTC broadcasts with both **L1** and **L2** triggers
  - **L1** message: 5 words (each 4-bits address and 12-bits data) which content: calibration flag; readout control bits(4); segmented readout flag; L1 software class flag; L1 active trigger classes (50).
  - **L2a** message: 8 words (each 4-bits address and 12-bits data) which content: bunch crossing ID(12); orbit ID(24); calibration flag; L2 software class; L2 cluster mask (6); L2 active trigger classes (50).
  - **L2r** word (4-bits address and 12-bits data) which contents: bunch crossing ID(12).
Sequence execution triggered by **Start signal** derived from BC scaled down, random generator, external pulser or software request.

The LTU board can generate incomplete sequences or different types of errors can be introduced, either randomly or "on demand" with CTP emulator in LTU software.
Newly developed TTCit board

Main functionality:

- Checking trigger sequences and detection of errors
- Indication of coming triggers and trigger errors on the front panel
- Counting triggers and trigger errors – counters accessible via VME bus
- Sampling trigger data into memory for offline analyze (26 ms)
TTCit board

- 23 LEDs for indication
- Flash memory for config.
- Altera FPGA for VME interf.
- SRAM for sampling data
- Altera Cyclone for TTCit functionality
- Lemo conn. for scope a,b
- L0 input (LVDS)
- TTCrq mezzanine board

6U VME board
The TTCit can be added, temporarily or permanently, to the sub-detector TTC partition (LTU, TTCvi, TTCex, TTCit) or it could also be installed separately, in Personnel Accessible Areas, for monitoring of the TTC operation during the physics run.

VME access
Triggers
Trigger errors
Scope a, b outputs
L0 input
TTC input
**TTCit software**

- HW counters for triggers and trigger errors
- Display snap-shot memory (SSM) content
- SSM analyzer – diagnostics of trigger sequences
- SOFT MONITOR - continuous scanning of SSM contents
- ONLINE MONITOR
- Scope signals
- Configuration – remote programming Flash memory and loading FPGA config.
Detection of trigger errors

- L0, L1 spurious
- L1 message: missing, data error, incomplete, spurious
- L2 message: missing, data error, incomplete, spurious
- PP error, CAL error
- BCID error
Status of project

- The ALICE Trigger system, including the Local Trigger Unit electronics, has been commissioned with all ALICE detectors on the surface
- All trigger electronics has been installed in the experimental cavern
- Integration and commissioning of the Trigger system with detectors in the experimental cavern is on the way
TWEPP 2007

- Thank you for your attention
Spare slides

- Spare slides
**LTU board**

- re-synchronisation of data and strobe signals
- de-serialization of the L1 Data and the L2 Data messages and their conversion into the adopted TTC format for the *L1 Message*, the *L2a Message* and the *L2r Word*
- queuing and temporary storage (FIFO) of the formatted TTC words
- control and arbitration of the FIFO read operation and transmission *via* the VMEbus to the TTCvi board