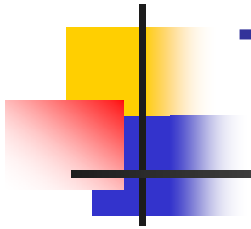

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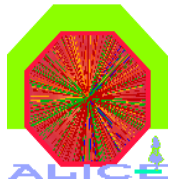


The ALICE trigger electronics

Marián Krivda

On behalf of Trigger Project in the ALICE collaboration

Overview

- Introduction to Trigger system in ALICE experiment
- Central Trigger Processor (CTP) electronics
- Local Trigger Unit (LTU) electronics
- Newly developed TTCit board
- Software
- Status of project

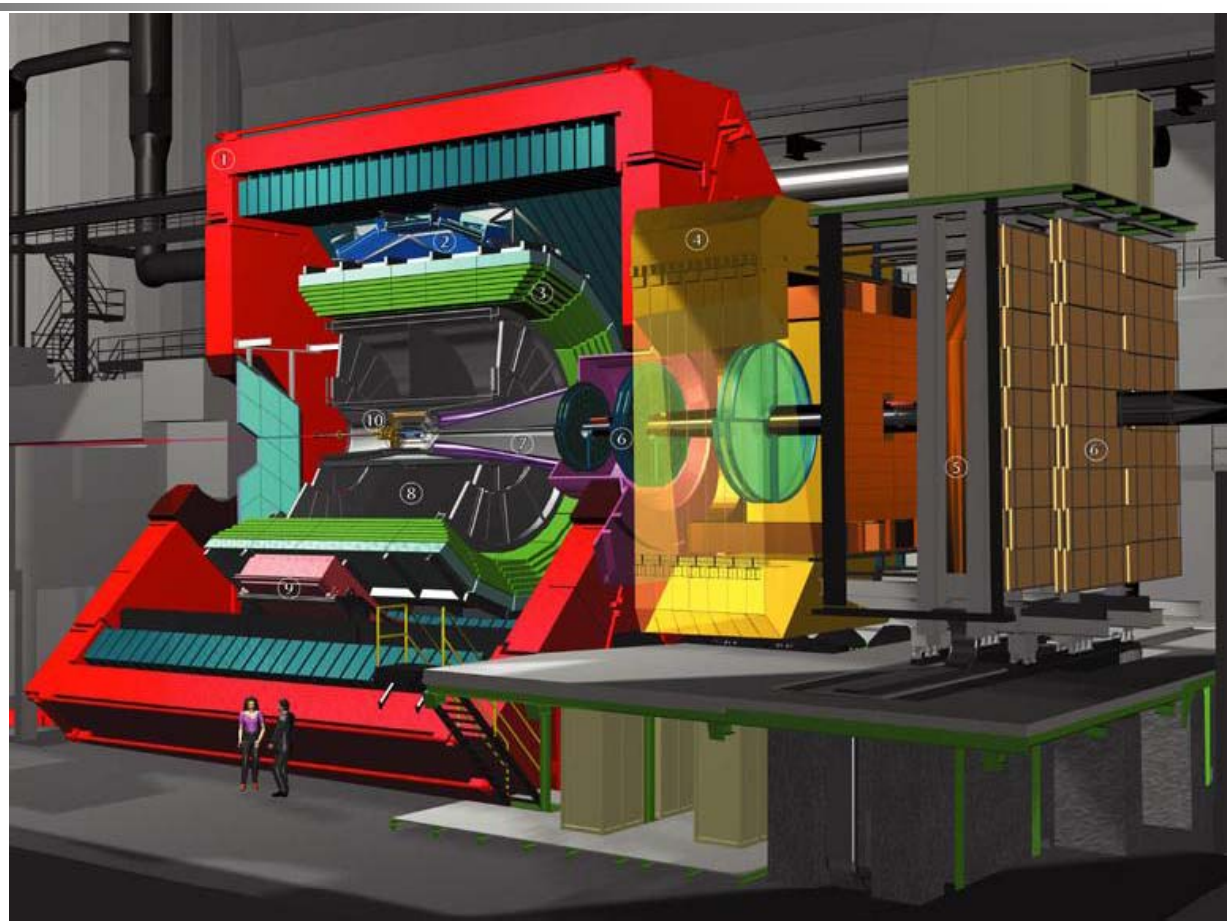
ALICE experiment

CENTRAL TRACKER
Silicon pixel, Silicon Drifts, Silicon Microstrips, TPC, TRD, TOF

FORWARD DETECTORS
T0, V0, FMD, PMD

SPECIAL DETECTORS
ACORDE, PHOS, EMCAL, HMPID

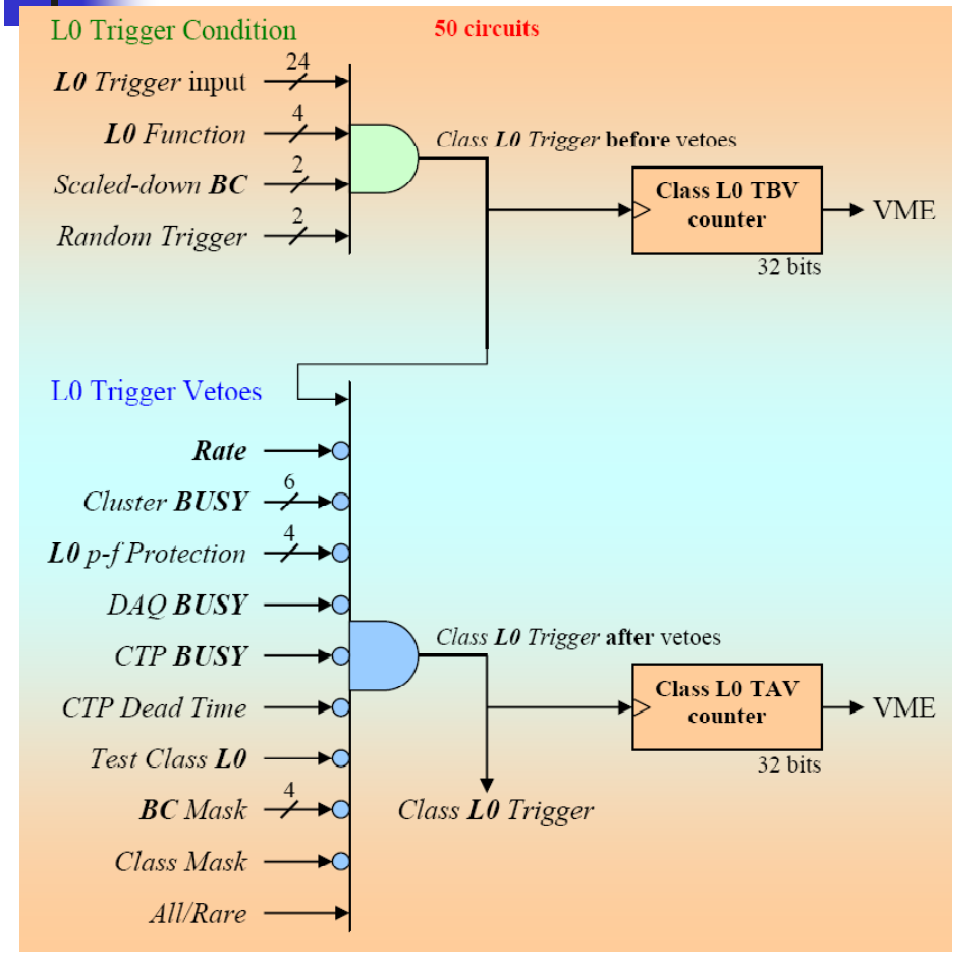
DIMUON TRACKER
Absorber, Tracking chambers
Trigger chambers



System parameters for ALICE Trigger

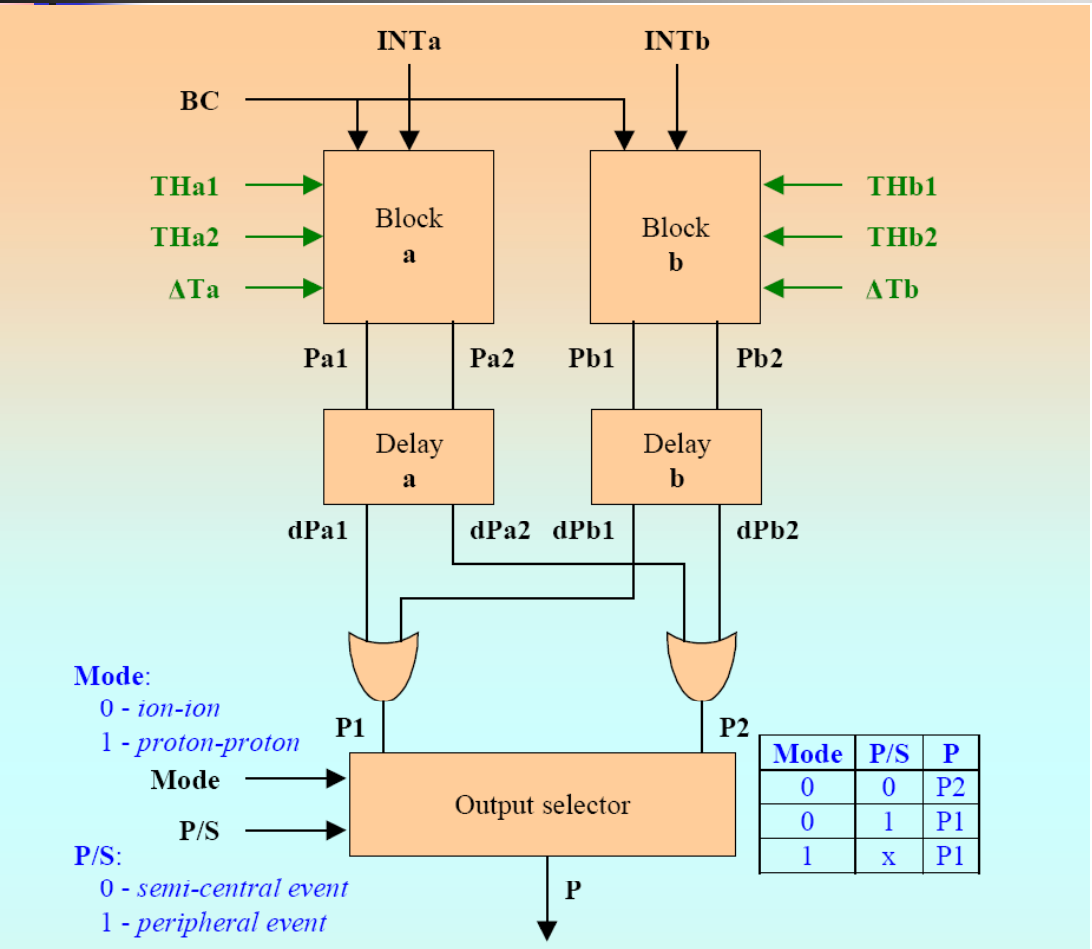
- 3 HW trigger levels:
  - **L0** inputs to CTP up to 800 ns, time for making decision 100 ns, time for delivery to detectors up to 300 ns, together is max. **1.2 μs** from interaction;
  - **L1** inputs to CTP up to 6.1 μs; time for making decision 100 ns, together is max. **6.5 μs** from interaction;
  - **L2** delivered to detectors **88 μs** from interaction.
- 60 trigger inputs
  - **L0** 24; **L1** 24; **L2** 12.
- Up to 24 detectors
- 6 independent partitions (*clusters*)
- 50 classes
- 4 past/future protection circuits
- Interaction record - a list of all the bunch-crossings in which the Interaction signal has been detected; for past-future protection check and pattern recognition
- Rare event handling

Classes and clusters



- 50 classes
- Classes define requested physics i.e. which trigger inputs must be active for making decision
- Cluster inside classes define which detectors will receive trigger decision
- Past-future protection inside classes define number of interaction in time interval
- Rare event handling

Past-future protection



- Past-future protection circuits (at each trigger level) check number of interaction in certain time window ΔT
- INTa,b – interaction inputs
- THa, THb – tresholds, number of interaction
- ΔTa,b – protection time intervals
- Px1, Px2 – outputs
- Delay a,b for alignment of result

Alice trigger system

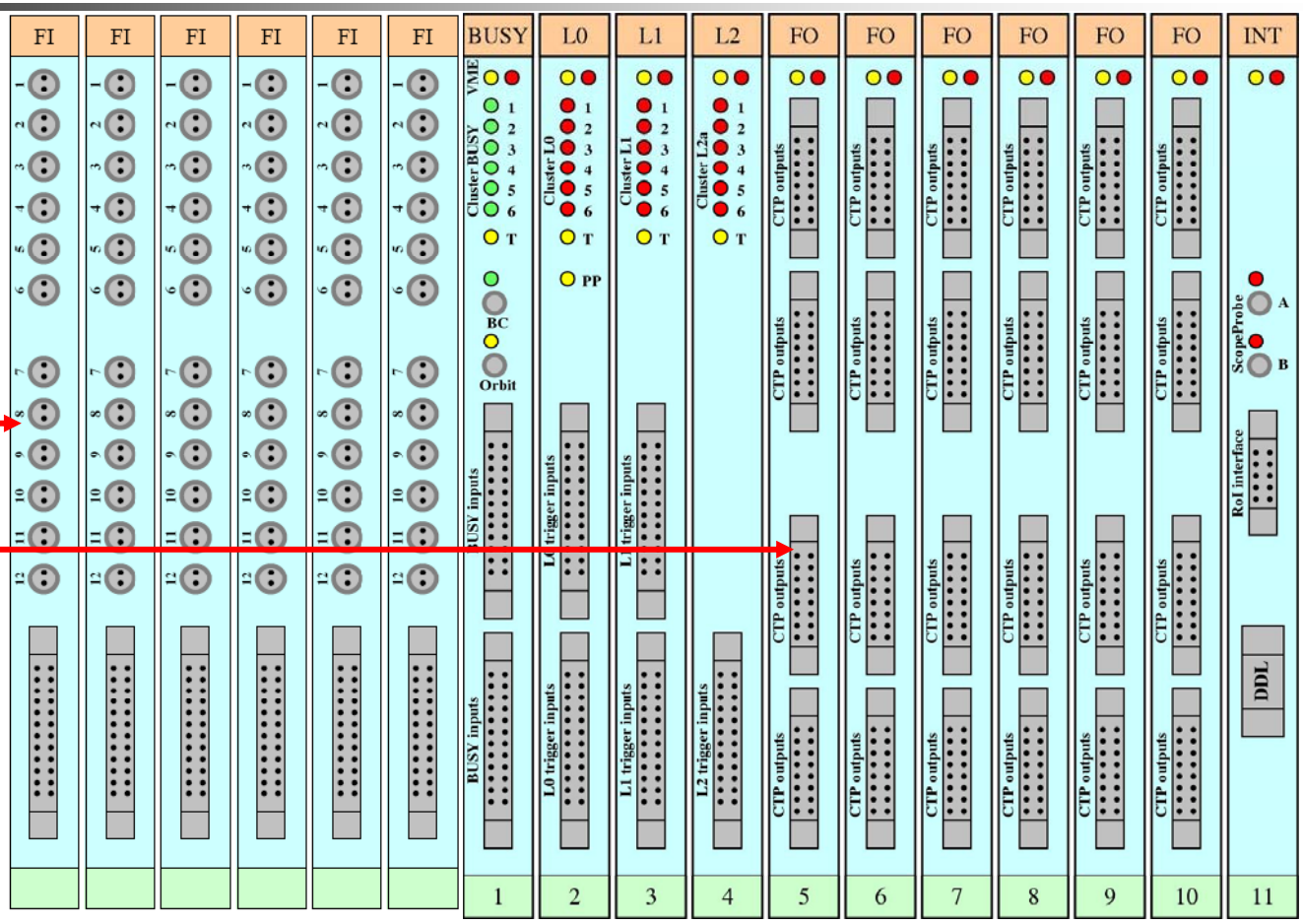
- Central Trigger Processor (CTP):
  receives trigger detector inputs,
  makes decision
- Local Trigger Unit (LTU):
  interface between CTP and readout detectors
- Trigger and Time Control (TTC):
  transmits LHC clock and delivers trigger signals to detectors

CTP layout

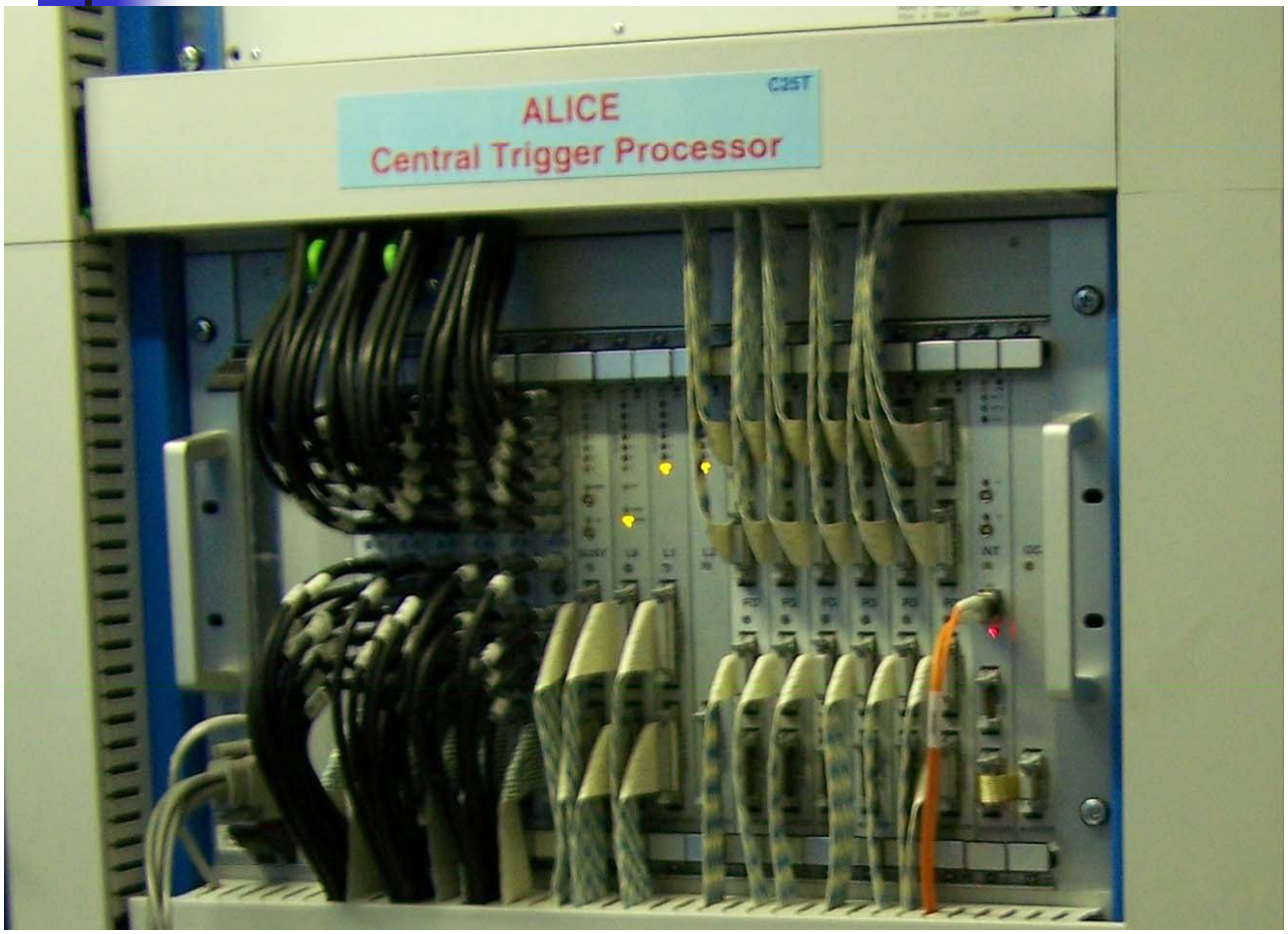
6U VME boards

Trigger inputs are LVDS

Outputs are sent to Local Trigger Units (LTUs) where conversion to output format occurs

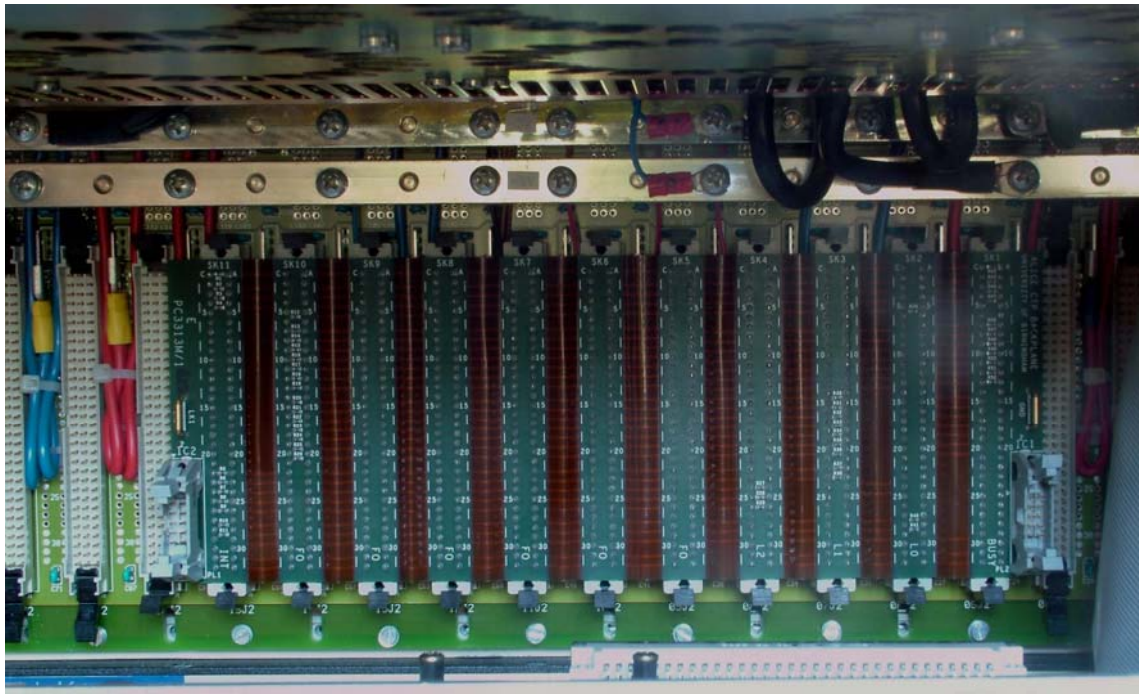


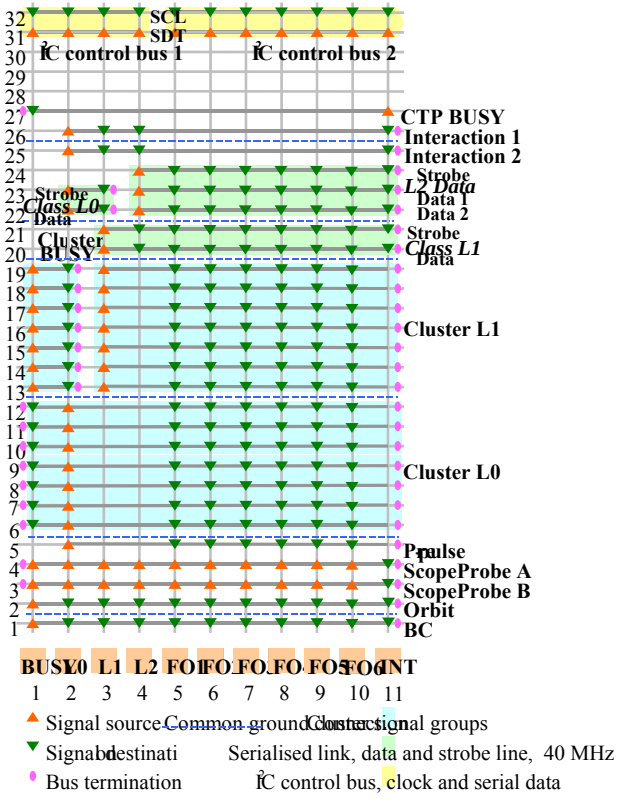
CTP in the experim. cavern

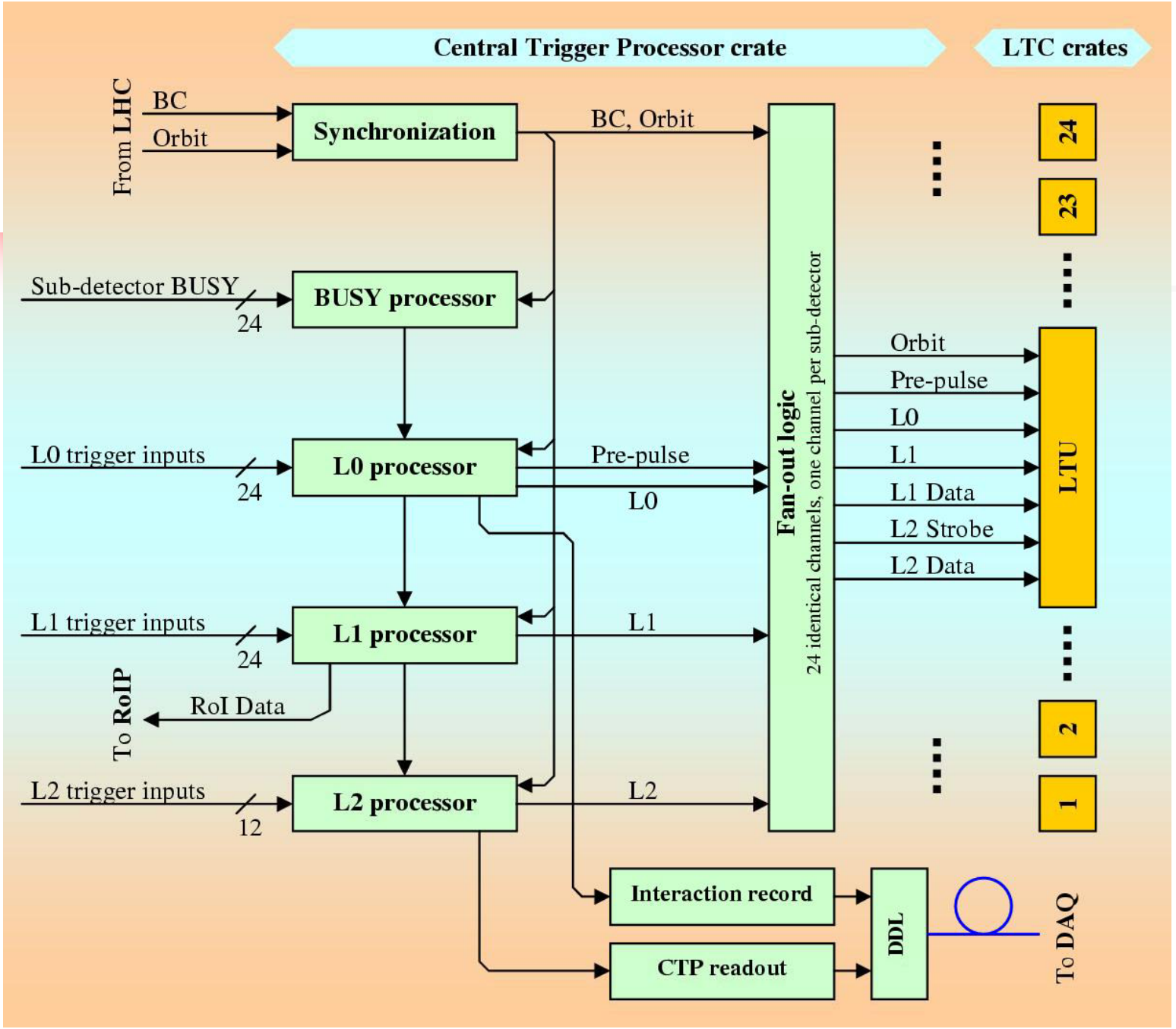


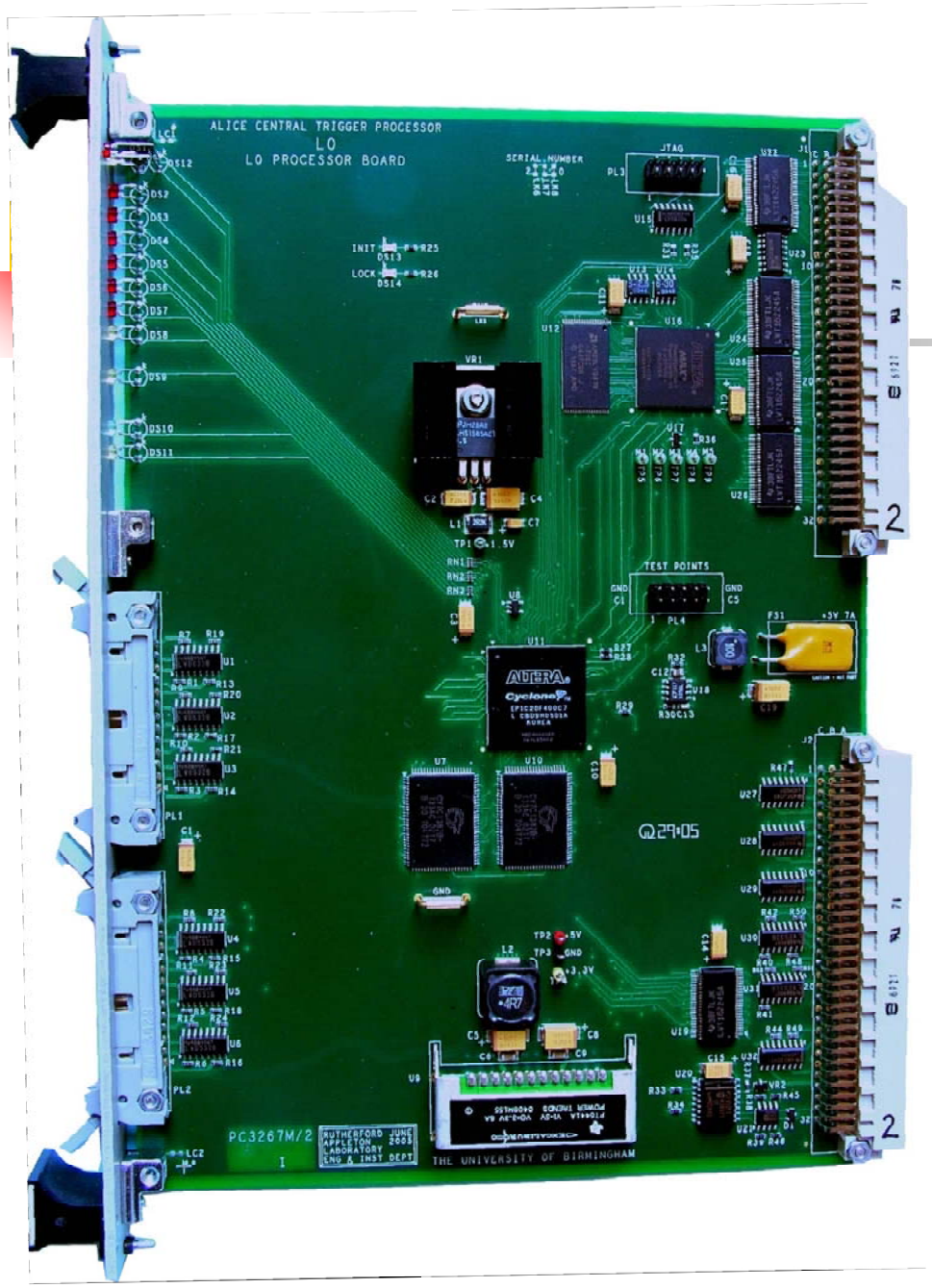
Due to short time for L0 latency the CTP is in the experimental cavern.

CTP backplane



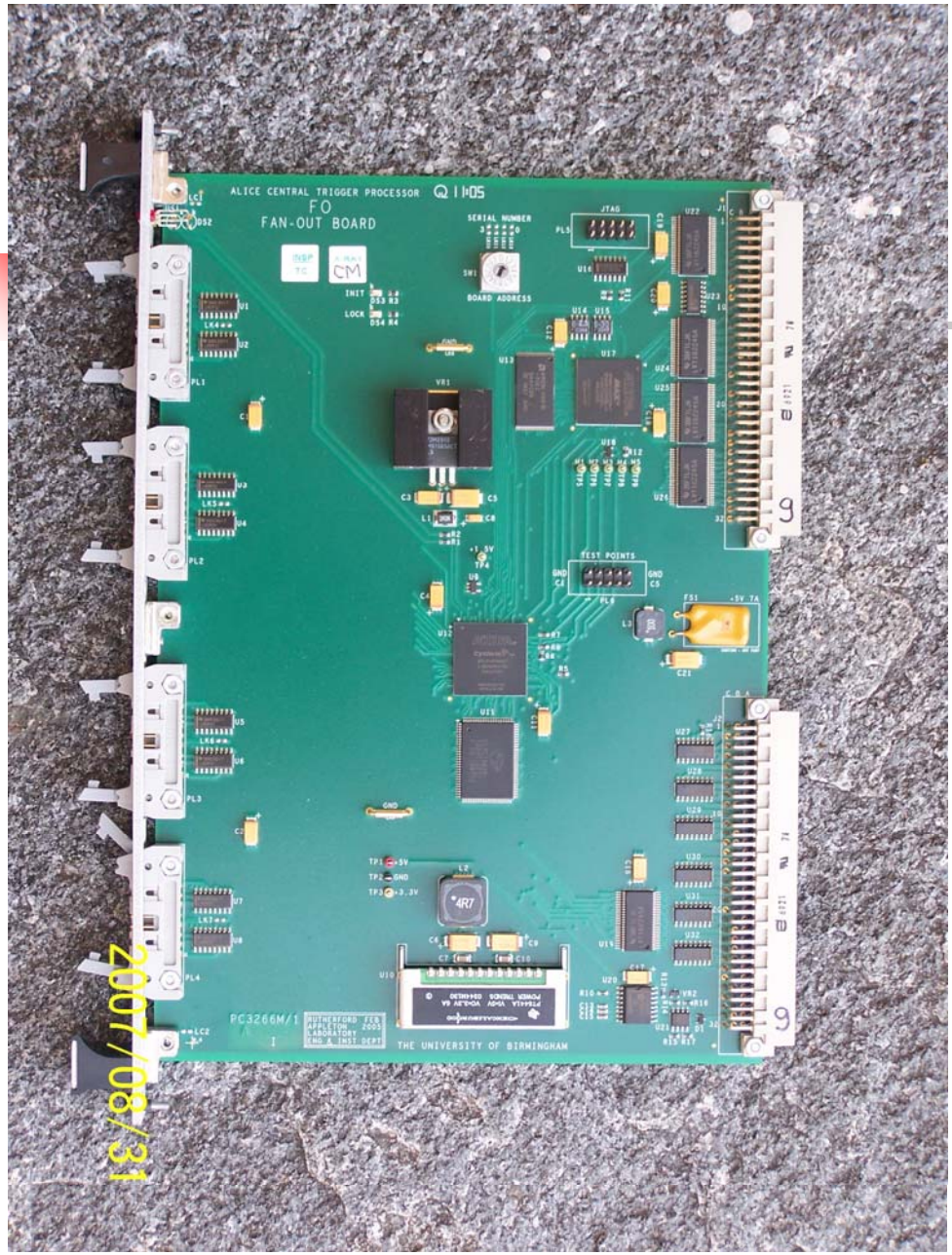



Central Trigger Processor crate
LTC crates
From LHC
BC
Orbit
Synchronization
BC, Orbit
Sub-detector BUSY
24
BUSY processor
L0 trigger inputs
24
L0 processor
Pre-pulse
L0
L1 trigger inputs
24
L1 processor
L1
To RoIP
RoI Data
L2 trigger inputs
12
L2 processor
L2
Fan-out logic
24 identical channels, one channel per sub-detector
Orbit
Pre-pulse
L0
L1
L1 Data
L2 Strobe
L2 Data
LTU
24
23
2
1
Interaction record
CTP readout
DDL
To DAQ



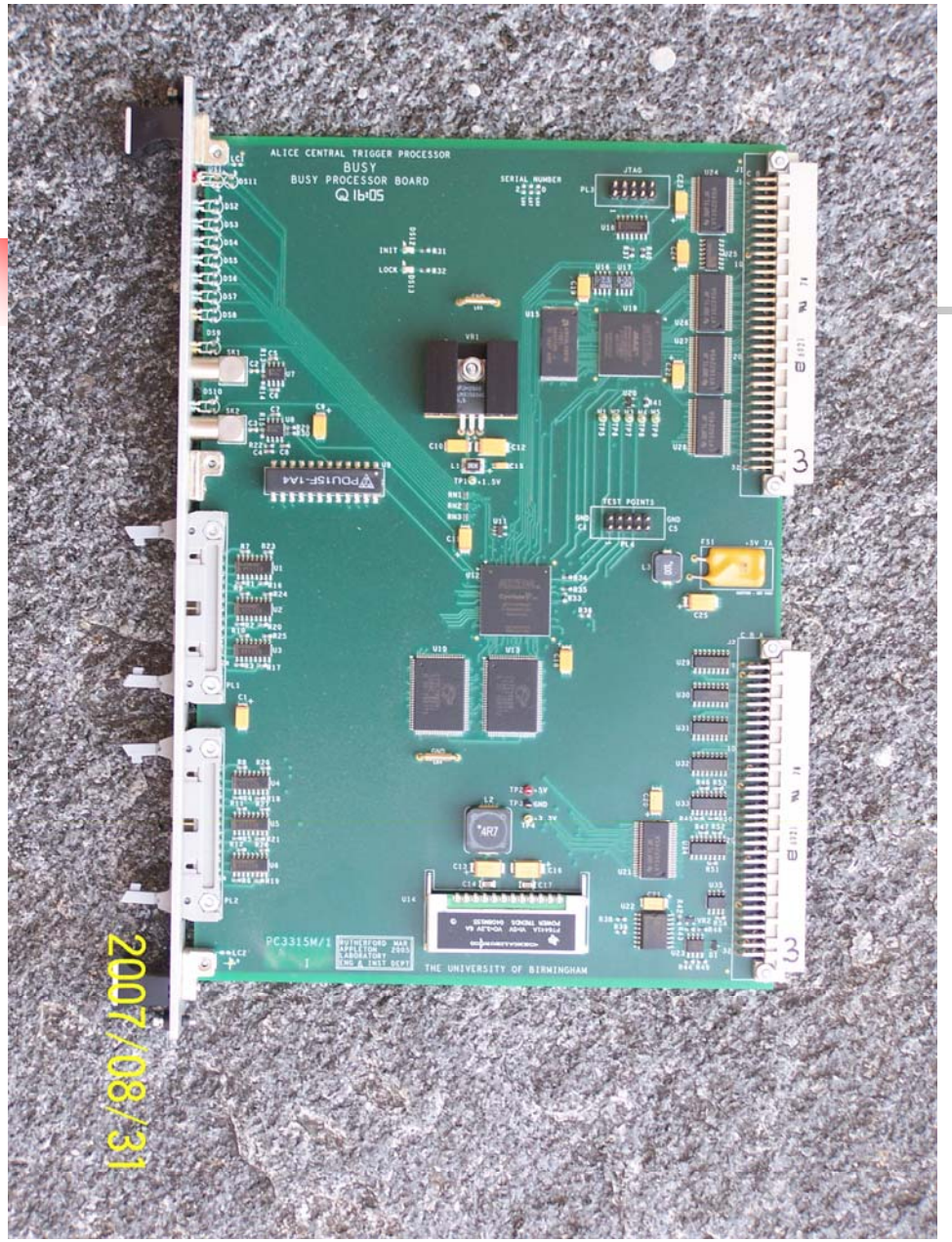
L0, L1, L2 boards

- Receives signals from trigger sub-detectors
- Compare received signals with defined classes
- Generate L0, L1, L2 triggers
- Serialize data and send them to the next level through VME backplane
- Past-future protection circuits
- Sampling memory for 26 ms



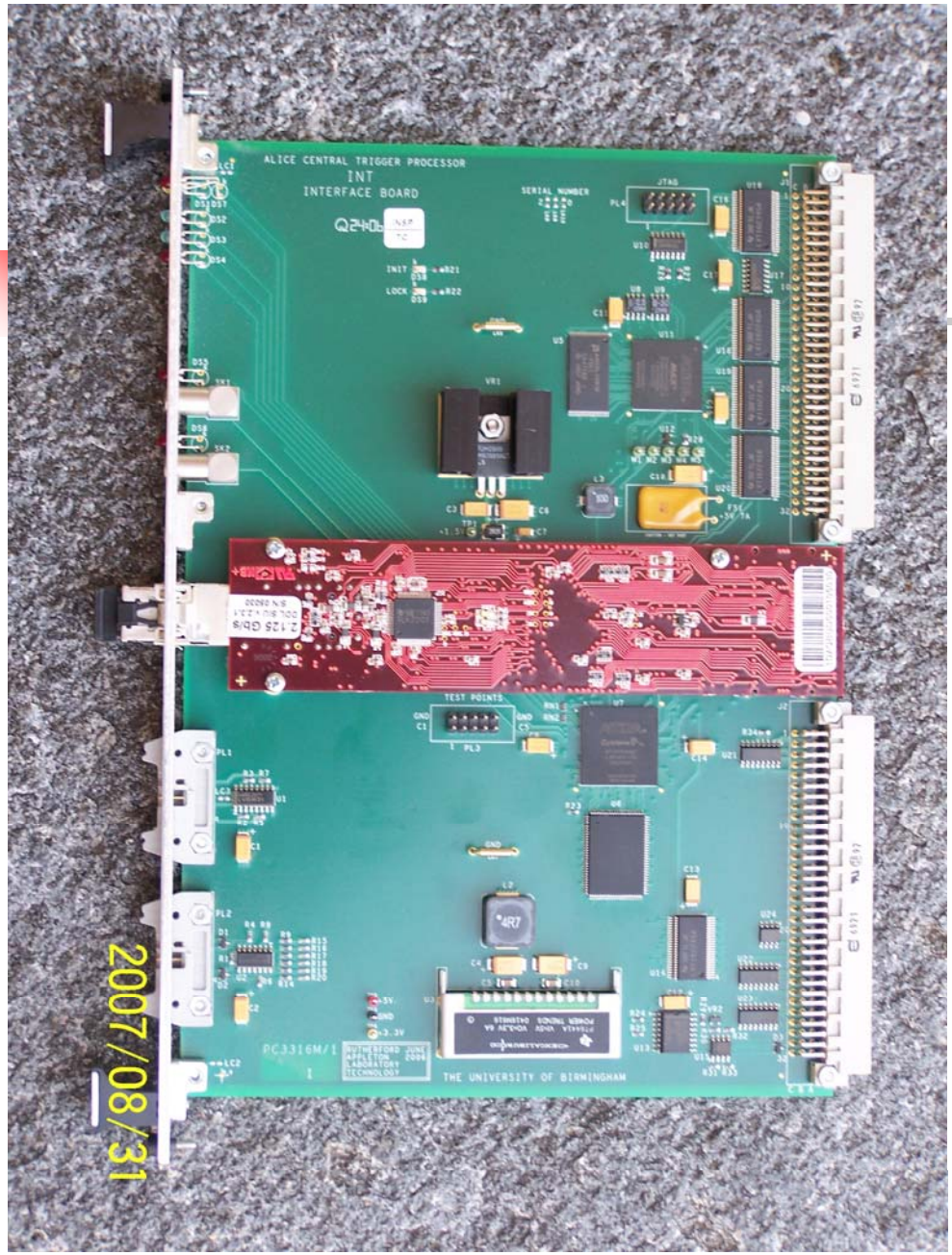
Fanout board

- Inside CTP is processing only classes and clusters
- In the Fanout board the clasters are converted into subdetector set of signals



BUSY board

- Receive BUSY signals from 24 sub-detectors
- Convert sub-detector BUSY signals to CLUSTER BUSY
- BUSY signals from sub-detectors that participate in a given cluster are all ***OR***ed together
- Generate CLUSTER BUSY for CTP

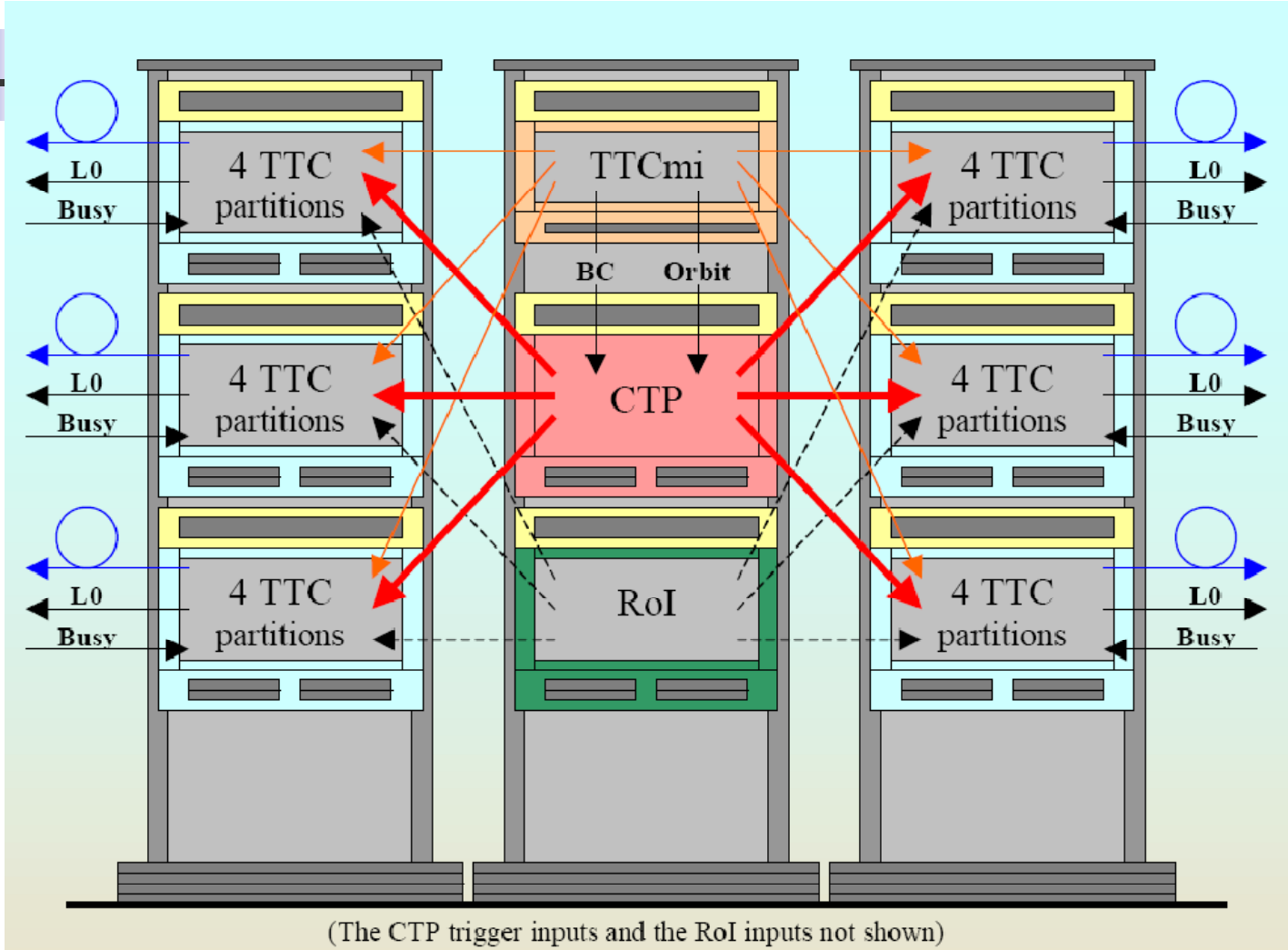


INT board

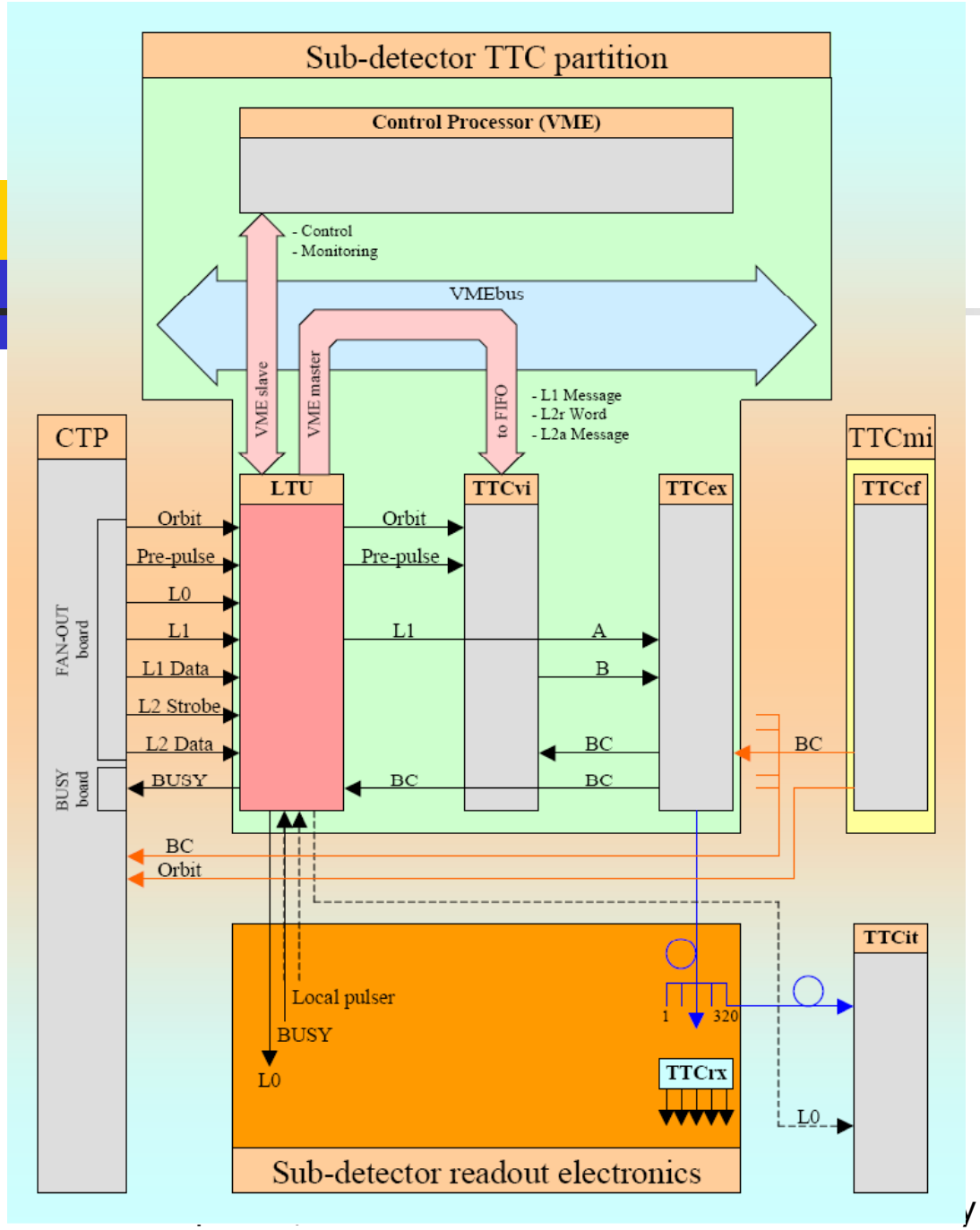
- Interface to DAQ –
1. CTP readout
2. Interaction record

- Trigger data are sent to DAQ System via SIU DDL module
- Reads SIU DDL busy and propagate it to the CTP

CTP connections

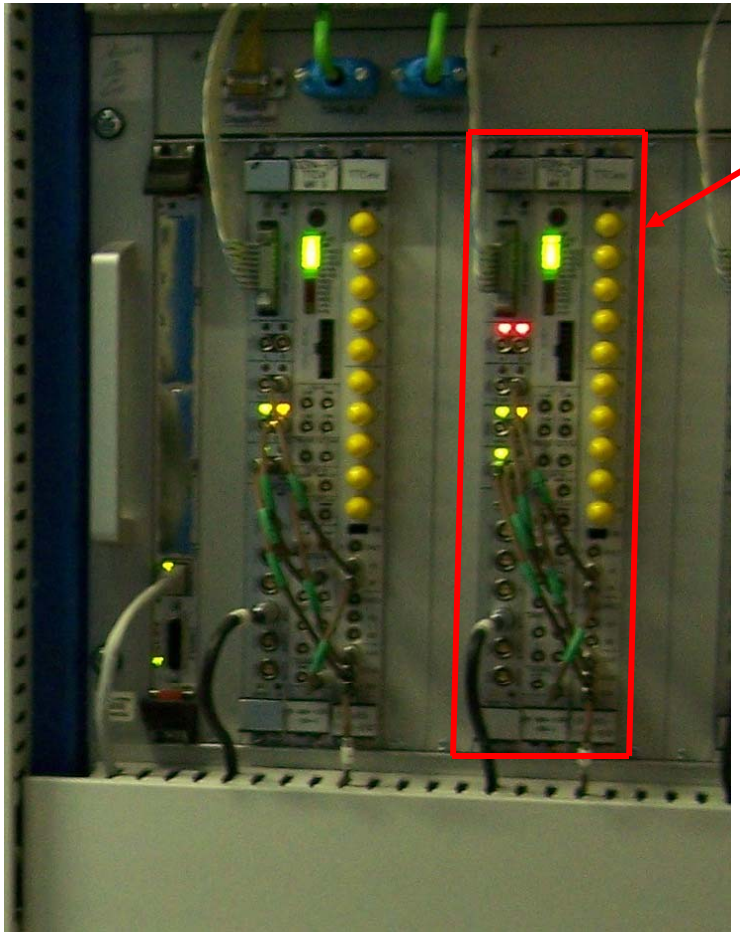


TTC partition

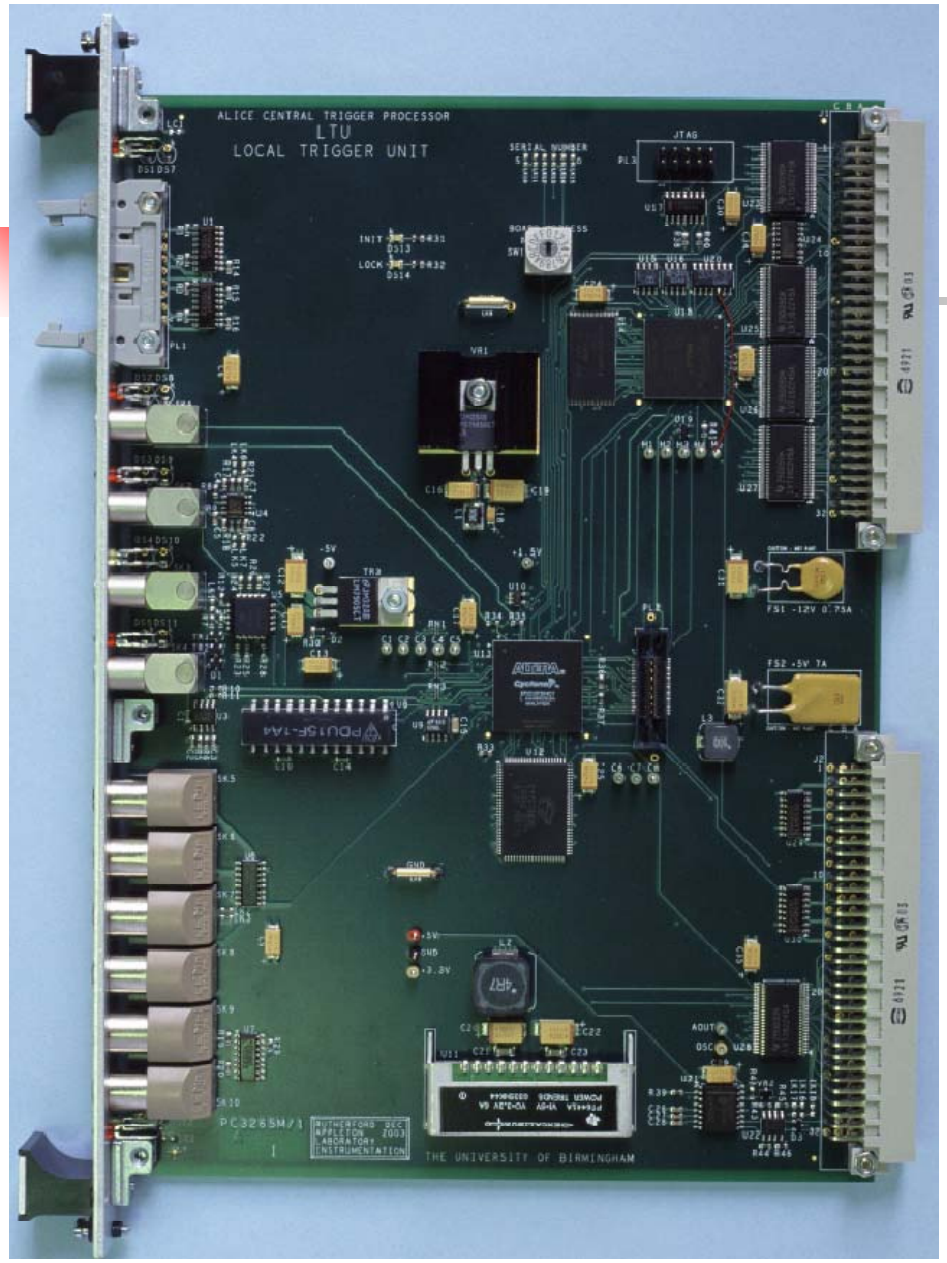


Each TTC partition contents:
- LTU board
- TTCvi board
- TTCex board

TTC partition in the experimental cavern



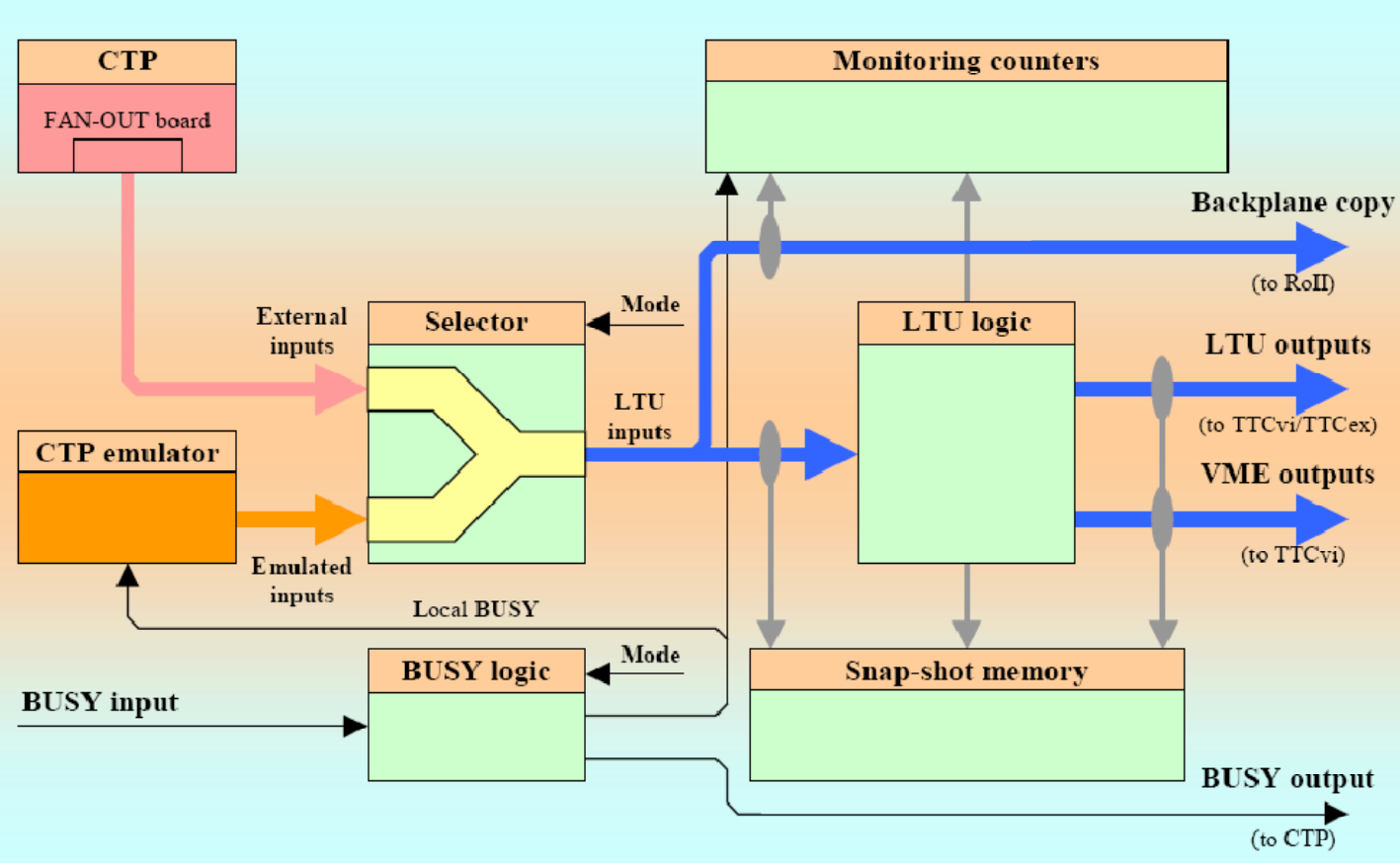
TTC partition:
- LTU board
- TTCvi board
- TTCex board



LTU board

- Serves as interface between CTP and detectors
- Global mode & standalone mode
- Emulation of CTP in the standalone mode – main functionality of LTU
- Each sub-detector can work on his own
- Receives BUSY from detector
- Sends BUSY to BUSY board (CTP)
- Sends L0 to detector through LVDS cable or through TTC system
- Sends L1 and L2 triggers though TTC system

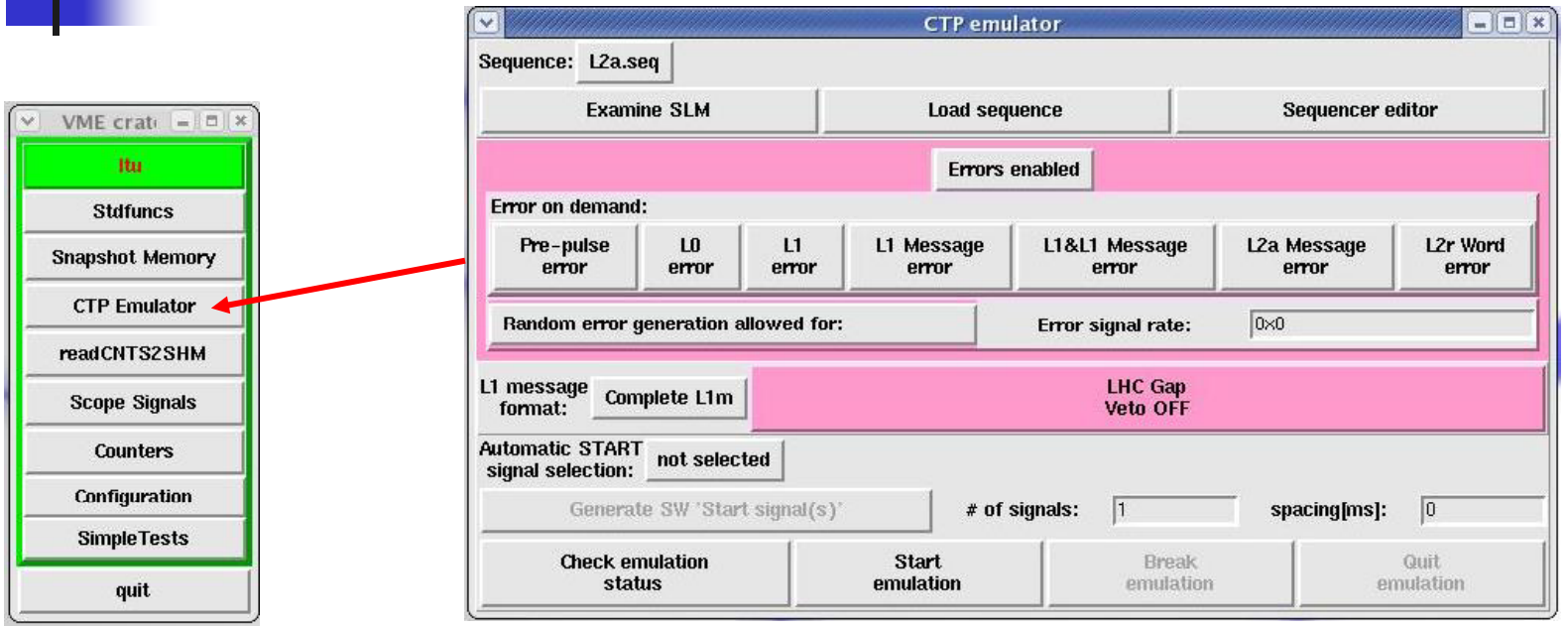
LTU board


CTP
FAN-OUT board
Monitoring counters
Backplane copy
(to RoII)
External inputs
Selector
Mode
LTU logic
LTU outputs
(to TTCvi/TTCex)
LTU inputs
CTP emulator
VME outputs
(to TTCvi)
Emulated inputs
Local BUSY
Mode
BUSY logic
Snap-shot memory
BUSY input
BUSY output
(to CTP)

Trigger data

- Trigger data are sent as TTC broadcasts with both **L1** and **L2** triggers
  - **L1** message: 5 words (each 4-bits address and 12-bits data) which content: calibration flag; readout control bits(4); segmented readout flag; L1 software class flag; L1 active trigger classes (50).
  - **L2a** message: 8 words (each 4-bits address and 12-bits data) which content: bunch crossing ID(12); orbit ID(24); calibration flag; L2 software class; L2 cluster mask (6); L2 active trigger classes (50).
  - **L2r** word (4-bits address and 12-bits data) which contents: bunch crossing ID(12).

LTU software



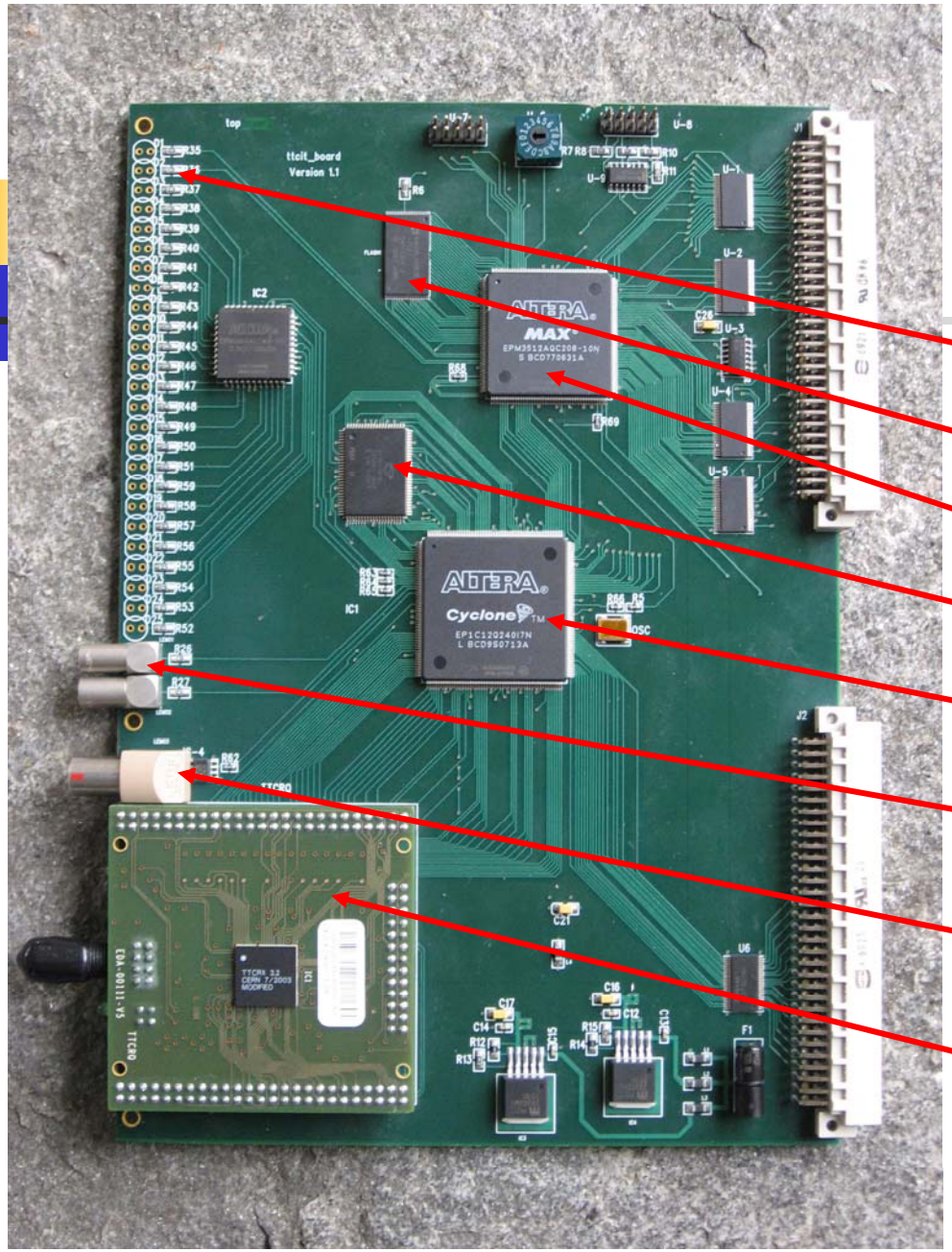
- Sequence execution triggered by **Start signal** derived from BC scaled down, random generator, external pulser or software request
- The LTU board can generate incomplete sequences or different types of errors can be introduced, either randomly or "on demand" with CTP emulator in LTU software

Newly developed TTCit board

Main functionality:

- Checking trigger sequences and detection of errors
- Indication of coming triggers and trigger errors on the front panel
- Counting triggers and trigger errors – counters accessible via VME bus
- Sampling trigger data into memory for offline analyze (26 ms)

TTCit board



23 LEDs for indication

Flash memory for config.

Altera FPGA for VME interf.

SRAM for sampling data

Altera Cyclone for TTCit functionality

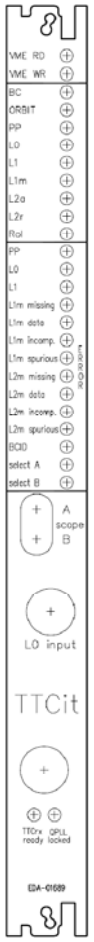
Lemo conn. for scope a,b

L0 input (LVDS)

TTCrq mezzanine board

6U VME board

TTCit front panel



VME access

Triggers

Trigger errors

Scope a, b outputs

L0 input

TTC input

The TTCit can be added, temporarily or permanently, to the sub-detector TTC partition (LTU, TTCvi, TTCex, TTCit)
or
it could also be installed separately, in *Personnel Accessible Areas,* for monitoring of the TTC operation during the physics run.

TTCit software

- HW counters for triggers and trigger errors
- Display snap-shot memory (SSM) content
- SSM analyzer – diagnostics of trigger sequences
- SOFT MONITOR - continuous scanning of SSM contents
- ONLINE MONITOR
- Scope signals
- Configuration – remote programming Flash memory and loading FPGA config.

Detection of trigger errors

- L0, L1 spurious
- L1 message: missing, data error, incomplete, spurious
- L2 message: missing, data error, incomplete, spurious
- PP error, CAL error
- BCID error

Status of project

- The ALICE Trigger system, including the Local Trigger Unit electronics, has been commissioned with all ALICE detectors on the surface
- All trigger electronics has been installed in the experimental cavern
- Integration and commissioning of the Trigger system with detectors in the experimental cavern is on the way

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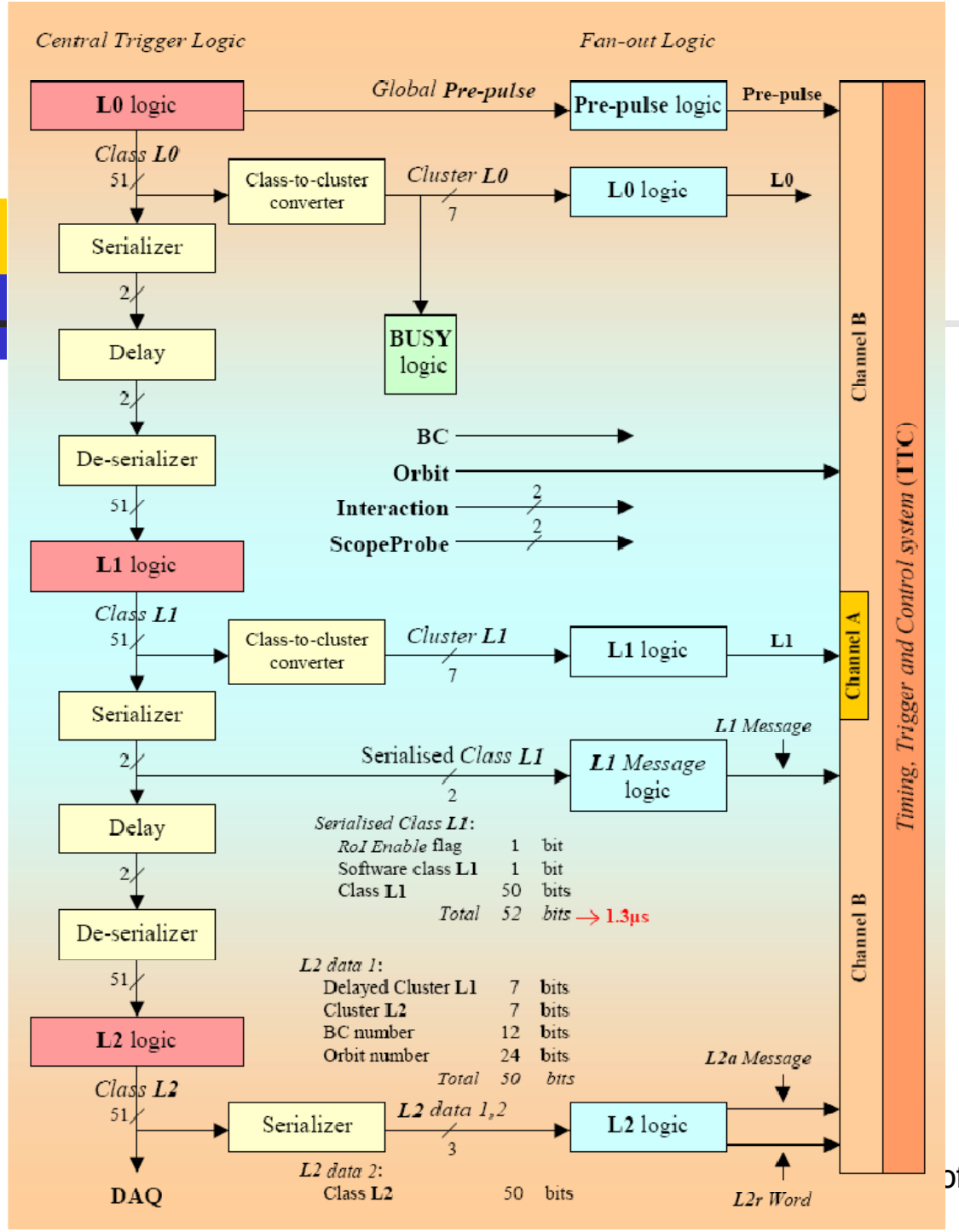
- Thank you for your attention

Spare slides

- Spare slides


Central Trigger Logic
Fan-out Logic
L0 logic
Global Pre-pulse
Pre-pulse logic
Pre-pulse
Class L0
51
Class-to-cluster converter
Cluster L0
7
L0 logic
L0
Serializer
2
Delay
2
BUSY logic
De-serializer
51
BC
Orbit
Interaction
2
ScopeProbe
2
L1 logic
Class L1
51
Class-to-cluster converter
Cluster L1
7
L1 logic
L1
Channel A
Serializer
L1 Message
2
Serialised Class L1
2
L1 Message logic
Delay
2
Serialised Class L1:
RoI Enable flag 1 bit
Software class L1 1 bit
Class L1 50 bits
Total 52 bits → 1.3µs
De-serializer
51
L2 data 1:
Delayed Cluster L1 7 bits
Cluster L2 7 bits
BC number 12 bits
Orbit number 24 bits
Total 50 bits
L2 logic
L2a Message
Class L2
51
Serializer
L2 data 1,2
3
L2 logic
L2 data 2:
Class L2 50 bits
DAQ
L2r Word
Channel B
Channel B
Timing, Trigger and Control system (TTC)

LTU board

- re-synchronisation of data and strobe signals
- de-serialization of the L1 Data and the L2 Data messages and their conversion into the adopted TTC format for the *L1 Message*, the *L2a Message* and the *L2r Word*
- queuing and temporary storage (FIFO) of the formatted TTC words
- control and arbitration of the FIFO read operation and transmission *via* the VMEbus to the TTCvi board