

The ALICE trigger electronics

Tuesday, 4 September 2007 16:20 (25 minutes)

The ALICE trigger system (TRG) consists of a Central Trigger Processor (CTP) and up to 24 Local Trigger Units (LTU) for each subdetector. CTP receives and processes trigger signals from trigger detectors and output from CTP are 3 levels of hardware triggers L0, L1 and L2. 24 trigger detectors are dynamically partitioned into up to 6 independent clusters. The trigger information is propagated through the LTUs to the Front-end electronics (FEE) of each subdetector via LVDS cable and optical fiber. The trigger information, which is sent from LTU to FEE can be monitored online for possible errors by the newly developed TTCit board.

After commissioning of TRG with each detector on surface, the ALICE trigger electronics has been installed and tested in the experimental cavern with appropriate ALICE experimental software. One setup is used for testing on the surface; the others are installed in experimental cavern.

This paper describes the current status of ALICE trigger electronics, online error trigger monitoring and appropriate software for this electronics.

Summary

The ALICE trigger system operates with interaction rates for nucleus-nucleus, proton-nucleus and proton-proton runs between about 8 kHz and 300 kHz. The main block of the ALICE trigger electronics is the Central Trigger Processor (CTP). The CTP is implemented using 6 different types of 6U VME board, together making up eleven active boards for the CTP. This block will receive and align up to 60 trigger inputs in parallel from the trigger detectors; it then processes trigger information inside cluster and generates result of processing. There are three different trigger levels (L0, L1 and L2) with latencies from 1.2 microseconds to 88 microseconds. The system allows dynamic partitioning in order to make optimum use of detector readout. The system provides a flexible past-future protection. The L0 trigger is sent as an LVDS signal or optionally via the Channel A of the TTC system. The L1 signal is sent on channel A of the TTC system and trigger data associated with level 1 are sent as a message on channel B of the TTC system. The L2 trigger is sent as a message on the TTC system after a delay, currently 88 microseconds, to allow for the longest required past-future protection interval.

Outputs from the CTP go to the LTUs of each subdetector. The LTU serves as an interface between the CTP and the subdetector readout electronics. The LTU is able to run also in the stand-alone mode of operation and the LTU fully emulates the CTP protocol and enables sub-detectors to carry out development, test and calibration tasks independently of the CTP. The timing of emulated trigger sequences is identical to the timing during the global run. The LTU can generate incomplete sequences or different types of errors can be introduced, either randomly or "on demand" (the option is available in both the global mode and the stand-alone emulation mode), all in order to verify the capability of the FEE to check the consistency of trigger information.

The trigger electronics is based on ALTERA Cyclone FPGAs (Field Programmable Logic Arrays), which provide flexibility to change the functionality of the trigger system by reprogramming FPGA. The system provides a range of monitoring and debugging options. Snap-shot memories enable detection of any system inconsistency and an identification of possible faults. Around 1200 counters, including many redundancies, are read in regular intervals (1 minute), which

provides relevant physics information and also verify the consistency of the hardware operation.

In order to monitor and recognize possible errors in the trigger timing and the errors in trigger messages the TTCit board has been developed. The board can monitor the optical output of a trigger partition. In case of an error the information is displayed on the front panel. For detailed information and a precise identification of errors, a snap-shot memory can be read-out. The snap-shot memory contains information triggered by error in tree modes: pre-trigger, middle-trigger or post-trigger.

The ALICE Trigger system, including the Local Trigger Unit electronics, has been commissioned with all ALICE detectors on the surface and in the pit in parallel. Currently it is installed in the cavern where the full system is integrated with appropriate experimental software (Trigger - TRG, Experiment Control System - ECS, Data Acquisition System - DAQ and Detector Control System - DCS).

Primary author: KRIVDA, Marian (University of Birmingham, UK)

Co-authors: BHASIN, A. (University of Birmingham, UK); JUSKO, A. (University of Birmingham, UK); LAZZERONI, Cristina (University of Birmingham, UK); EVANS, D. (University of Birmingham, UK); JONES, G.T. (University of Birmingham, UK); KRÁLIK, I. (Institute of Experimental Physics, Košice, Slovakia); URBÁN, J. (P.J. Šafárik University, Faculty of Science, Košice, Slovakia); ŠÁNDOR, L. (Institute of Experimental Physics, Košice, Slovakia); VILLALOBOS BAILLIE, O. (University of Birmingham, UK); JOVANOVIĆ, P. (University of Birmingham, UK); LIETAVA, R. (University of Birmingham, UK)

Presenter: KRIVDA, Marian (University of Birmingham, UK)

Session Classification: Parallel session B3 - Trigger 3