Commissioning of the Jet/Energy-sum and Cluster Processors for the ATLAS Level-1 Calorimeter Trigger System

ATLAS Level-1 Calorimeter Trigger Collaboration

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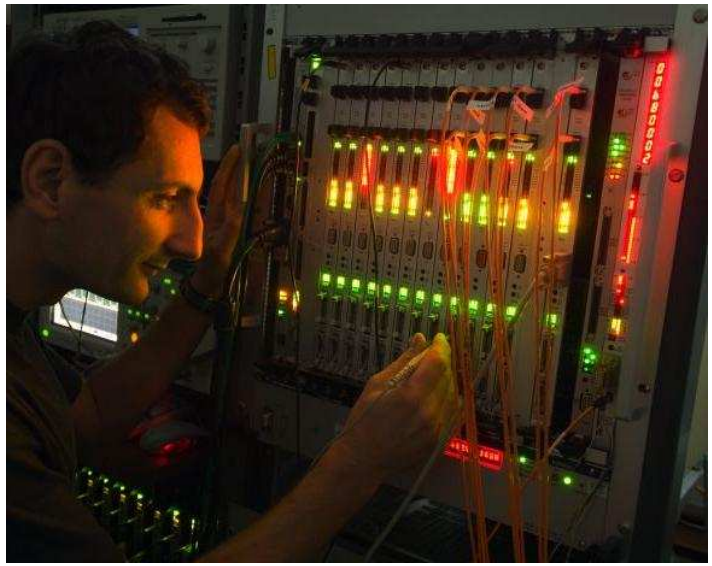
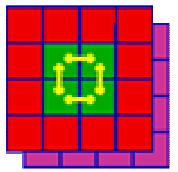


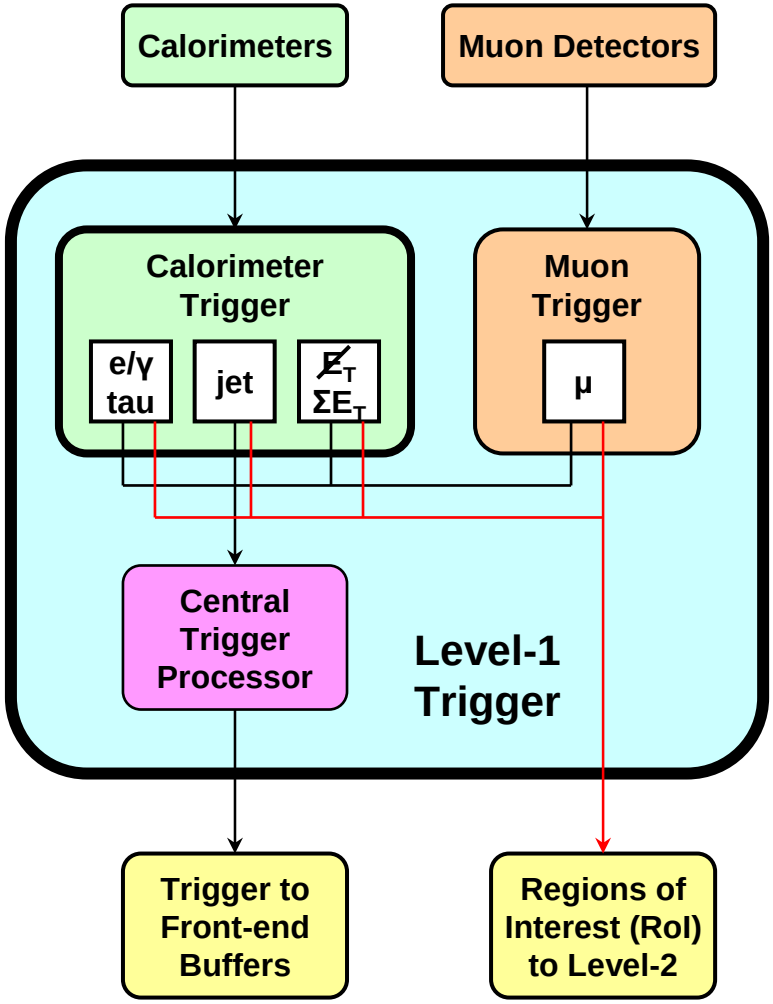
Commissioning Experience with the ATLAS Level-1 Calorimeter Trigger System



- Trigger Architecture
  - Algorithm
  - I/O
- Commissioning and Integration
  - Installation
  - Problems
  - Integration into ATLAS Data Acquisition
  - M4 commissioning run (cosmic ray) results
- Lessons Learnt

Level-1 triggering in ATLAS

- Three-stage triggering system
  - Level-1: custom-built hardware, fixed latency – target rate 75 kHz
  - Level-2: mostly software, RoI-based selection – target rate 1000 Hz
  - Event Filter: software, full detector – target rate 200 Hz
- All data buffered at bunch-crossing rate of 40 MHz for 2.5 μs
- Level-1 has three sub-systems:
  - Calorimeter Trigger
  - Muon Trigger
  - Central Trigger (CTP)



Calorimeter Trigger Architecture

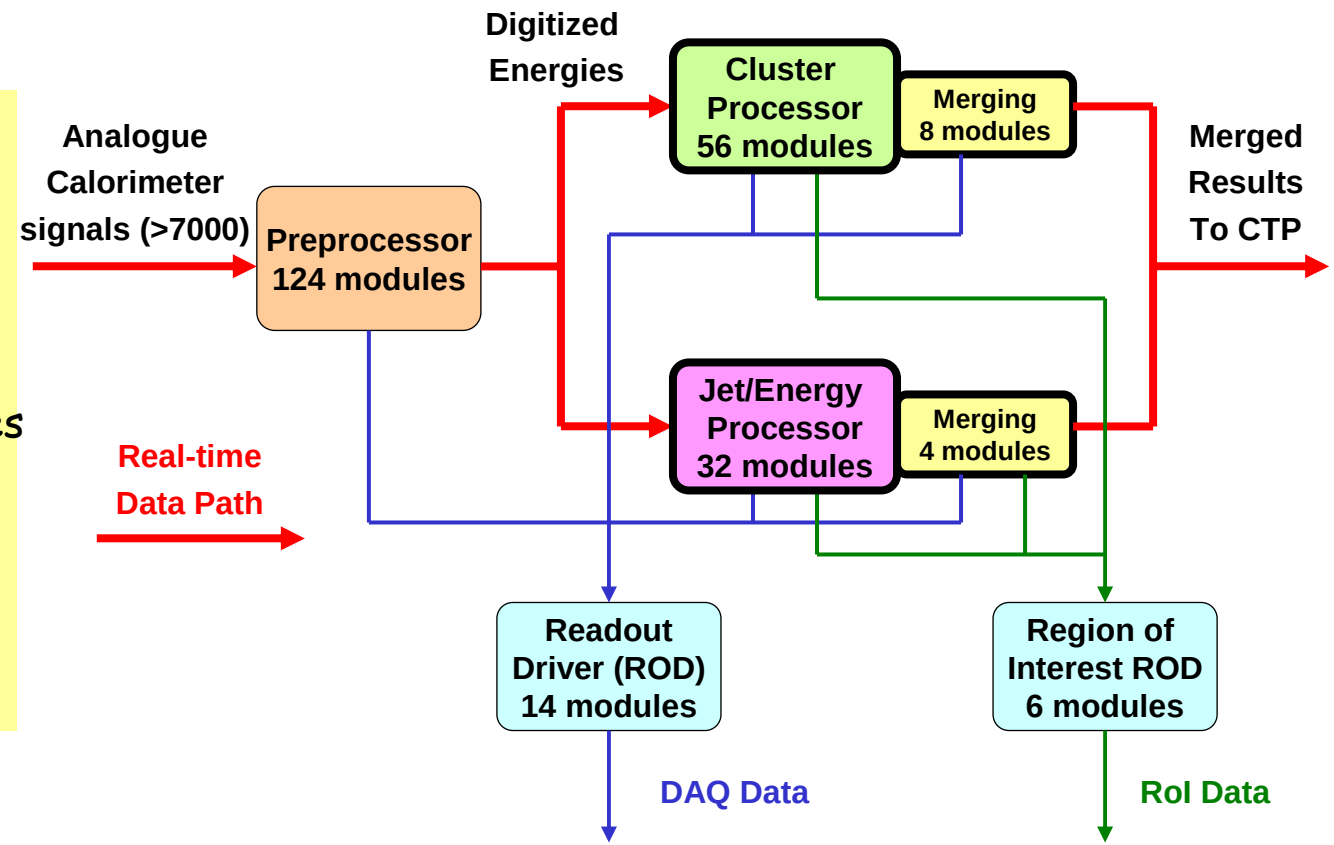
Features:

Real-time Path: Fixed Latency (~1μs)

Many processing stages

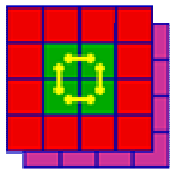
Massive parallelism

Heavily FPGA based



Five Main Types of Custom 9U Modules: **PPM** **CPM** **JEM** **CMM** **ROD**

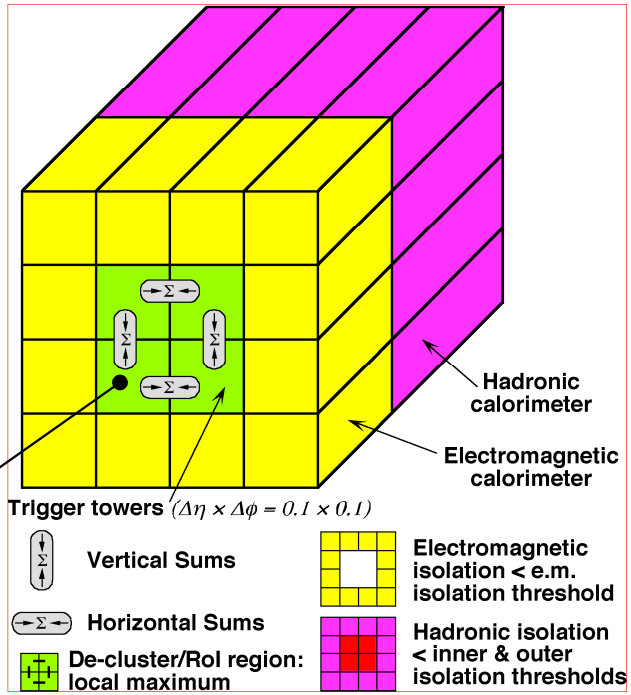
Physics Algorithm



- Processor input is a matrix of tower energies
- Physics algorithms use 4x4 grid
- To process each location, an outer environment is required
- Algorithm windows overlap and slide by 1 trigger tower in both coordinates.

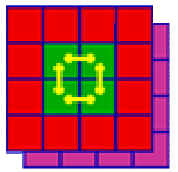
Reference cell

Electron/photon Algorithm

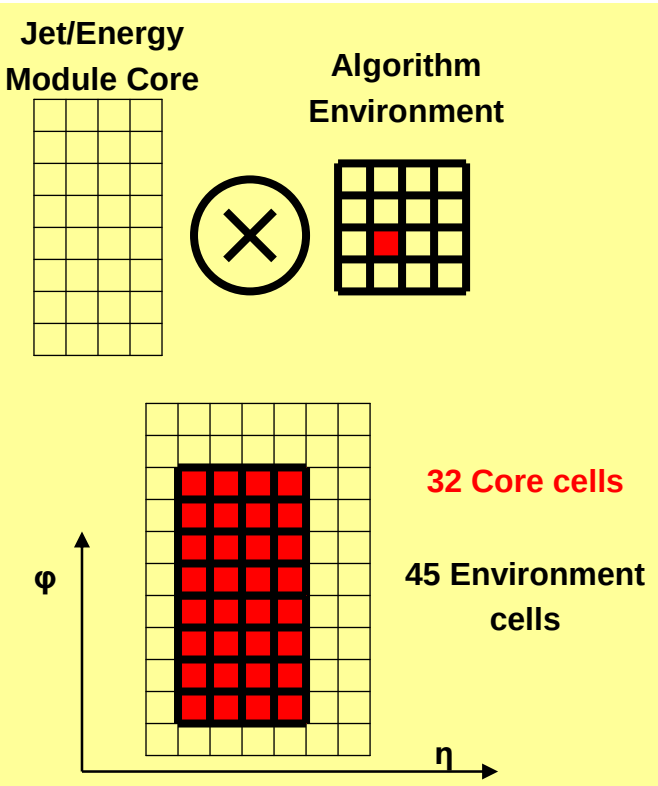


Tau/hadron algorithm adds 1x2/2x1 e.m. clusters to 2x2 inner hadronic region. Isolation uses e.m. and outer hadronic 'rings'.

Trigger-Tower mapping to Processor Modules



- Physics algorithms use 4x4 grid
  - 2-D / 2.5-D pattern recognition
  - Applied throughout full input matrix
  - Windows overlap in both coordinates (eta and phi)
- To process each location, an outer 'environment' is required
- Each processor (module, crate) has a core of towers processed with 'environment' achieved by duplication (fanout) of data.

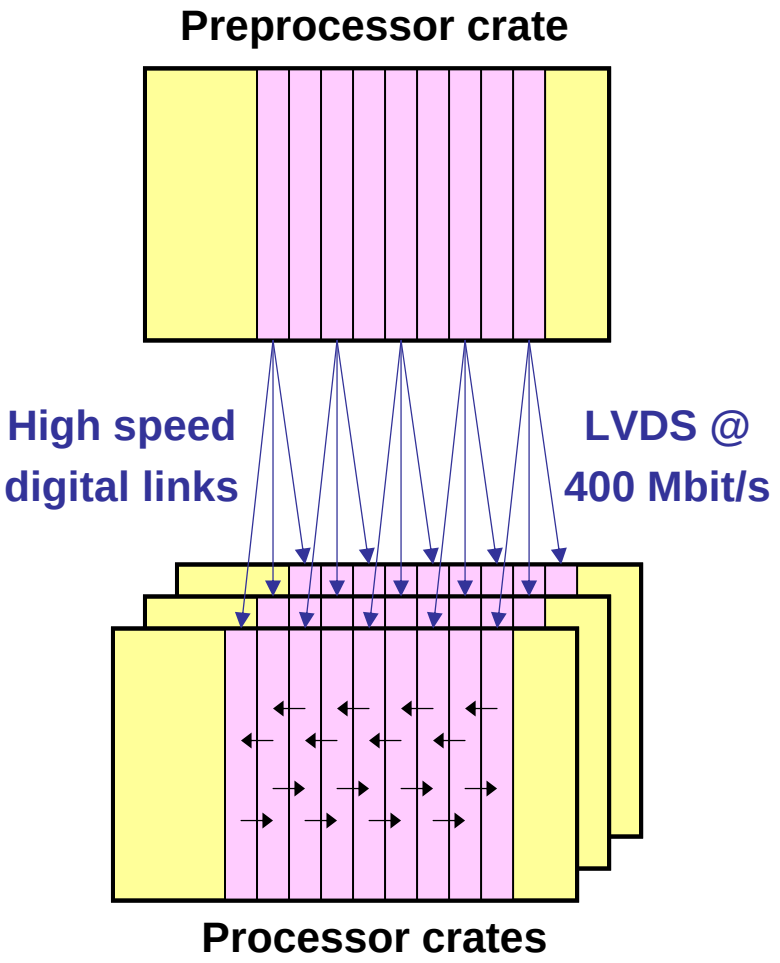


jet/energy-sum module (4x8) 32:45

e/gamma/tau cluster module (4x16) 64:69

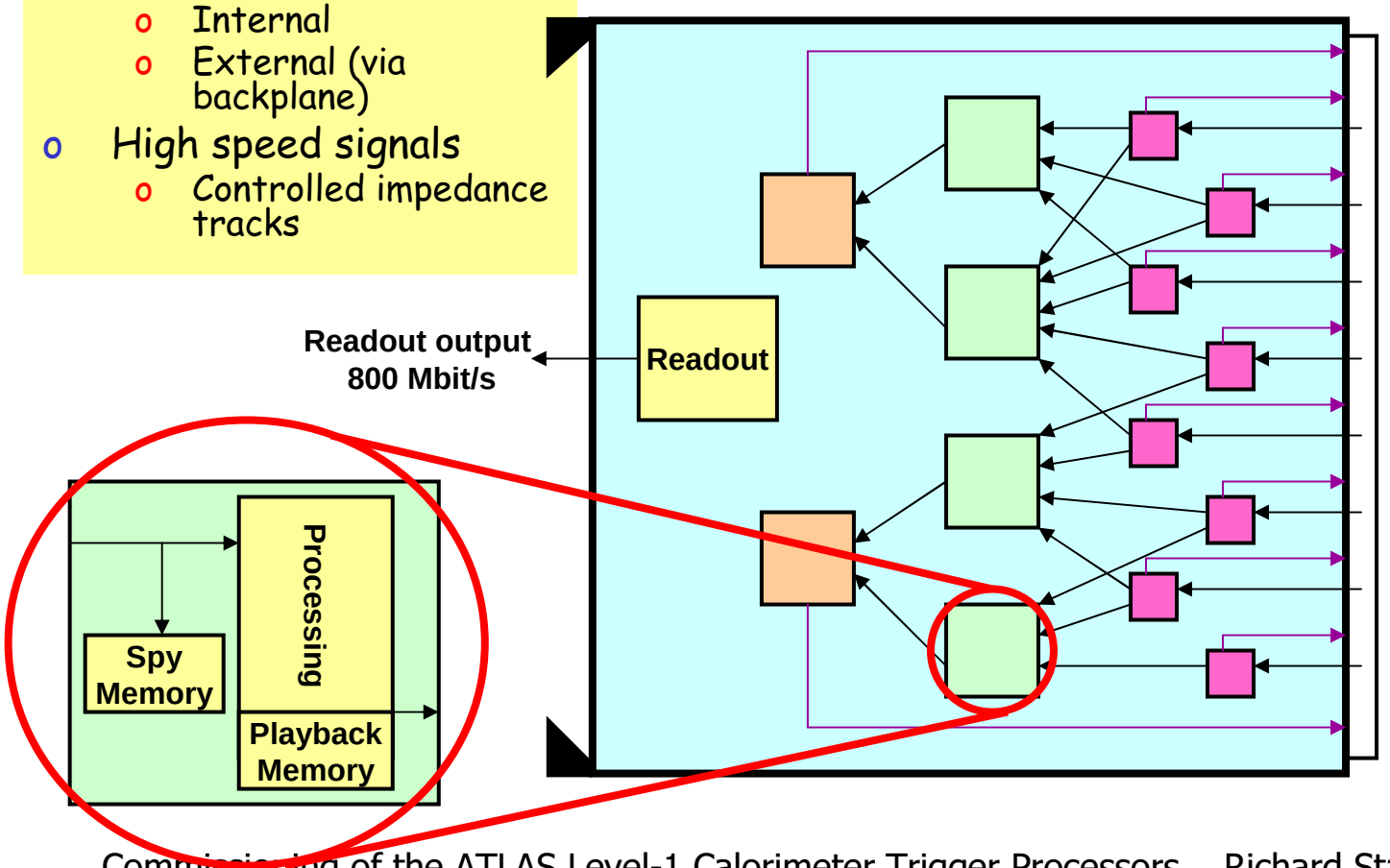
Solution and implications

- Preprocessor feeds high-bandwidth serial links to:
- Parallel Processor
  - Four 9U VME crates (Quadrants) for e/gamma/tau trigger
  - Two 9U VME crates for jet/energy-sum trigger
- Necessary fanout performed via:
  - Digital cables to processors
    - Quadrant boundary (fanout in phi)
  - Custom backplane in processor crate
    - In other dimension (fanout in eta)



Processor Module Design

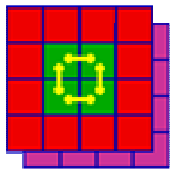
- Many FPGAs
- High connectivity
  - Internal
  - External (via backplane)
- High speed signals
  - Controlled impedance tracks



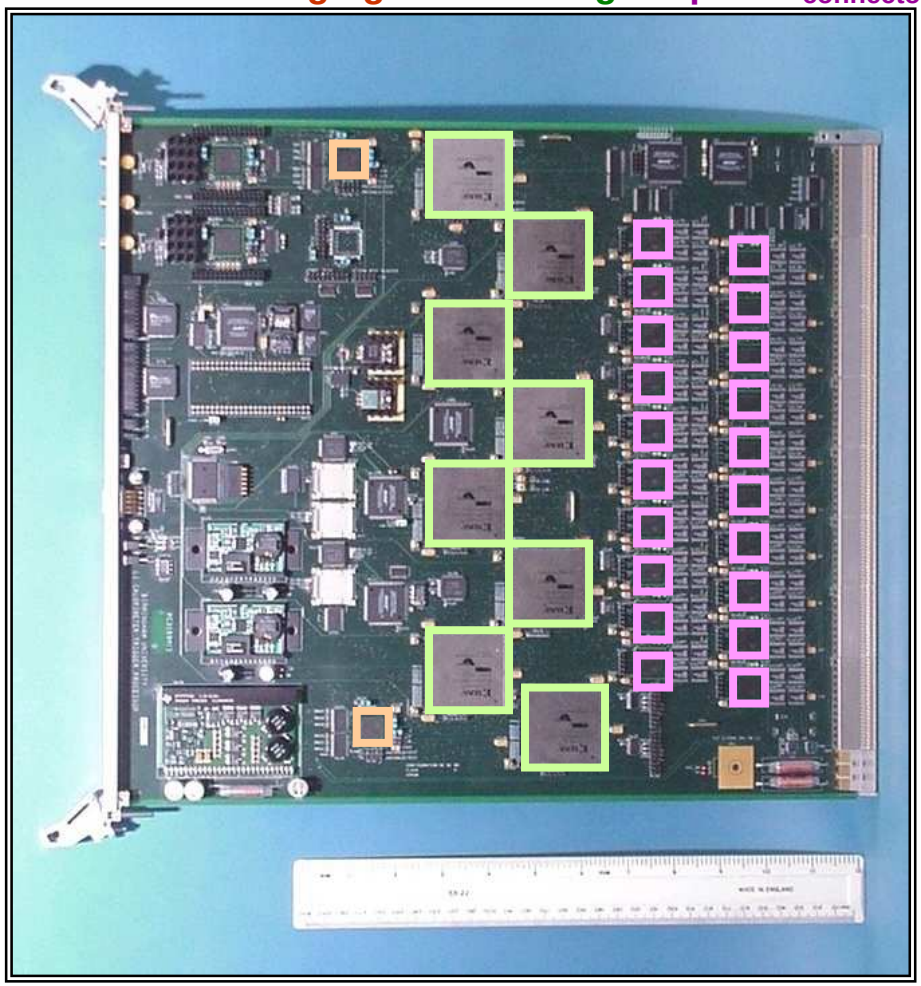
High Density Backplane Connector (~1150 pins)

Signal Speeds up to:
400 Mbit/s differential
160 Mbit/s single ended

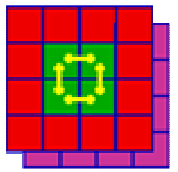
A real example: the Cluster Processing Module



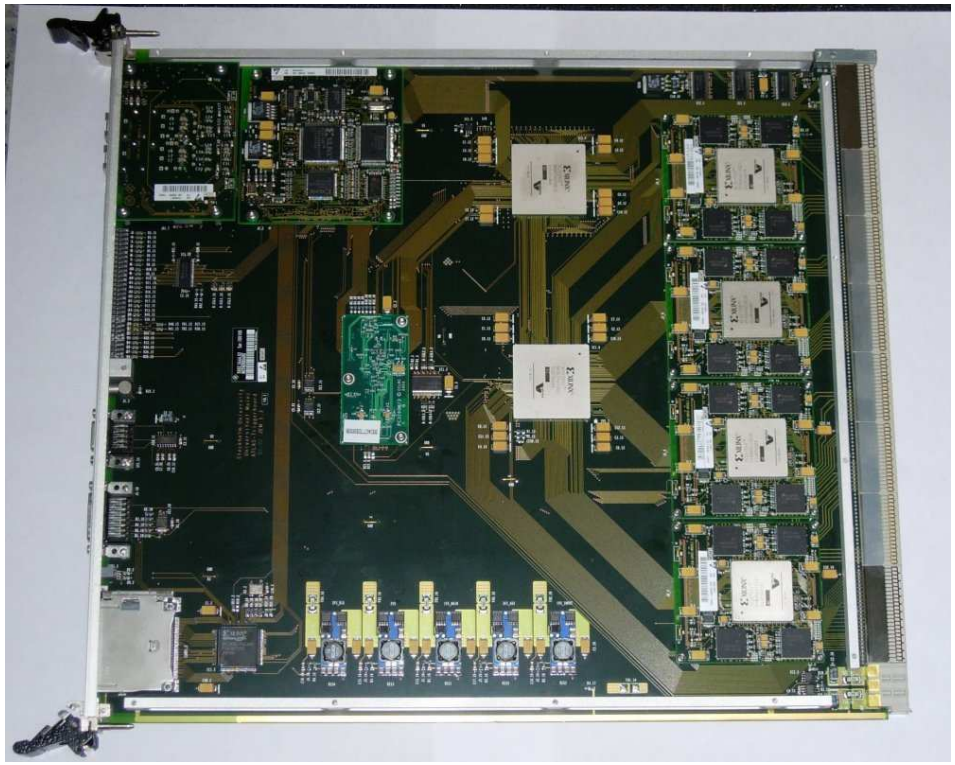
- Backplane Connector i/o
  - Input: ~58 Gbit/s
  - Output: ~28 Gbit/s
- Input Stage:
  - 20 FPGAs
- Processing Stage:
  - 8 FPGAs
- Merging Stage:
  - 2 FPGAs
- Modules in system: 56



Another real module: the Jet / Energy-sum Module



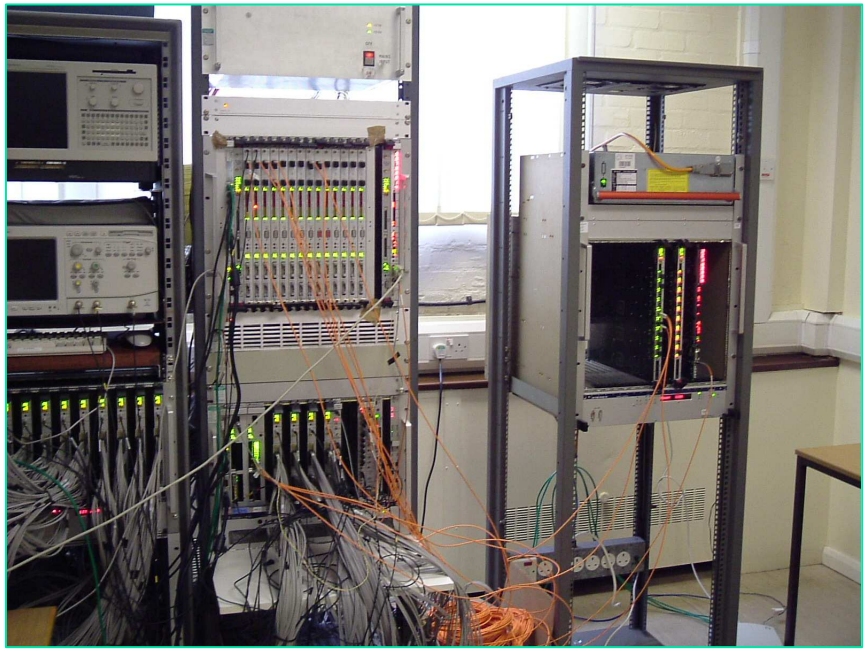
- Backplane Connector i/o
  - Input: ~ 45 Gbit/s
  - Output: ~ 15 Gbit/s
- Input Stage:
  - 4 FPGAs
- Processing + Merging Stage:
  - 1 FPGA Jet
  - 1 FPGA Sum
- Modules in system: 32



Module Production Tests

Pre-installation testing:

- Manufacturing checks
  - Visual checks
  - JTAG / BS
- Comprehensive tests at Home Institutes
  - Modules tested within subsystems
  - Complete crates built



Installation in USA15

e/gamma/tau Trigger

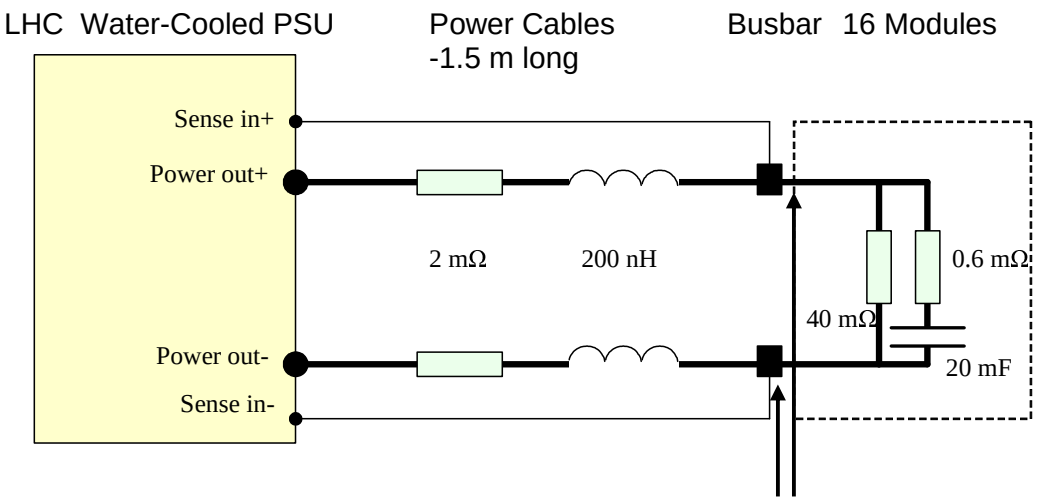
- 3/4 Crates commissioned

Jet/Energy –sum trigger

- 2/2 Crates commissioned

(1 crate holds 2 Quadrants)

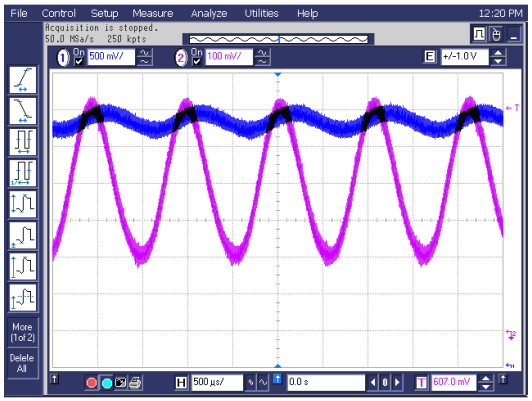
Crate Power Supplies



Large phase shift (120°) in power feed circuit due to cable inductance and module decoupling capacitance

At certain frequencies PSU sense input sees feedback as positive

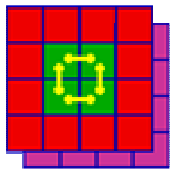
→ OSCILLATIONS



3.3 V ± 100mV

40 A ± 20 A

Crate Power Supplies



Solutions to prevent Oscillation:

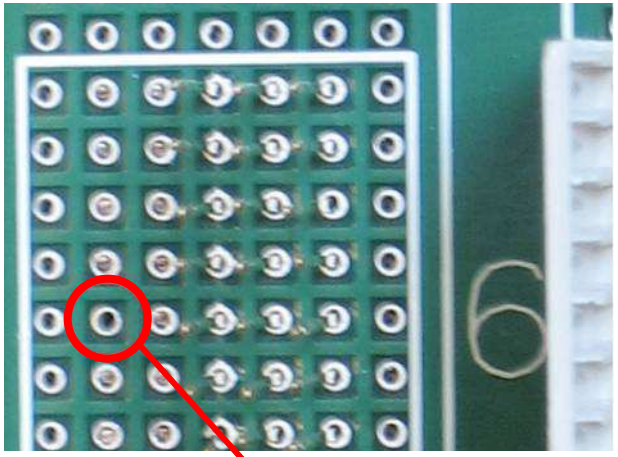
- Modify modules to reduce load capacitance
- Tie power-ground cables pairs together to reduce loop inductance

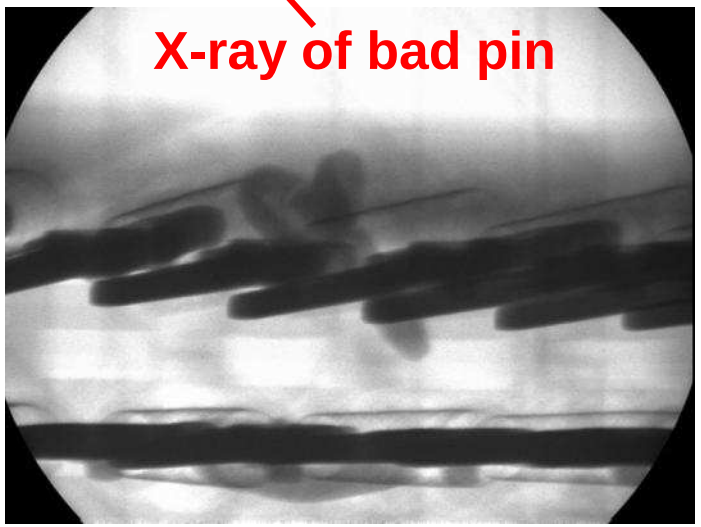
- Change to local sensing rather than remote
- Use extra-thick power cable – IR drop < 100mV

- PSU manufacturer investigating control circuit

Backplane Problems and Status

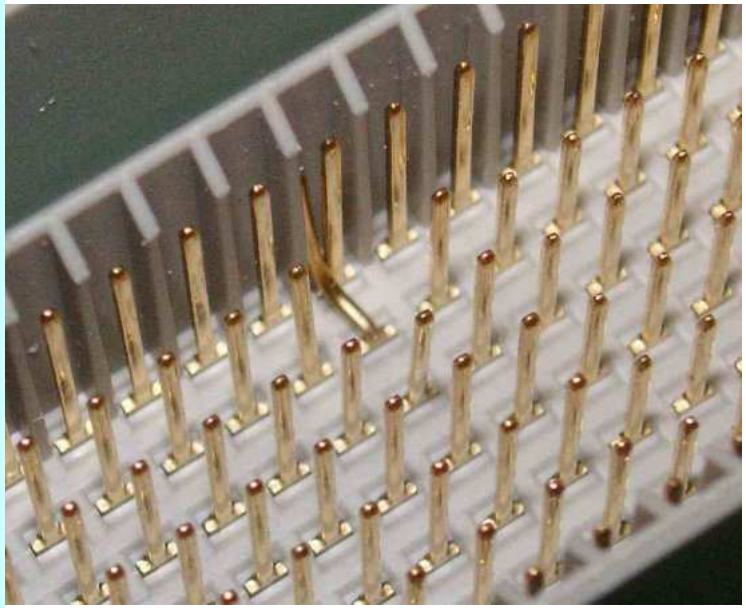
- Dense, high bandwidth backplane
  - About 1,150 pins per slot
  - About 22,000 pins in all
- After production, pin problems at ~0.01% level
  - ie about 1-2 errors per backplane!
- Pins bent during insertion of connectors into PCB
- Successfully replaced all bad connectors





Backplane Problems

- 1 pin damaged during module insertion.
  - Very high insertion force (estimated 370 N)
  - Module guide pegs reduce risk.
- Tools for replacing individual pins (Harting & AMP/Tyco)
  - Backplane has to be removed in most cases



Installation Reality Check: Digital Cabling into Processor Crates

1368 individual LVDS signals into one JEP crate

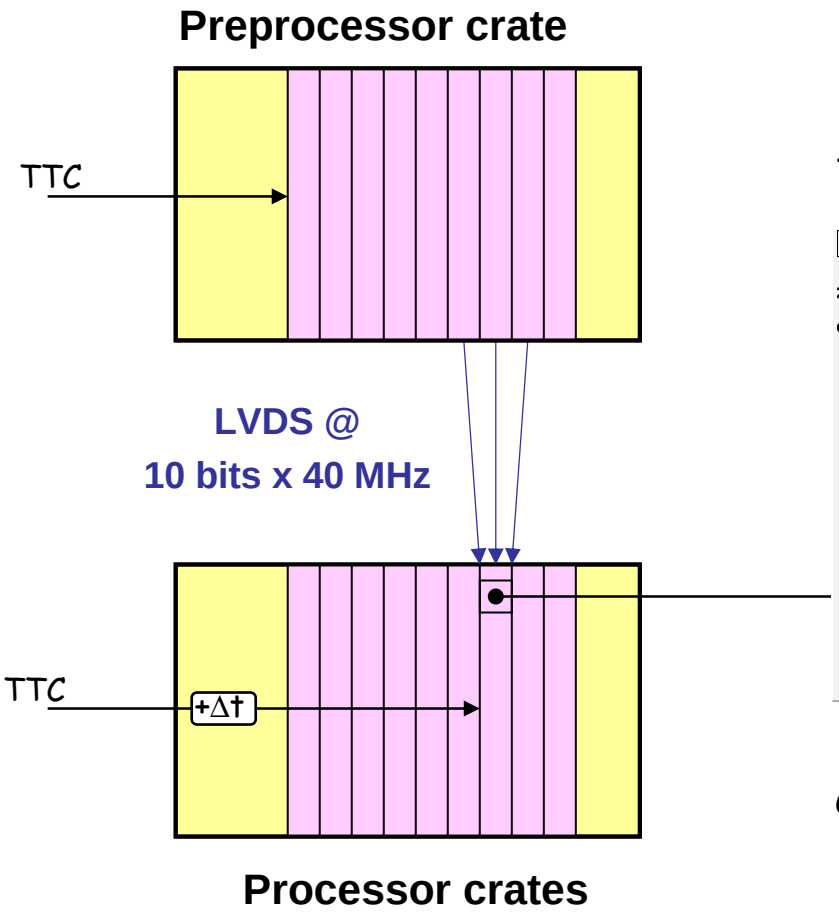
Input data bandwidth = 547 Gbit/s

Observed anti-static precautions to avoid damaging electronics (Cable discharge events)

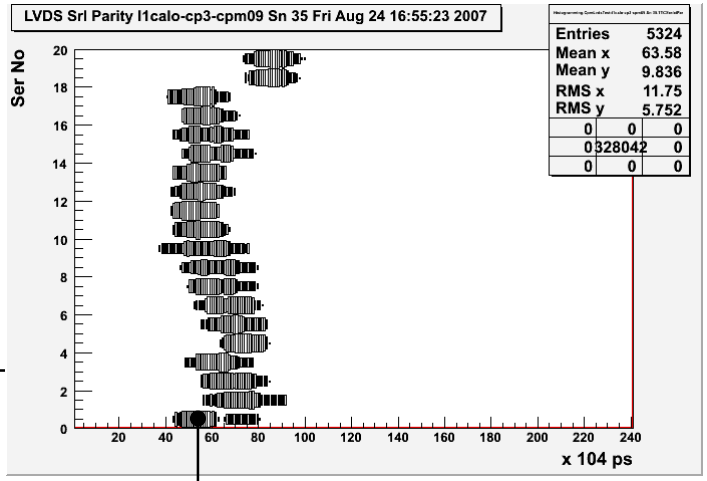
Status -Have tested 1/3 of cables

- No 'Swaps'
- 1 possible fault

Timing of incoming LVDS links



Timing Scan – Error Count per Serialiser

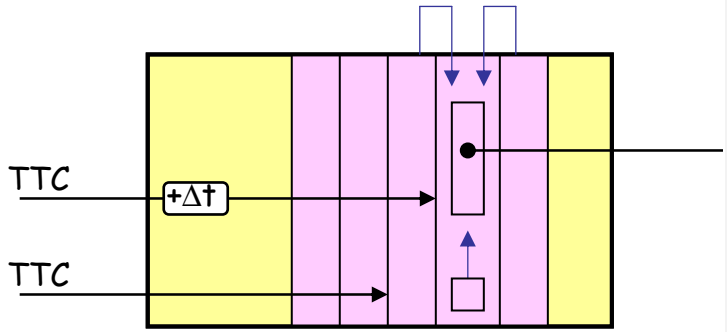


Group of 4 links

18 ns error free

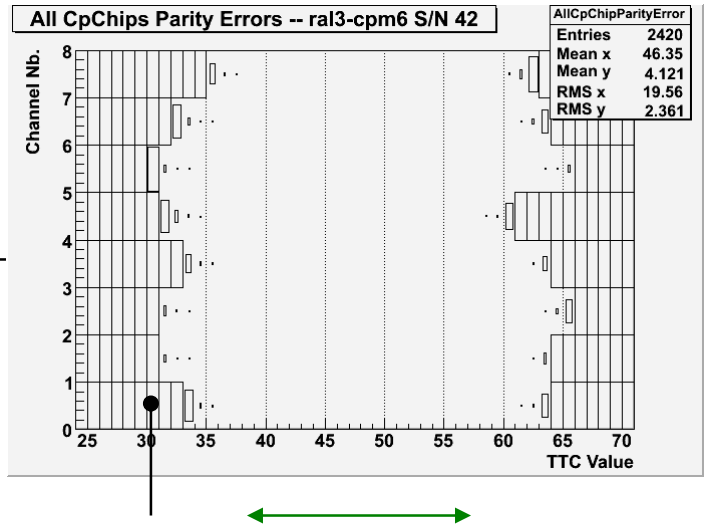
Timing of 160Mb/s links

Onboard and backplane I/O @160 Mb/s
Into all Cluster Processor chips



Processor crate

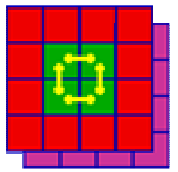
Timing Scan – Error Count per CP Chip



1 CP chip
108 inputs

2 ns error free

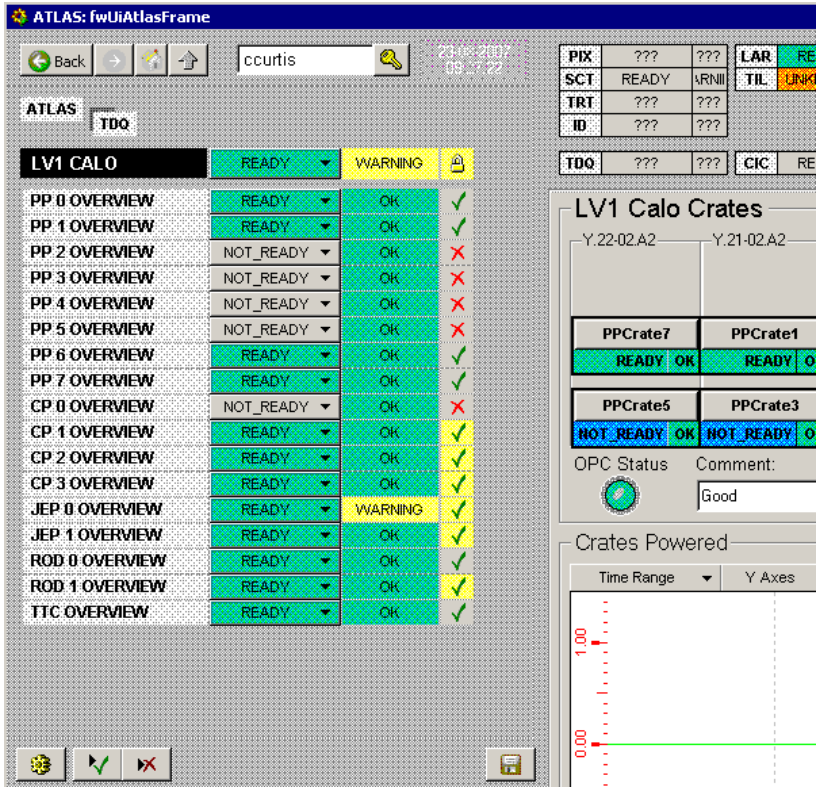
Integration into ATLAS infrastructure



- Tests of output to all downstream hardware performed in situ
  - Simple setups for the moment
- Links to Readout System and Region of Interest Builder showed no data corruption
  - Tested at high rates
- Real-time links to Central Trigger Processor
  - Commissioned

DCS Integration

- All crates are now connected to the global DCS (Detector Control System).
- Every module contains a CAN µC which reports voltage, current and temperature (CANopen)
- Most of the modules are visible to the global control stations. Work in progress.

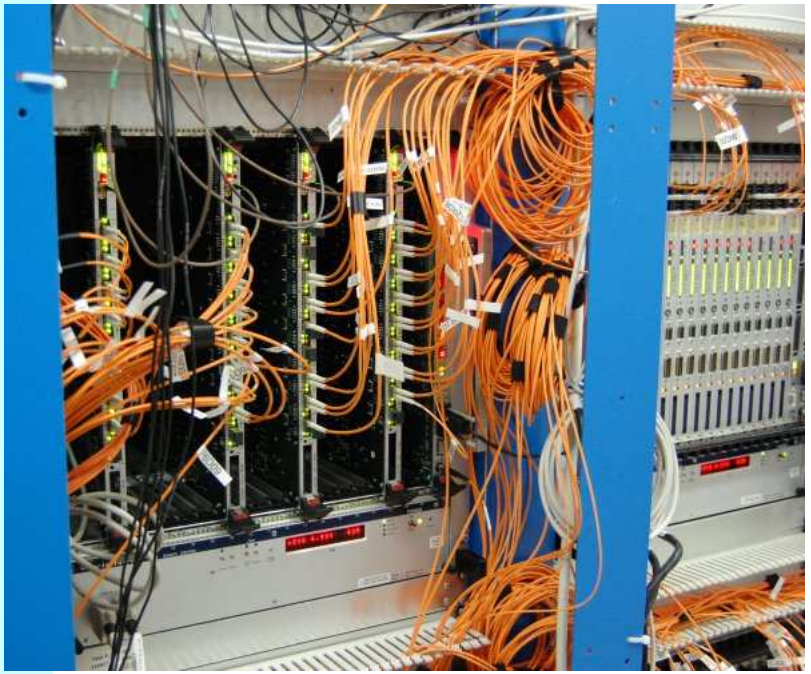


View from ATLAS Control room

M4 Commissioning run

Hardware

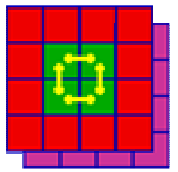
- Processors
  - 4/8 PPr crates
  - 2/2 JEP crates
  - 3/4 CP crates
- 9 ROD Modules
  - JEP 1 DAQ + 1 ROI
  - CP 2 DAQ + 1 ROI
  - PPr 4
- DCS operational



ROD crate (1 of 2)

JEP crate (1 of 2)

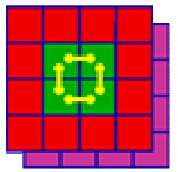
M4 Commissioning run



Hot News

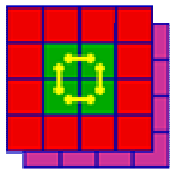
- L1Calo joined combined M4 run contributing triggers
- Stable , reading-out > 100 modules ≈ ½ of final system
- Detector signals aligned using calibration pulses
- Have seen cosmic data from calorimeters
- Data sent to RoI builder. Recorded and verified OK

Lessons Learnt



- Don't underestimate cable installation
- Test using actual power supplies ASAP
- Consult mechanical engineer

Lessons Learnt



What would we do differently (if timescales permitted)

- Use newer larger faster FPGAs
  - Larger trigger-tower coverage – less signal duplication
    - Benefit PCB layout
  - More clock resources
    - Improved timing margins
  - Faster I/O - Run LVDS directly into Processor Chips
    - Remove De-serialisation/ Re-serialisation
    - Reduce trigger latency
- Use higher bandwidth connectors and backplane links
  - Gbit/s differential
    - Reduce Backplane Pin-count – lower insertion force