Integration of the CMS Regional Calorimeter Trigger Hardware into the CMS Level-1 Trigger

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Abstract

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid (CMS) Experiment have been produced and tested. The RCT hardware consists of 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8 bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing. Integration tests with the TPG and GCT subsystems have been successful.

Before installation, the RCT was part of the CMS Magnet Test and Cosmic Challenge as part of trigger for the HCAL. Now, installation is complete and commissioning of the final system is underway. Pattern tests are used to validate 1026 TPG links and 108 GCT cables as well as test slices of the calorimeter trigger system. These tests and future tests including CMS Global Runs, their results, and the RCT installation will be described.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) is a general-purpose detector that will operate at the Large Hadron Collider (LHC). Its construction is nearly complete at the European Laboratory for Particle Physics (CERN) near Geneva, Switzerland. This large detector will be sensitive to a wide range of new physics at the high proton-proton center of mass energy $\sqrt{s}$ =14 TeV [1]. First beam is expected in May 2008 and commissioning in July 2008 [2].

At the LHC design luminosity of 10^{34} cm^{-2} s^{-1}, a beam crossing every 25 ns contains on average 17.3 events. These 10^9 interactions per second must be reduced by a factor of 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. This will be done in two steps. The level-1 trigger first reduces the rate to 75 kHz, and then a High Level Trigger (HLT), using an on-line computer farm, handles the remaining rate reduction.

The CMS level-1 electron/photon, τ-lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [3]. The RCT plays an integral role in the reduction of the proton-proton interaction rate (10^9 Hz) to the High Level Trigger input rate (10^5 Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and $PbWO_4$ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$. An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions 0.087x0.087 ($\Delta\phi x \Delta\eta$), which corresponds 1:1 to the physical tower size of the HCAL.

II. RCT HARDWARE

A. PRIMARY RCT CARDS

The 18 crates of the RCT electronics process data for the barrel, endcap, and forward calorimeters. There is another crate for clock distribution. These are housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code are sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards located on each of 7 Receiver Cards and the single Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the one mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts the 1.2 Gbaud serial data to 120 MHz TTL parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional E_T sums and the electron candidates to the Global Calorimeter Trigger (GCT). The GCT implements the jet algorithms and forwards the 12 jets to the Global Trigger (GT).

The Receiver Card (shown in Figure 1), in addition to receiving and aligning calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Lookup tables are used to translate the incoming E_T values onto several scales and set bits for electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

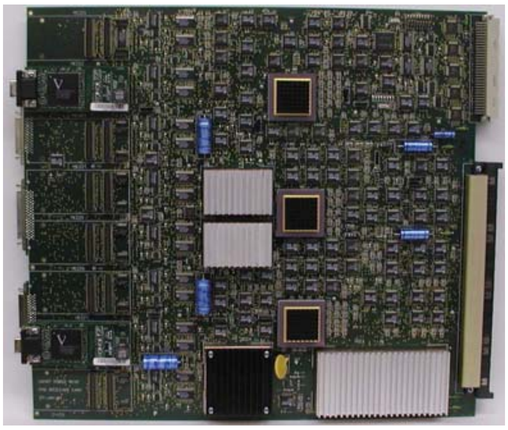


Figure 1: Front of a Receiver Card showing two Receiver Mezzanine Cards in place and Adder ASICs.

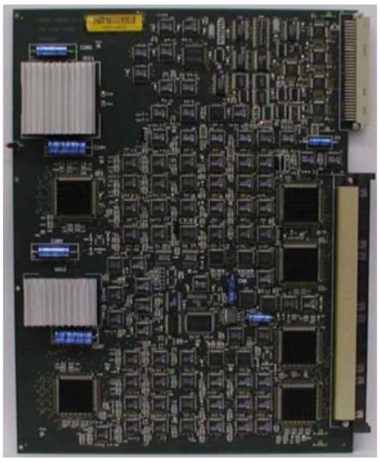


Figure 2: Electron Identification Card showing 4 Sort ASICs (right) and 2 EISO ASICs (left).

The Electron Isolation Card (shown in Figure 2) receives data for 32 central towers and 28 neighboring trigger towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in Sort ASICs on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S Card also receives E_T sums via the backplane, and forwards them and two types of muon identification bits (minimum ionizing and quiet bits – described later) to the GCT. A block diagram of this dataflow is shown in Fig. 3.

To implement the algorithms described above, five high-speed custom Vitesse ASICs were designed and manufactured, a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [4]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216 and check for data transmission errors. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC handles board level boundary scan functions and drivers for data sharing. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/γ candidates. All these ASICs have been successfully tested on the boards described, and procured on in the full quantities needed for the system, including spares. The boards described have been produced using these ASICs and sufficient quantity has been obtained to fill 18 crates and create a stock of spares.

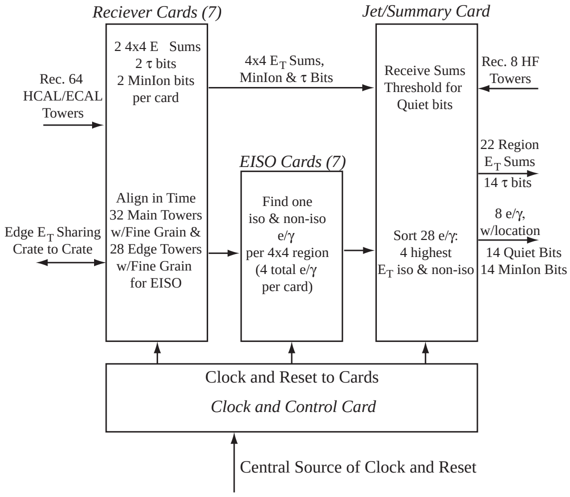


Figure 3: Dataflow diagram for an RCT crate, showing data received and transferred between cards on the 160 MHz differential ECL backplane. Brief explanations of the card functionality are shown. For more details see the text or ref. [3].

Figure 4: The Master Clock Crate and cards. Central is the CIC, receiving the fibre from the TTC system, and moving outwards, 2 CFCm cards, and 7 CFCc cards.

A Master Clock Crate (MCC) and cards are centrally located in the 10 RCT racks to provide clock and control signal distribution (Figure 4). Input to the system is provided by the CMS Trigger Timing and Control (TTC) system [5]. This provides the LHC clock, Bunch Crossing Zero (BC0), and other CMS control signals via a optical fibre from a TTCci (TTC input card) which can internally generate or receive these signals from either a Local

Trigger and Control board (LTC) or the CMS Global Trigger.

The MCC includes a Clock Input Card (CIC) with a LHC TTCrm mezzanine board [5] to receive the TTC clocks and signals via the fibre and set the global alignment of the signals. The CIC feeds fan-out cards, a Clock Fan-out Card Midlevel (CFCm) and a Clock Fan-out Card to Crates (CFCc) to align and distribute the signals to the individual crates via low-skew cable. Adjustable delays on these 2 cards allow fine-tuning of the signals to the individual crates.

B. *RCT Jet Capture Card*

For validation and production testing, a special test board was developed to verify the output of the RCT. The Jet Capture Card (JCC) was developed to capture the output of the JSC in a variety of modes and if needed, generate an external trigger. It sits in the spare VME slot of an RCT crate, receives clocks and control signals from the CCC on two low-skew cables and data on six 68-pin cables from the JSC. Using the ability of the RCT to repeatedly cycle through its LUTs, it was possible to validate the data paths of a full RCT crate with changing patterns for an extended period of time. The capture feature is used in integration tests described later in and the trigger feature was exploited in the CMS Magnet Test and Cosmic Challenge (see below) [6].

III. INPUT AND OUTPUT OF THE RCT

A. *Trigger Primitive Generators - Input*

The HCAL Trigger Readout (HTR) Boards and the ECAL Trigger Concentrator Cards (TCCs) provide the input to the RCT using a Serial Link Board (SLB), a mezzanine board with the V2716-1 mounted on it. The SLB is configurable, with two Altera Cyclone® FPGAs for data synchronization at the V2716-1, Hamming code calculation, FIFOs, and histogramming. The clocking for the SLB is separate from the HTR and TCC primary clocking to ensure alignment at the RCT. The HTR can have up to 6 SLBs and receives data from the front end on fibres into its front panel. The TCC has up to 9 SLBs and also receives front-end data via a fibre to its front panel.

B. *GCT Source Cards – Output*

Each RCT crate is connected to GCT Source Cards, which convert the parallel ECL output of the RCT to optical, so that it may be sent easily to the lower floor of USC55. They are located in the RCT racks, directly above the RCT crates.

IV. COMMISSIONING

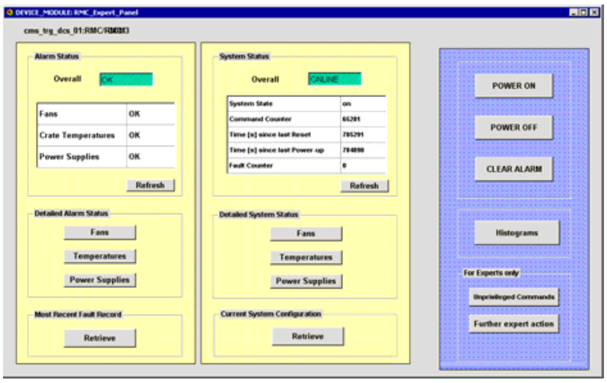
A. *Commissioning the RCT at CMS*

Installation of the RCT is nearly complete. The RCT has 10 racks that hold a total of 21 RCT crates, 6 GCT Crates, and a crate for clock distribution to the SLBs (See Figure 5). The MCC and eighteen of the 20 standard RCT crates are part of the final system. The remaining 2 RCT crates will be used for local testing and storage.

Figure 5: The front of the RCT Racks. Additional, temporary cables seen are for testing.

1) *Rack Infrastructure Installation*

In late July 2006, as soon as the underground counting room (USC55) was deemed "ready for crates" a team from Wisconsin arrived to install the rack infrastructure and empty crates. This included the installation of a custom rack monitoring system. This system, at the heart of which is a Rack Monitor Card (RMC), monitors the status of the power supplies, fans and crate temperatures. A serial port on the card is attached to a serial-to-ethernet connection and PVSS [7], an object-oriented process visualization and control system, is used for the software interface to the RMC. A sample control panel for one of the racks is shown in Figure 6. PVSS enables remote control and monitoring of the system. System variables, such as current and temperature are histogrammed and stored in a database for later access.



DEVICE_MODULE: RMC_Expert_Panel

Alarm Status

Overall: OK

Fans	OK
Crate Temperatures	OK
Power Supplies	OK

System Status

Overall: ONLINE

System State	on
Command Counter	65201
Time [s] since last Reset	785291
Time [s] since last Power-up	784890
Fault Counter	0

Figure 6: PVSS control panel for one RCT rack. From right to left are Alarm Status, System Status, and control and histograms.

2) *Card and Cable installation*

Before the end of August 2007 all the RCT cards were installed in crates in USC55. Cards were shipped as pre-tested sets (16 individual cards to a crate) and the cards were validated one more time at the CMS electronics integration facility using 2 JCCs and crate self-test software that including cable sharing.

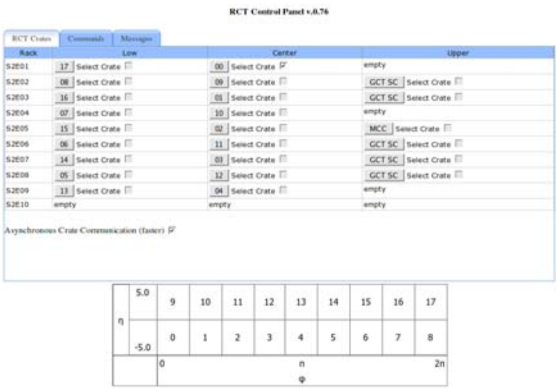
In addition, the cables from the HCAL HTR and HTR TCC SLBs have been installed and the links validated. The JSC to GCT cables have been installed as well, though only about 30% of the GCT Source Cards are in place.

3) *Intercrate Testing*

In order to test the system, the RCT can cycle the addresses of its input LUTs on the Receiver Cards, emulating data from the links. The first intercrate tests were done using the RCT Jet Capture Card receiving the RCT output on just two RCT crates. Now up to 6 RCT crates with all data sharing cables (unconnected edges are quiet) are tested. The software steps through the crates, programming the LUTs and configuring. Then the output is predicted and compared to data captured at the JCCs, reporting any errors. This test is limited to the 6 JCCs available. In order to expand the intercrate testing to all 18 crates, the GCT Source Cards will be used in the final system to capture the data.

4) *Trigger Supervisor*

The Trigger Supervisor (TS) is an online framework to configure, test, operate, and monitor the trigger components and to manage communications between trigger systems [8]. Individual cells are set up for each system, with a central cell interacting with multiple systems at one time using SOAP [9] commands. This enables central configuration of the system for day-to-day running and interconnection tests. The RCT TS handles the crate configuration either using a key from the central cell, or via a user interface (Figure 7). It will also monitor the system and store and retrieve information from a central database. Currently, an eighteen crate TS without monitoring is in use



Rack	Low	Center	Upper
S2E01	17 Select Crate ☐	00 Select Crate ☑	empty
S2E02	08 Select Crate ☐	09 Select Crate ☐	GCT SC Select Crate ☐
S2E03	16 Select Crate ☐	01 Select Crate ☐	GCT SC Select Crate ☐
S2E04	07 Select Crate ☐	10 Select Crate ☐	empty
S2E05	15 Select Crate ☐	02 Select Crate ☐	MCC Select Crate ☐
S2E06	06 Select Crate ☐	11 Select Crate ☐	GCT SC Select Crate ☐
S2E07	14 Select Crate ☐	03 Select Crate ☐	GCT SC Select Crate ☐
S2E08	05 Select Crate ☐	12 Select Crate ☐	GCT SC Select Crate ☐
S2E09	13 Select Crate ☐	04 Select Crate ☐	empty
S2E10	empty	empty	empty

Asynchronous Crate Communication (faster) ☑

η	5.0	9	10	11	12	13	14	15	16	17
	-5.0	0	1	2	3	4	5	6	7	8
		0				π				2π
						φ				

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Figure 7: RCT Trigger Supervisor window for programming individual crate crates and cards. Individual tests can be chosen.

5) *Trigger Emulator*

The trigger emulator is a software package designed to reproduce the hardware response of the trigger exactly. It includes the Look Up Tables (LUTs), hardware and firmware registers, and all other configuration options. It is used for hardware validation and monitoring, and is currently in use during calorimeter trigger integration.

The trigger emulator takes the files used by the HCAL and ECAL as input to their TPG pattern generators and files of data captured by the RCT, GCT, and GT as output, and make direct comparisons. In this way errors are tracked down in the software, hardware, and firmware. In reverse, the validation of the algorithms can be done by injecting physics patterns into the hardware pattern generators and verifying the output.

V. INTEGRATION

A. *The Magnet Test and Cosmic Challenge*

In summer and autumn 2006, the CMS barrel rings and endcap disks, along with parts of the muon system, ECAL, HCAL, and tracker were used to understand the effects of the magnetic field and perform a “slice test” of the CMS DAQ system. The Magnet Test and Cosmic Challenge (MTCC) included the trigger systems. Since the full calorimeter trigger chain was not yet available in the second phase (autumn), the RCT exploited the Jet Capture Card’s capability of sending a trigger signal out. For two portions of the HCAL barrel (upper and lower) a separate trigger signal was generated. A coincidence was needed, so the JCC’s signals went to NIM hardware outside of the crate and the final AND was sent to the LTC, which can also receive and distribute triggers. It used the AND as part of its readout and L1A generation. After timing in, events using the HCAL/RCT as a trigger at 4T magnetic field were seen. A display of an MTCC event captured by the HCAL/RCT trigger is seen in Fig. 8.

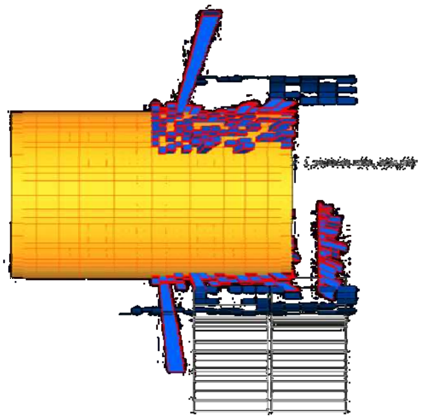

Figure 8: An event captured by the HCAL/RCT trigger. The gold barrel represents the HCAL. The drift tube hits can also be seen in the lower part of the picture.

B. *Integration Tests in USC55*

Additional integration tests took place well before USC55 was ready. These tests, some of which took place at the electronics integration facility, have been described in reference [10].

1) *ECAL and HCAL TPGs to RCT JCC*

The HCAL and ECAL TPGs successfully sent patterns to the RCT in the electronics integration facility using a common clocking system [10]. In USC55, a similar system was put in place, using a Local Timing and Control (LTC) board with 3 Trigger Timing and Control interface (TTCci) boards [5] to send clocks and global control signals to all three systems, HCAL, ECAL, and the RCT. when the systems' hardware was in place, these tests were moved underground.

The RCT's LUTs were programmed to copy the data coming from the TPGs to the RCT regional sums path. The HCAL sent a pattern of all Trigger Primitives (TPs) filled with the same value, which incremented every five crossings. This was captured successfully as regional sums with the JCC, and aligned with BC0. The ECAL sent a single crossing of identical data on all of its channels and the data was seen and aligned to BC0 at the JCC as 4x4 regional sums. Next, the ECAL sent a single tower per bunch crossing. The LUTs were reprogrammed and the data sent on the e/γ path. This was captured at the JCC as isolated electrons, as expected.

2) *ECAL/HCAL TPGs and RCT to GCT*

After the GCT had installed the electron Source Cards (SCs) tests were made capturing with the SCs and without the RCT JCC. The HCAL and ECAL TPGs sent either constant data on one bunch crossing or an increment pattern. The RCT was programmed with an identity LUT to send the pattern to the GCT on the e/γ path. The GCT captured and verified that the data was correct.

Later, with the ECAL TCC only, the single-tower increment data was forwarded to the GCT Concentrator Card (just before the Global Trigger) and captured. This was checked with the L1 Trigger Emulator predictions. Errors in software and firmware were found and corrected. The tests were repeated to ensure that the fixes were correct.

3) *ECAL/HCAL TPGs, RCT, GCT to Global Trigger*

After the above tests, the Global Trigger (GT) was included in integration. Instead of using the LTC for sending control signals to the sub-systems, the GT took over this responsibility to capture data from the GCT.

At first the simple one-tower increment pattern was sent from the ECAL TCC through the RCT e/γ path, GCT, and captured at the GT. Captured data was compared to that predicted by the L1 Trigger Emulator. All data matched, except for a phi index mismatch that was understood and is being corrected.

After this, more complex patterns representing simulated 35 GeV electrons across multiple trigger towers in a 4x4 trigger tower region were sent, captured, and compared to the emulator. An additional exercise, sending the same pattern to another RCT crate checked synchronization. In both cases, data agreed with the emulator, except for the phi index.

4) *Future Tests*

With over 1000 SLB cables nearly installed, the SLB to RCT cabling map needs to be checked. For this, the TPGs will send TP values to specific towers and SLBs on specific crossings and the RCT will verify the map at the JCC. This test will provide the groundwork for an eventual automated check using the GCT Source Cards to verify cabling after any work done on the systems.

Since May 2007 Monthly Global Runs of about 3 days have been used to test "slices" of the detector and data acquisition. In the near future The RCT will participate with either or both the ECAL and HCAL TPGs and forward the information to the GCT on the e/γ and regional sum paths. The e/γ and jet triggers can then be used to time in, and validate the readout.

Tests will continue on until the LHC turn on in 2008. Tests planned for the future include using increasingly complex patterns, more RCT crates, and RCT internal data sharing on cables to verify timing and synchronization. To verify alignment between subsystems, HCAL and ECAL patterns will be sent at the same time. The emulator will be used to verify the results. The GCT Regional Sum Source cards and Jet path is expected to come on line in November 2007 and integration and verification of the algorithms is planned as well. In December 2007, the RCT will take part in a longer term CMS Cosmic Run with half of the detector and a 0T magnetic field.

VI. CONCLUSIONS

The integration and testing of the Regional Calorimeter trigger has expanded our understanding of the hardware and the subsystems that we connect to, the HCAL HTR, the ECAL TCC, the GCT, and the GT. It has led to improvements in the hardware and the firmware of the subsystems. As integration continues during installation underground, lessons learned will help provide a robust RCT for the turn-on of the LHC in 2008.

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