Thermal pedestal fluctuation in a room with air condition. Re-mating optical connectors can also change the analog signal amplitude.

Automatic pedestal correction to a value of $12$.

Narrowing of the event number coding due to the automatic pedestal correction, preventing misinterpretation.

The final data block consists of:

- Start: 3 UB (Ultra-black), BL (black)
- Header (event number)
- 4 CLK periods
- DAC or Temperature
- UB, BL, data
- Pixel data: 5 CLK periods, pulse height
- Trail: 2 UB, 2 BL, 4 trail bits

This scheme shows the various data, clock and control buses. The data flows from inputs via ADCs, data processors into FIFO1. Four or five channels are collected in FIFO2. All event data is eventually transferred into FIFO3.

Two slow data buses (32 bits wide) transport VME data from and to the Altera FPGA. All data and control lines are clock-synchronous, and the latter are equipped with digital filters for noise rejection. One of the buses has a length of 80cm and a transition from D to 1 (or inverse) on many or all bits creates a noise peak on the whole board. Hence VME commands should be avoided during data taking. Without clock, only the reset signal works. Analog, controls and clocks are all differential signals. Clock, trigger, fast reset and bunch counter signals are provided by the TGC system (ICPRA). Alternatively, standalone operation is possible by using a custom P0 bus.

The Pixel FED consists of a mother board, five ADC daughter boards and five Altera daughter boards. These boards are in sync with each other using a modular approach.

Advantages:

- Reduction of mother board complexity (110 instead of 14 layers with 1.8mm thickness)
- Micro-vias (200um) are required with the Altera 85A, and can be realized with thinner daughter boards
- Testing, repairing, and spare keeping is easier

Disadvantages:

- More space needed (not an issue here)
- Electric signal degradation (addressed with using serially terminated point-to-point connections only)
- Connector relability

Detailed description of data flow:

The incoming pixel data is processed after digitization, resulting in a 40 bit wide data block with channel header and trailer, which is stored in the FIFO1. The TGC event number, latched by the L0 trigger, is stored in a special event number FIFO. As long as that FIFO is not empty, we also expect pixel data in the FIFO2 and hence a trigger to FIFO2 is indicated, which collects data from 4 or 5 FIFO1s. Several checks are performed during the transfer, such as a comparison between the TBM event number and the TGC event number. Errors are stored with detailed information and copied to the data. Repeatedly occurring critical errors are sent to the TTS system.

Other errors include a missing channel or error bits in the ROC trailer. Moreover, the number of bits in each ROC double is histogrammed and can be read by VME in order to detect potential problems. Another FIFO stores digitized DAC or temperature values sent by the ROCs.

Finally, the data from eight FIFOs are transferred to the final data processor over two busses of 64-4 bits each. Proceeded by a special header as expected by the DAQ, the data is stored in FIFO3. After a data block is read out via the S-Link, a DAC trailer is finally added.

Spy memories are included in various locations on the Pixel FED to allow data checking, testing and maintenance. Such spy memories also capture the final data transferred via the S-Link.