The CMS Pixel FED

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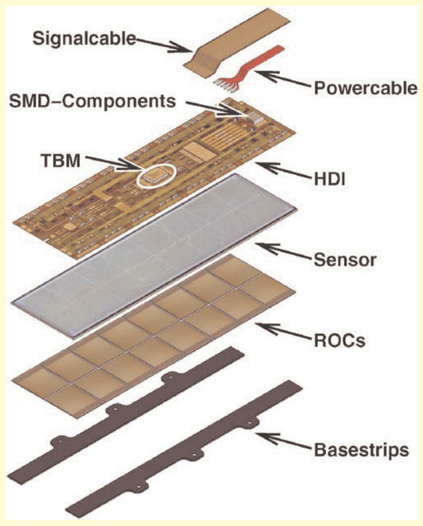
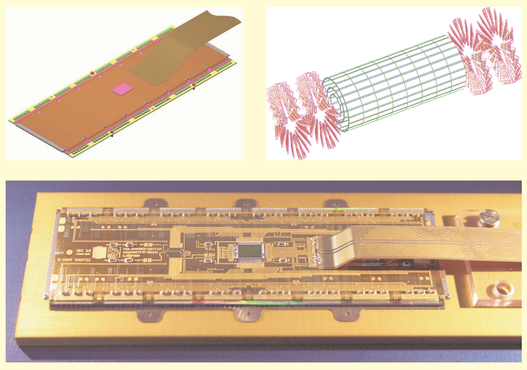
ABSTRACT

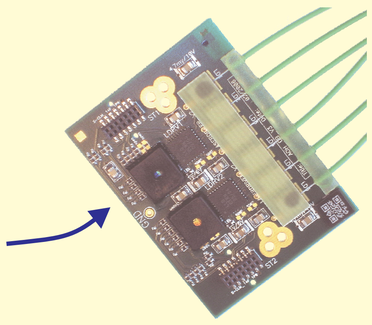
The innermost detector of the CMS Experiment consists of 60 million silicon pixels. The hit data has to be read out and must be digitized, synchronized, formatted and transferred over the S-Link to the final CMS DAQ. The amount of data can only be handled because the readout chip (ROC) delivers zero-suppressed data above an adjustable threshold for every pixel.
The Pixel FED 9U VME module receives an optical analogue signal, which is subsequently digitized and processed. The position of the pixel on a module is transmitted with 5 symbols coded in 6 pulse height steps each. The data of 36 inputs from one event build a final event data block. The main challenge is that the information which arrives on the different inputs at the same time can be from different events and can differ up to 16 events depending on the number of hit pixels in past. That is possible because the ROC has a multi event memory and the input data length can be very different. Finally the information will be transferred over the S-Link to the CMS DAQ. Each module must be able to process more than 100 kHz trigger rate or if in trouble to send an alarm signal. The number of inputs is limited by the maximum data transmission rate of the S-Link (640 MB/s) for the expected high luminosity of LHC.
The data flow on the module is continuously controlled. Errors are written in an error memory, included in the data stream and if critical sent to the general CMS readout control.

READOUT CHAIN

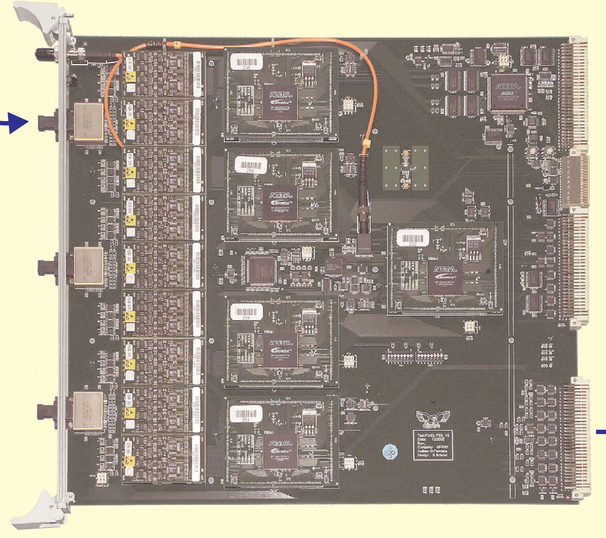




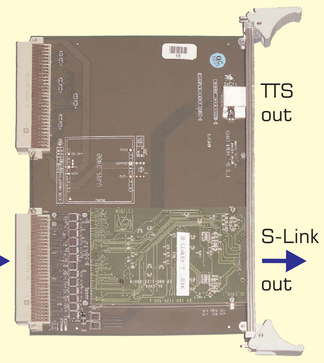
A barrel sensor is read out by 16 Read Out Chips (ROCs), a forward sensor needs 24 ROCs. Each ROC can store up to 16 events. The pixel data are transmitted to the Optohybrids over controlled impedance differential lines.



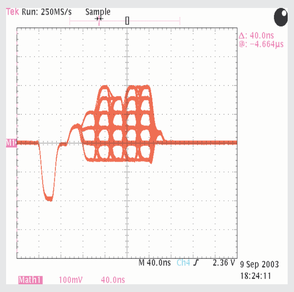
The pixel hit data are converted to optical signals using Analog Optohybrids which are composed of six laser diodes. The hybrids are cooled by electrically isolated cooling tubes.



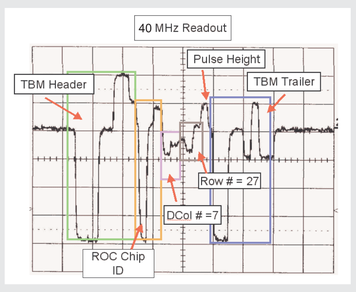
32 of these 9U Pixel FED modules serve the barrel pixel, 8 more are used in the forward section. A 6U S-Link is attached to the rear of each Pixel FED.



PIXEL DATA



Overlay plot showing position coding as well as the signal pulse height of a single ROC.



Data from one ROC, plus header and trailer genrated by the Token Bit Manager (TBM), at the input of the Pixel FED.

The final data block consists of:

Start	3 UB (Ultra-black), BL (black)
Header (event number)	4 CLK periods
DAC or Temperature	UB, BL, data
Pixel data	5 CLK periods, pulse height
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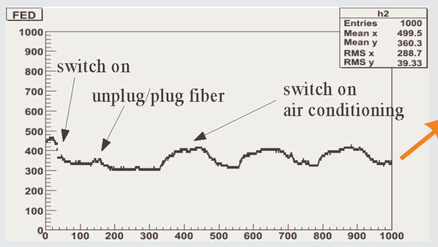
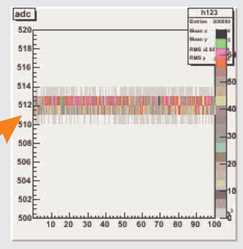
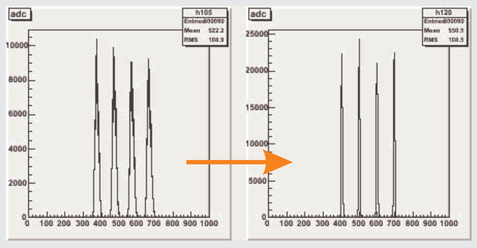
Trailer	2 UB, 2 BL, 4 trailer bits



Thermal pedestal fluctuation in a room with air condition. Re-mating optical connectors can also change the analog signal amplitude.

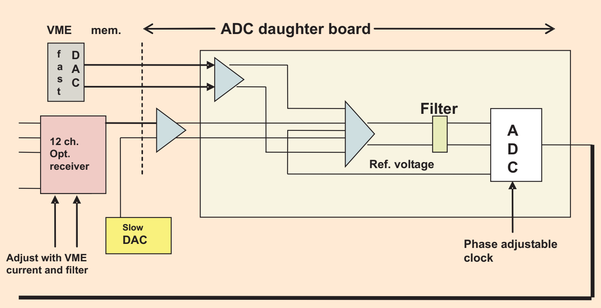


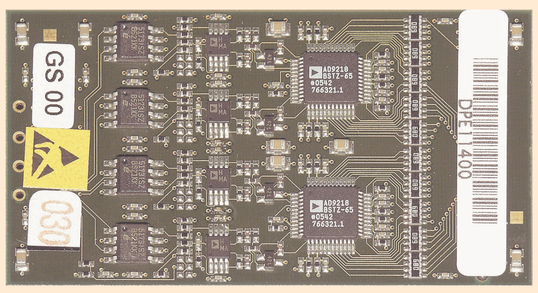
Automatic pedestal correction to a value of 512.

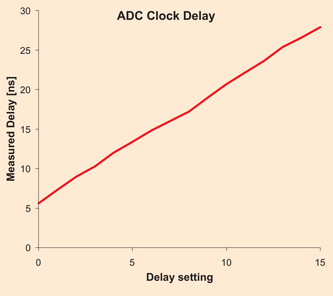


Narrowing of the event number coding due to the automatic pedestal correction, preventing mis-interpretation.

ANALOG-DIGITAL CONVERSION



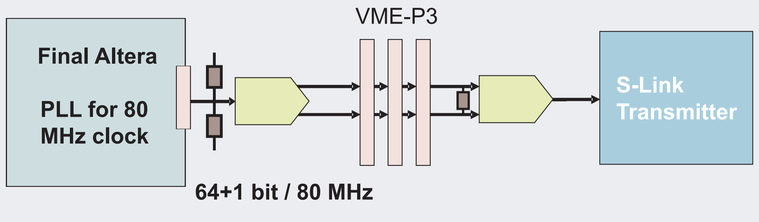




Each ADC daughter board contains four channels. The input is the sum of the optical receiver output, a slow DAC signal to adjust the offset and a fast DAC signal which can be used for test purposes (e.g. ROC emulation).

Each ADC has an adjustable clock phase. 16 different clock delays are created from Altera-internal PLLs. Selection of the optimum sampling point is essential for non-ideal signals (limited bandwidth and slew rate).

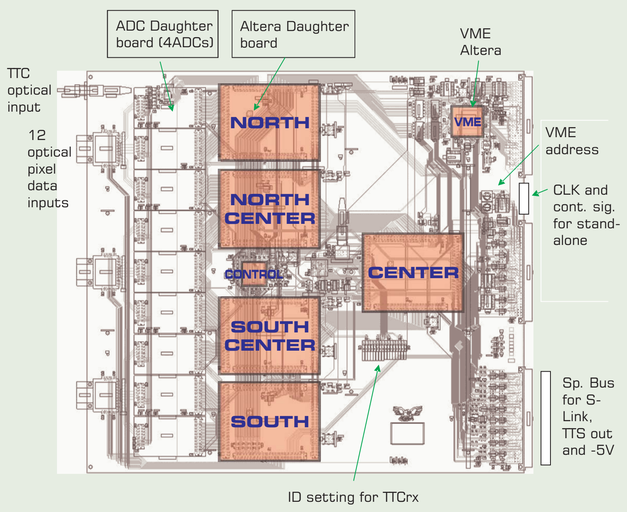
S-LINK OUTPUT



The data transfer was successfully tested with 300kHz trigger rate and short events, using the BUSY signal to throttle the trigger when the S-Link was at the limit and FIFOs nearly full. At full luminosity, about 100 events of average size can be stored on board.

The S-Link mezzanine board, which was developed at CERN, sits on a 6U VME board located in the rear part of the VME crate to allow easy extraction of the Pixel FED. The electrical signal has to pass several connectors in order to reach the S-Link mezzanine board.
A well defined data block is expected by the S-Link. The data is 64+1 bits wide and transferred at 80MHz. The clock phase, latching the data into the S-Link, can be adjusted in the Final Altera. It was found that safe transmission is achieved throughout a range of at least 8ns for that clock phase delay.

PIXEL-FED INTERNALS



This scheme shows the various data, clock and control buses. The data flows from inputs via ADCs, data processors into FIFO1. Four or five channels are collected in FIFO2. All event data is eventually transferred into FIFO3.
Two slow data buses (32 bits wide) transmit VME data from and to the Altera FPGAs. All data and control lines are clock-synchronous, and the latter are equipped with digital filters for noise rejection. One of the buses has a length of 60cm and a transition from 0 to 1 (or inverse) on many or all bits creates a noise peak on the whole board, hence VME commands should be avoided during data taking.
Without clock, only the reset signal works. Analog, controls and clocks are all differential signals. Clock, trigger, fast reset and bunch counter signals are provided by the TTC system (CERN). Alternatively, standalone operation is possible by using a custom PO bus.

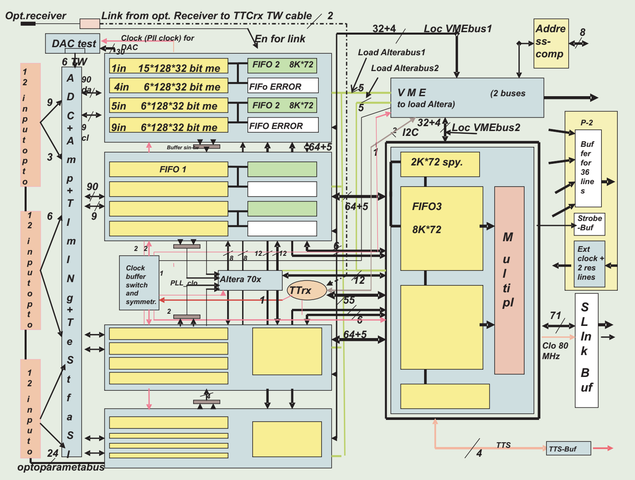
The Pixel FED consists of a mother board, nine ADC daughter boards and five Altera daughter boards.
There are pros and cons with such a modular approach.

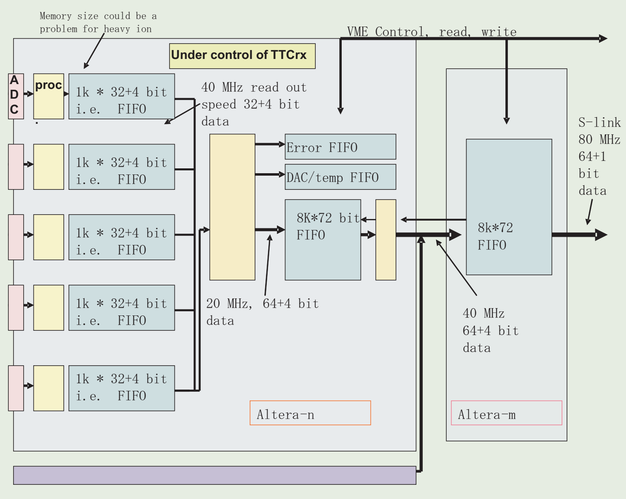
Advantages:

- Reduction of mother board complexity (10 instead of 14 layers with 1.8mm thickness)
- Micro-vias (200μm) are required with the Altera BGAs and can be realized with thinner daughter boards
- Testing, repairing, and spare keeping are easier

Disadvantages:

- More space needed (not an issue here)
- Electric signal degradation (addressed with using serially terminated point-to-point connections only)
- Connector reliability





Detailled description of data flow:
The incoming pixel data is processed after digitization, resulting in a 40 bit wide data block with channel header and trailer, which is stored in the FIFO1.
The TTC event number, latched by the LO trigger, is stored in a special event number FIFO. As long as that FIFO is not empty, we also expect pixel data in the FIFO1 and hence, a transfer to FIFO2 is initiated, which collects data from 4 or 5 FIFO1s. Several checks are performed during the transfer, such as a comparison between the TBM event number and the TTC event number. Errors are stored with detailled information and copied to the data block. Repeatedly occuring critical errors are sent to the TTS system.

Other errors include a missing channel or error bits in the ROC trailer.
Moreover, the number of hits in each ROC double-column is histogrammed and can be read by VME in order to detect potential problems. Another FIFO stores digitized DAC or temperature values sent by the ROCs.
Finally, the data from eight FIFO2s are transferred to the final data processor over two busses of 64+4 bits width each. Preceded by a special header as expected by the DAQ, the data is stored in FIFO3. After a data block is read out via the S-Link, a DAQ trailer is finally added.
Spy memories are included in various locations on the Pixel FED to allow data checking, testing and maintenance. Such a spy memory also captures the final data as transferred to the S-Link.

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