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The CMS Pixel FED

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The innermost detector of the CMS Experiment consists of 60 million silicon pixels. The hit data has to be read out and must be digitized, synchronized, formatted and transferred over the S-Link to the final CMS DAQ. The amount of data can only be handled because the readout chip (ROC) delivers zero-suppressed data above an adjustable threshold for every pixel.
The Pixel FED 9U VME module receives an optical analogue signal, which is subsequently digitized and processed. The position of the pixel on a module is transmitted with 5 symbols coded in 6 pulse height steps each. The data of 36 inputs from one event build a final event data block. The main challenge is that the information which arrives on the different inputs at the same time can be from different events and can differ up to 16 events depending on the number of hit pixels in past. That is possible because the ROC has a multi event memory and the input data length can be very different. Finally the information will be transferred over the S-Link to the CMS DAQ. Each module must be able to process more than 100 kHz trigger rate or if in trouble to send an alarm signal. The number of inputs is limited by the maximum data transmission rate of the S-Link (640 MB/s) for the expected high luminosity of LHC.
The data flow on the module is continuously controlled. Errors are written in an error memory, included in the data stream and if critical sent to the general CMS readout control.

Summary

The signal of the pixel detector has to pass several steps before the arrival at the Front End Driver (FED). Initially it is a 40 MHz differential analogue signal. Inside the pixel detector it is transferred over cables and PCB traces to the optohybrid. The main intention was to keep material budget as small as possible, to include a cooling system for the hybrids and to have a minimum of signal reflections. Using a single-mode fiber, the signal is finally transferred to the FED. On the way it passes several connectors where uncontrolled signal attenuation occurs.
The pixel readout system consists of 40 PX-FEDs with 36 inputs each. The optical input signal is converted to electrical on the board. Adjustable current sources in the optical receiver are used to tune the output range. Furthermore a DC-DAC signal for every input allows optimal offset adjustment in the 10 bit range of the ADC. A fast DAC can create arbitrary input pattern for test purposes. We do not expect that the input signals are in phase to the clock, hence every input has its own clock, where the clock phase can be adjusted to the main clock in steps of 1.6 ns to select the optimum digitization sampling point for each input.
The data processing is done on Altera FPGAs, four at the front and one for final data block building as well as multi event storage. Each front Altera handles nine inputs. The first task is to synchronize the ADC data to the main clock and automatically adjust the pedestal of the incoming signals to a pre-defined value. This is absolute necessary, because the optical transmission system is strongly influenced by temperature. Each input has its own data processor. The data arrive at different times and have different length. A Readout Chip (ROC) at the front end can store up to 16 events. An average of 20 hits is expected with high beam intensities. The result is an event data block with primary header and trailer and stored in the first FIFO-1. If the data size is too big, the data stream is truncated and closed with a trailer. If the FIFO-1 is nearly full the data length is drastically reduced. A busy is sent to the general control system and an error message stored. A possible reason for such a condition could be problems with the pixel data threshold. A trigger signal together with an event number starts a readout process of one event, stored in the 36 FIFO-1.On the way to the next FIFO-2, where the data from 4 or 5 inputs are stored, the data are checked if the input event number correlates with that of the TTC system, once all data from each input has arrived after a certain time. A column histogram shows the distribution of the column numbers. All the errors are stored in a special error memory with some more information like input and event numbers. The error message is also transferred as error data to the event data and if absolutely critical, the error information is also sent over the TTS system to the general control system. With two data buses, each 64+4 bits wide, the event information of the eight FIFO-2 is collected in the final FIFO-3. On this path several spy FIFOs are included. Finally, the data are transferred to the CMS DAQ over the S-Link at 80 MHz.
The Pixel-FED board also includes two 32 bit bus systems controlled by VME. One has a length of approxi-

mately 65 cm and was a critical part because of crosstalk to the input signals and to each other because of the fast rise time of the drivers.
The VME data on board are clock synchronized and all logic blocks need a clock for proper functioning except the reset signal which is asynchronous. The inputs for the two data strobes, address and data and read/write decision have a digital filter for protection against noise and spikes.
No hang-up of the processing und storage system should be possible. The data transfer is as fast as the highest S-Link speed. The module was tested with 300 kHz trigger rate and short events. The BUSY signal was used to reduce the trigger rate when the S-Link was at the limit and the FIFOs nearly full. At full luminosity, about 100 events of average size can be stored on board.
The module is composed of a mother board, nine ADC and five Altera daughter boards. Thus, the number of layers for the main board could be reduced to ten. The general design rule for fast signals was that one output drives one input (point to point connection). Most signal lines are serially terminated, which reduces the drive power significantly considering the wide parallel buses.

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