The GBT, a Proposed Architecture for Multi-Gb/s Data Transmission in High Energy Physics

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Outline

- Motivation
- The proposed link architecture
  - Link topology
  - GBT chipset
  - Link bandwidth
  - GBT to Front-end link topology
- TTC
- Slow control
- Development and testing
- Error correction and line coding
- Summary

Disclaimer:

"This project is still in its specification phase, detailed features are likely to change prior to the final silicon fabrication…"

The objective of this presentation is to communicate the current ideas to stimulate discussion and to obtain feedback from the potential users!

LHC upgrade (SLHC)

- Higher beam luminosity:
  - Improved statistical accuracy of the measurements
  - More complex DAQ/TTC/SC systems (higher bandwidth)
  - Higher radiation doses
- Higher bandwidth links required at (if possible):
  - No penalty on the detector's mass budget
  - No penalty on power consumption
- The viable solution is to:
  - Reduce the number of optical fibre links
  - Increase the bandwidth available per link
- Benefits:
  - Lower mass
  - Possible overall reduction of power consumption
  - Lower installation and maintenance costs

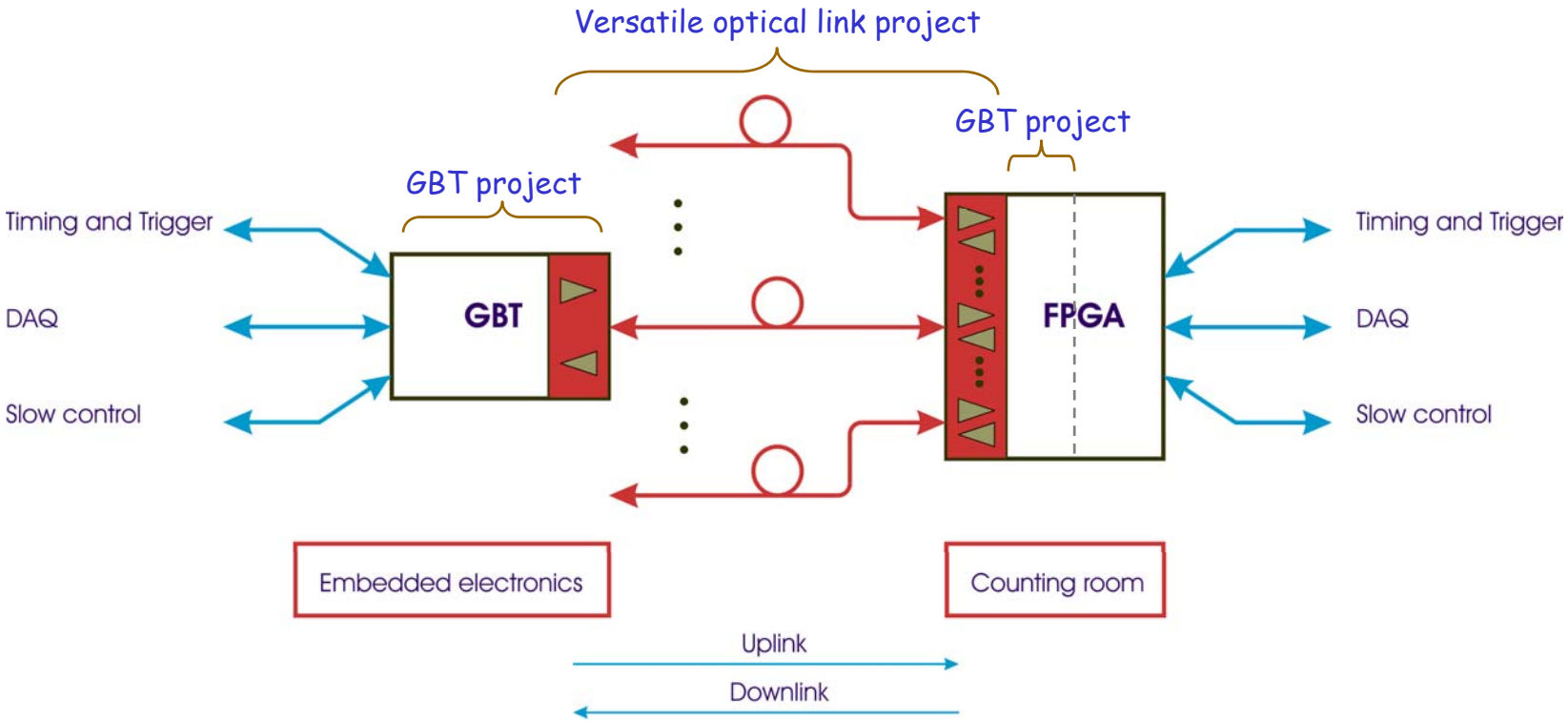
TTC / DAQ / SC links – past

- Running HEP experiments takes 3(+) systems:
  - Data Acquisition (DAQ) systems
  - Timing, Trigger and (fast) Control (TTC) system
  - Slow control (SC) systems
- Data transmission links for these systems have different requirements
- In the past specific data transmission links have been custom developed for each of these applications:
- This was justified by:
  - The type of application being targeted
  - Technological limitations.

TTC / DAQ / SC links – future

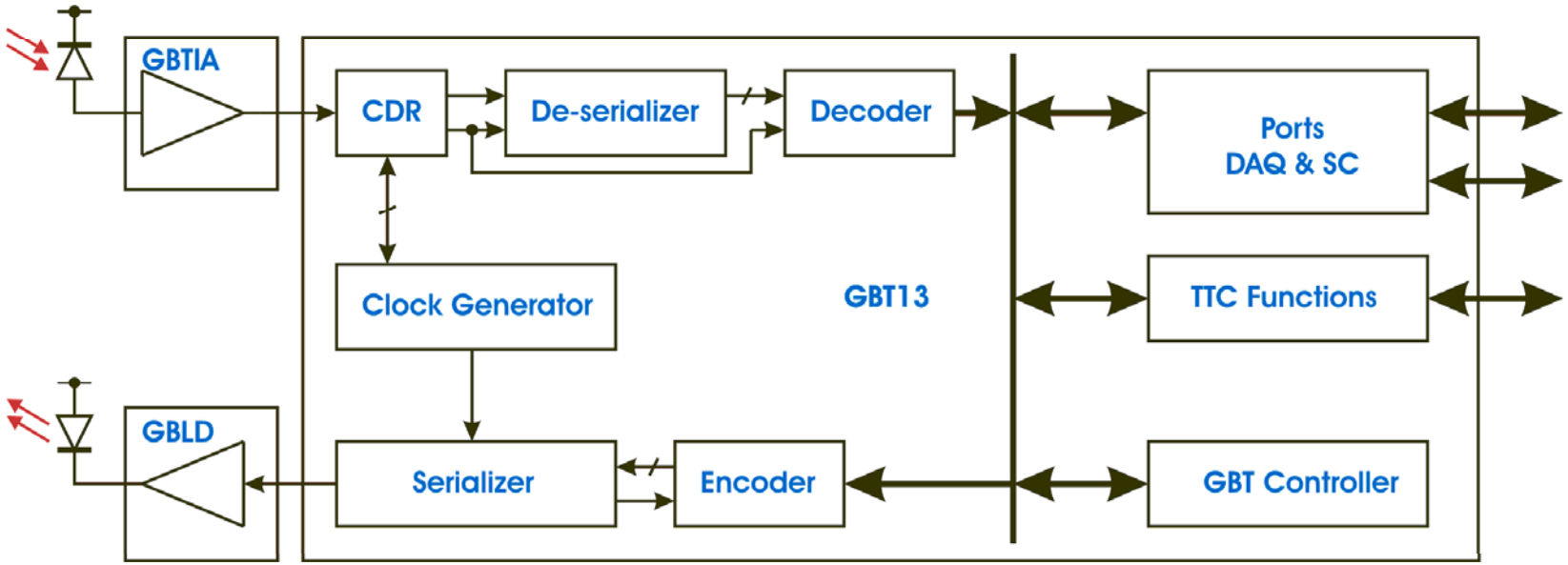
- We propose the development of a general purpose optical-fibre link which can simultaneously serve:
  - DAQ
  - TTC
  - SC
- The maturity of today's Optoelectronics and CMOS technologies enables such a development
- The advantages are multiple:
  - R&D effort concentrated on a single project
  - Single type of components needs to be:
    - Developed
    - Qualified
    - Produced
    - Installed
    - Maintained
  - Reduction of the number of optical fibres installed:
    - The channel bandwidth is increased
    - DAC/TTC/SC data transits over a single fibre.

GBT link architecture



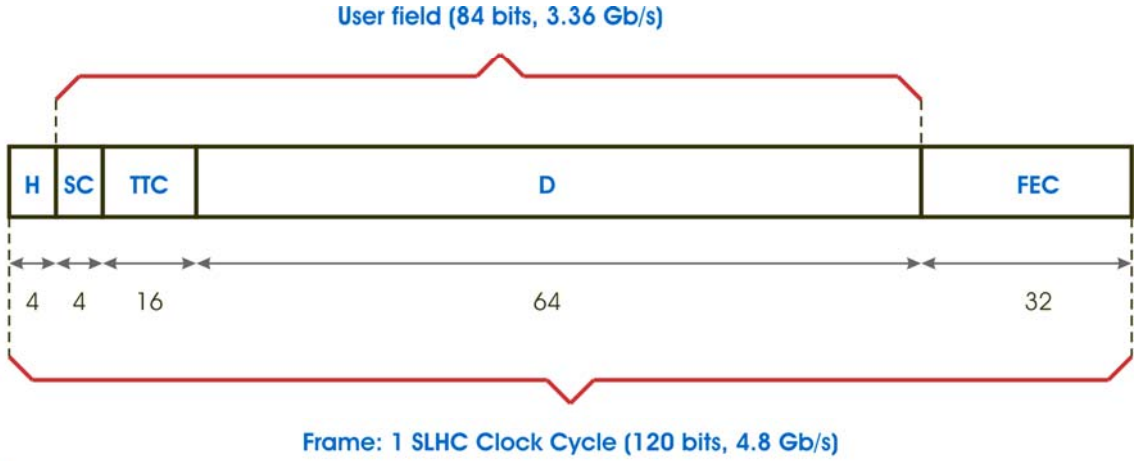
- Bidirectional point-to-point optical fiber links
- The heart of the link is the GigaBit Transceiver (GBT13)
- Each link carries simultaneously: DAQ, TTC and SC data
- Embedded transceiver: the GBT Chipset
- Counting room transceivers: FPGA and COTS optoelectronics components

The GBT chipset



- GigaBit Transimpedance Amplifier (GBTIA)
- GigaBit Laser Driver (GBLD)
- GigaBit Transceiver (GBT13)
  - SERDES
  - Communications controller
  - TTC receiver
- GBT – Slow Control ASIC

Link bandwidth



H - Header

SC - Slow Control (160 Mb/s)

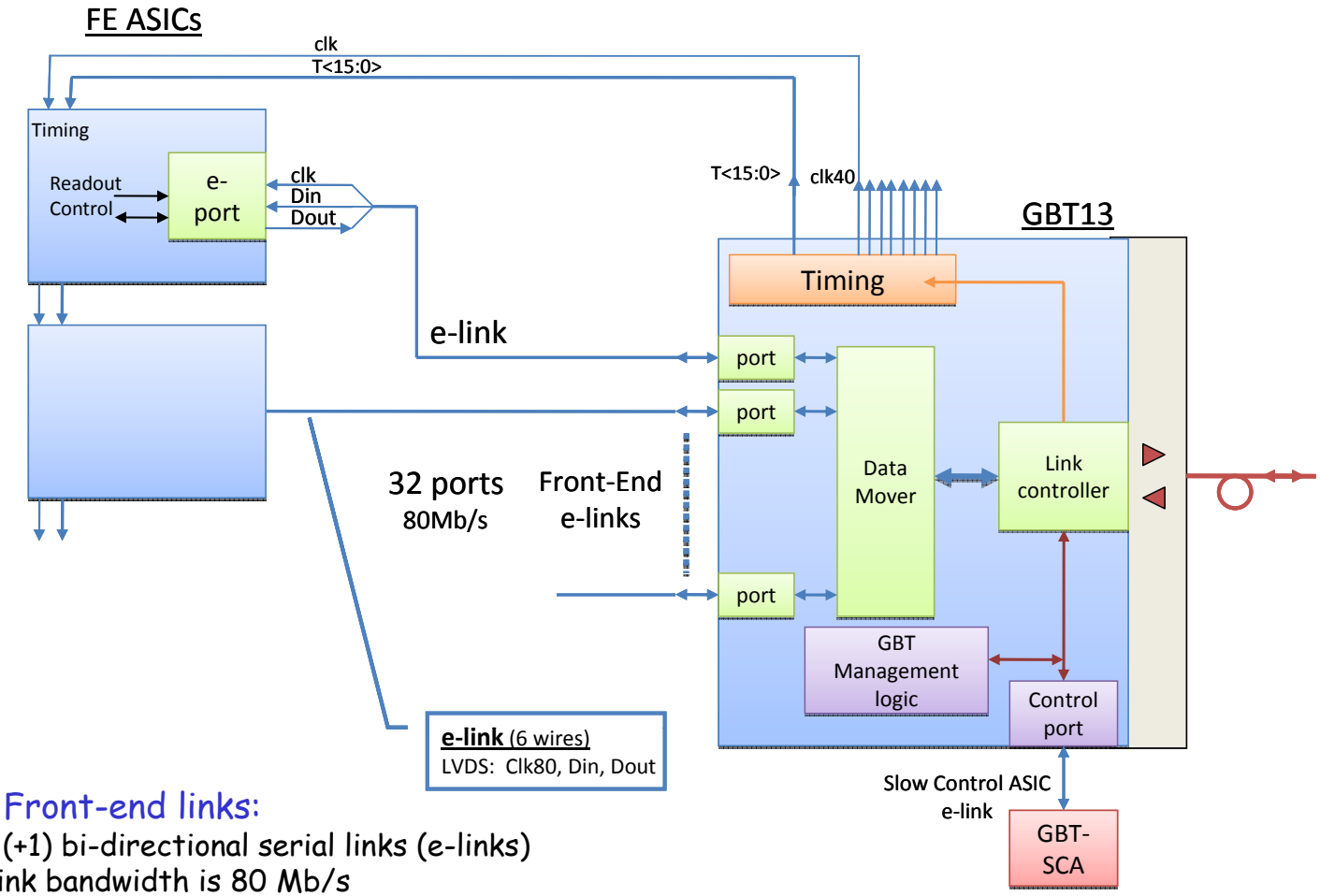
TTC - Timing Trigger and Control (640 Mb/s)

D - Data (2.56 Gb/s)

FEC - Forward Error correction

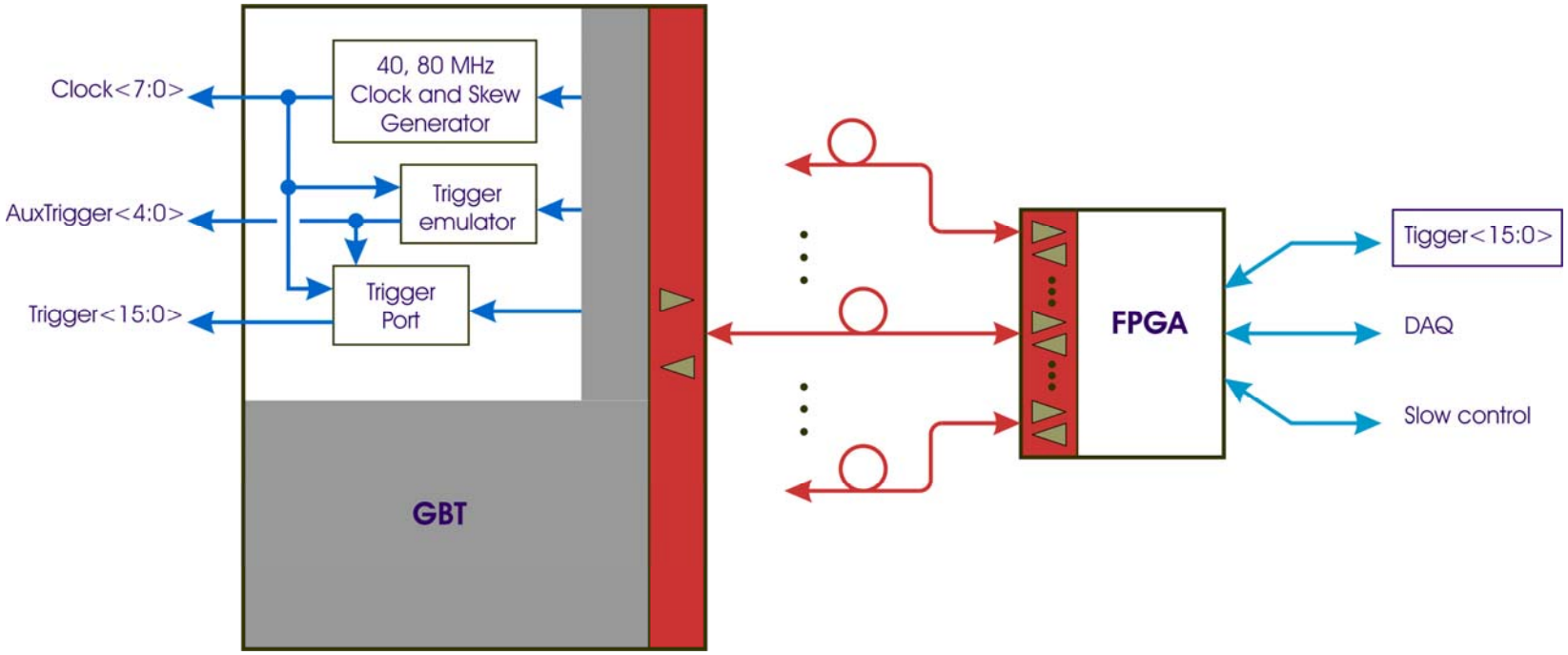
- GBT: 120-bits transmitted during a single bunch crossing interval → 4.8 Gb/s.
- 4 header bits
- 32 forward error correction bits
- User field of 84 bits → 3.36 Gb/s:
  - SC: 4-bits → 160 Mb/s
  - TTC: 16-bits → 640 Mb/s
  - DAQ: 64-bits → 2.56 Gb/s
- Bandwidth is fixed per frame but can be shared by the front-end devices

GBT to front-end link topology



- GBT to Front-end links:
  - 32 (+1) bi-directional serial links (e-links)
  - E-link bandwidth is 80 Mb/s
  - Several e-links can be grouped together to serve a single front-end device achieving bandwidths that are multiples of 80 Mb/s
- 16-bits for TTC
- 8 phase adjustable clocks
- **An E-Link Port Adaptor (EPA) "macro" will be available for integration in the front-end ASICs**

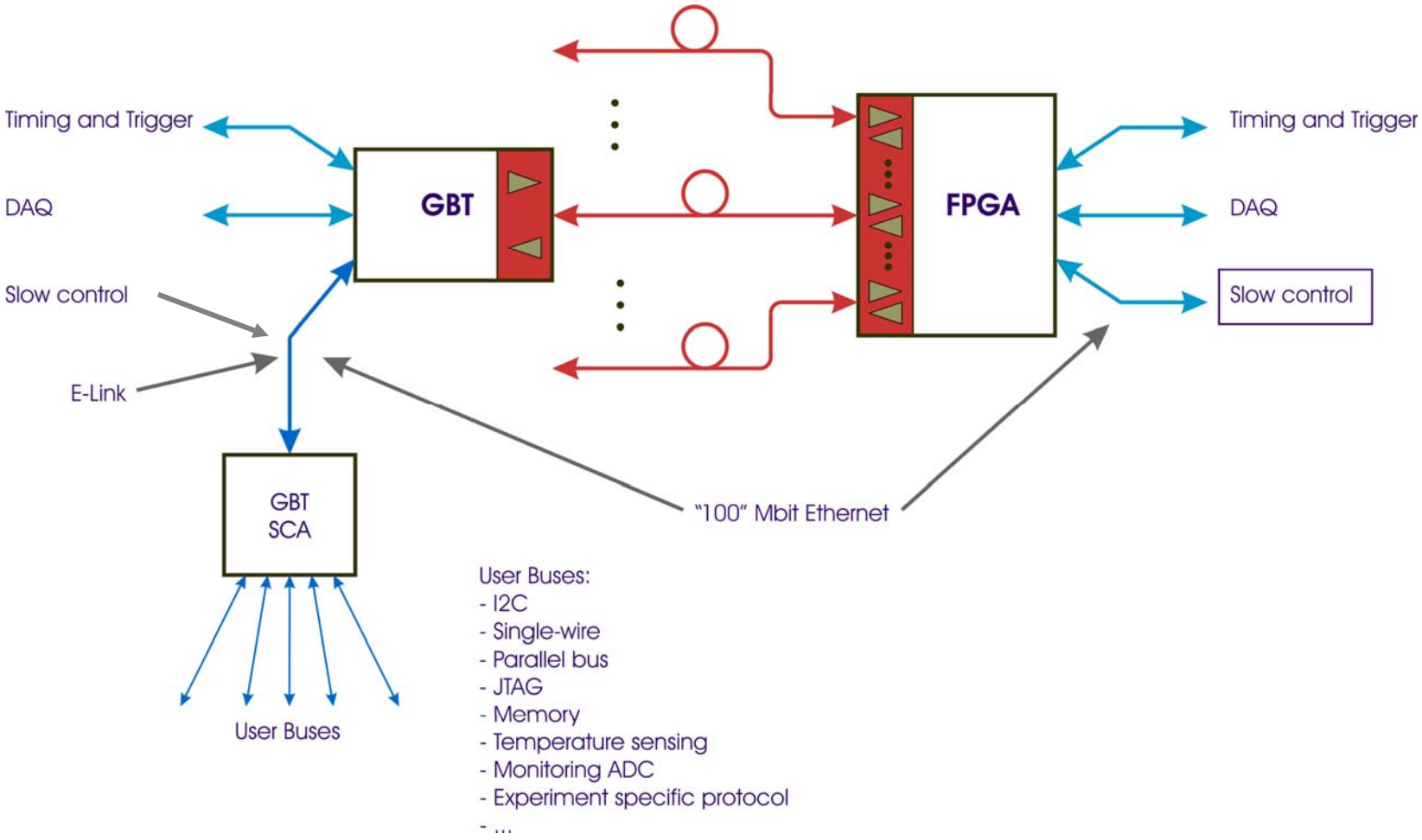
TTC functionality



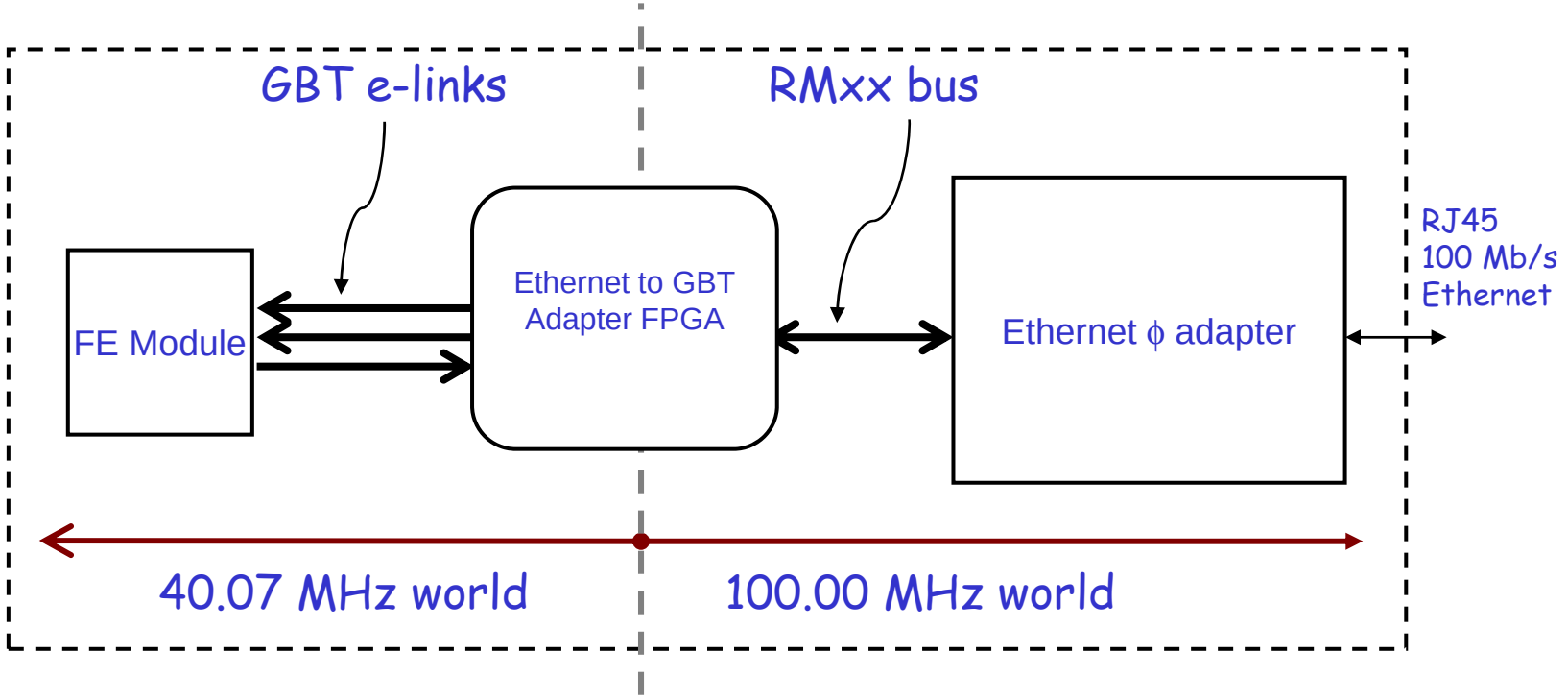
Slow control

- 4-bits are reserved in each frame for slow control
- A pair of E-links is reserved to implement a slow control channel
  - GBT management
  - GBT-SCA
- The available bandwidth is 2 × 80 Mb/s
- The slow control functions will be under the control of a dedicated ASIC:
  - GBT – Slow Control ASIC (GBT – SCA)
  - It interprets the Ethernet frames carried by the SC field of the GBT frame
  - Serves as node controller:
    - Routes commands to the appropriate channels
    - Waits for acknowledgements from the different channels
    - Feeds back to the counting room the requested responses

SC – Two chips solution



Development and testing

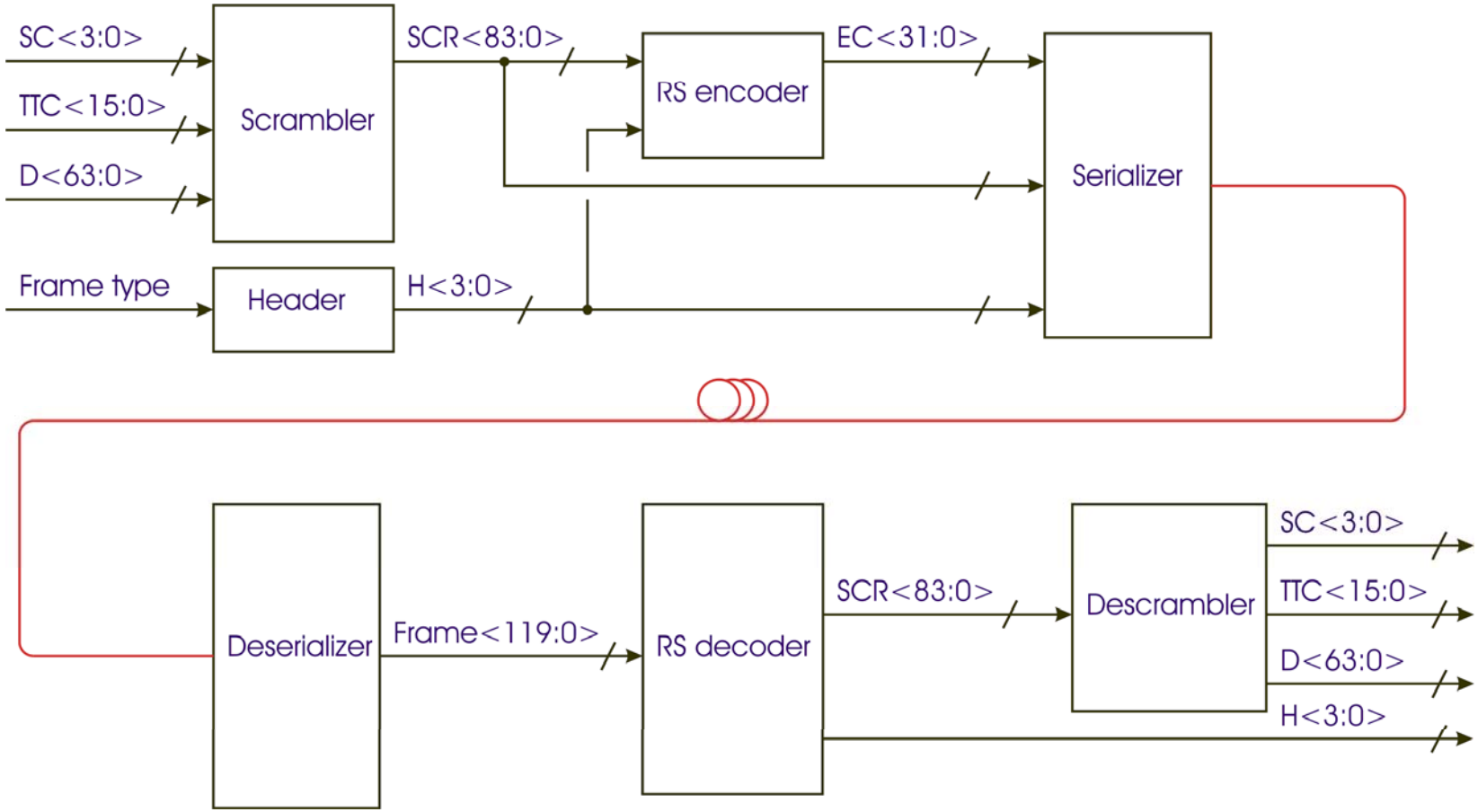


- 100% compatibility with standards desirable
  - For testing and development of GBT based systems
- LHC "forces" non-standard frequencies and physical interfaces
- Solution:
  - Provide an adapter board that can be use in the lab for 100% compatibility with the standard
  - The adapter board designed by the GBT team and available to the users

Forward error correction (FEC)

- Objectives:
  - Correct burst errors:
    - Generated on the PIN-diode
    - Generated by particles hitting the transceiver
    - Generated in the fast SERDES circuits (which cannot be triplicate)
    - Done with minimal latency
    - Done with good efficiency
    - Merge with line-coding
- Proposed code:
  - Compatible with FPGAs capabilities
  - Interleaved Reed-Solomon double error correction
  - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - **$2_{Interleaving} \times 2_{RS} = 4$ symbols $\cong$ 16-bits**
  - Code efficiency: 88/120 = 73%
  - Line speed: 4.80 Gb/s
  - Coding/decoding latency: one 25 ns cycle

Line coding


SC<3:0>
TTC<15:0>
D<63:0>
Scrambler
SCR<83:0>
RS encoder
EC<31:0>
Serializer
Frame type
Header
H<3:0>
Deserializer
Frame<119:0>
RS decoder
SCR<83:0>
Descrambler
SC<3:0>
TTC<15:0>
D<63:0>
H<3:0>

Summary

- We propose a "Single" Link solution for:
  - Timing Trigger Links
  - Data Acquisition Links
  - Experiment Slow Control Links
- The link is based on:
  - The GBT chip set in the detectors:
    - GBT13, GBTIA, GBLB & GBT-SCA
  - Optoelectronics from the Versatile Link Project
  - An FPGA in the counting room
- Both ends implement a error robust transmission protocol over an optical fibre
- The GBT13 communicates with the front-end electronics with up 32(+1) e-links
- Two or more e-links can be grouped to match the front-end bandwidth
- We propose that the e-links communicate using the Ethernet protocol
- An E-link Port Adaptor "macro" will be provided by the GBT team for integration in the front-end ASICS
- Slow control is implemented by a dedicated channel
  - One e-link
  - Slow control is managed by the GBT-SCA