The ATLAS Level-1 Muon to Central Trigger Processor Interface

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Abstract

The Muon to Central Trigger Processor Interface (MUCTPI) is part of the ATLAS Level-1 trigger system and connects the output of muon trigger system to the Central Trigger Processor (CTP). At every bunch crossing (BC), the MUCTPI receives information on muon candidates from each of the 208 muon trigger sectors and calculates the total multiplicity for each of six transverse momentum (p_T) thresholds. This multiplicity value is then sent to the CTP, where it is used together with the input from the Calorimeter trigger to make the final Level-1 Accept (L1A) decision. In addition the MUCTPI provides summary information to the Level-2 trigger and to the data acquisition (DAQ) system for events selected at Level-1. This information is used to define the regions of interest (RoIs) that drive the Level-2 muon-trigger processing.

The MUCTPI system consists of a 9U VME chassis with a dedicated active backplane and 18 custom designed modules. The design of the modules is based on state-of-the-art FPGA devices and special attention was paid to low-latency in the data transmission and processing. We present the design and implementation of the final version of the MUCTPI. A partially populated MUCTPI system is already installed in the ATLAS experiment and is being used regularly for commissioning tests and combined cosmic ray data taking runs.

I. ATLAS First Level Muon Trigger

The ATLAS Level-1 trigger [1] uses information on clusters and global energy in the calorimeters and multiplicities from tracks found in the dedicated fast muon trigger detectors in order to reduce the event rate to 100 kHz with an overall latency of less than 2.5 µs.

The muon trigger detectors are resistive plate chambers (RPC) in the barrel region and thin-gap chambers (TGC) in the end-cap and forward regions of ATLAS. Coincidences of hits in different detector layers are used to identify muon candidates. The muon trigger electronics also determines the transverse-momentum (p_T) of the muon candidates and classifies them according to six programmable p_T thresholds.

The muon trigger detectors are divided into sectors, 64 for the barrel, 96 for the end-cap and 48 for the forward region. Each sector can identify up to two muon candidates. The trigger sector logic modules send information about the position and p_T threshold of the muon candidates to the MUCTPI at the bunch crossing (BC) rate of 40.08 MHz.

An overview of the muon trigger system is shown in Figure 1 below.

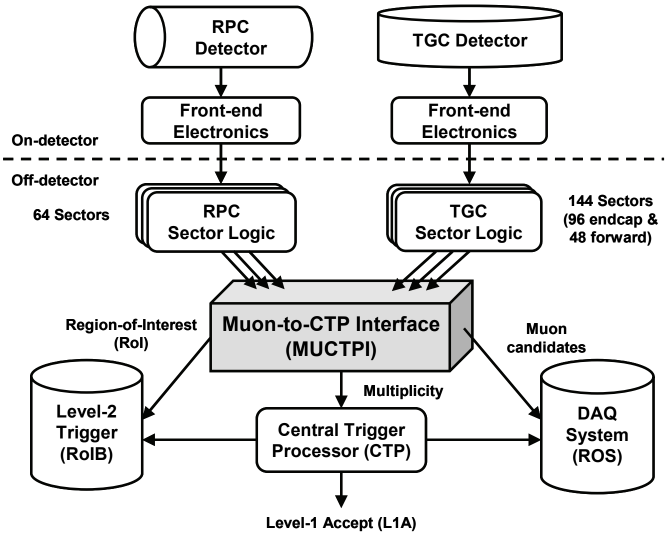

Figure 1: Overview of the ATLAS Level-1 muon trigger

II. Muon to Central Trigger Processor Interface (MUCTPI)

The MUCTPI combines the information from all of the muon trigger sectors and calculates total multiplicity for each of the six p_T thresholds, also resolving possible double counting of muon candidate tracks that traverse more than one detector region, and forwards these multiplicity values to the CTP which takes the final Level-1 decision.

In addition the MUCTPI provides data to the Level-2 trigger and to the DAQ system for events selected at Level-1. The DAQ system receives a formatted copy of the information on candidate muon tracks as well as computed candidate multiplicity. The Level-2 trigger system receives a subset of the candidates, ordered according to decreasing p_T. This information is used to define regions of interest (RoIs) that drive the Level-2 muon-trigger processing.

The MUCTPI has to avoid double counting muons which traverse more than one set of trigger chambers [2], since this would lead to an unacceptably high rate of fake di-muon triggers. This effect is particularly marked for low-p_T muons as their tracks are considerably deflected by the magnetic field.

Figure 2 below illustrates the overlap between the barrel and end-cap muon trigger chambers. Tracks for low and high-p_T muons in the barrel and end-cap chambers as well as an example of a muon track that would be detected in both systems are shown. The MUCTPI has to detect this case and to suppress one muon candidates in overlap in the multiplicity.

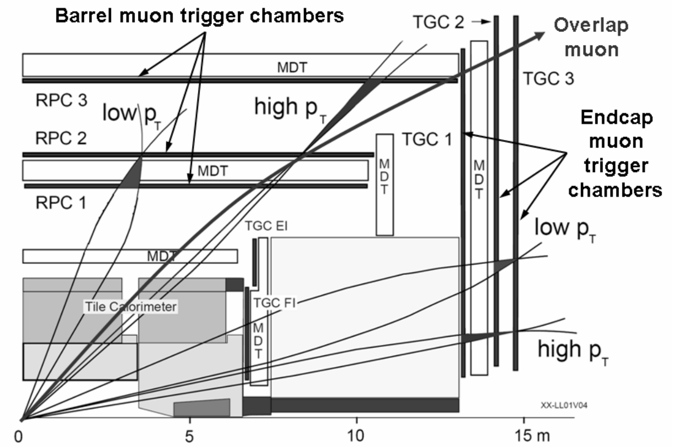

Figure 2: Barrel and end-cap muon trigger chambers

III. MUCTPI ARCHITECTURE

The MUCTPI system consists of a 9U VME chassis with a dedicated active backplane and three types of custom designed modules as shown in Figure 3 below.

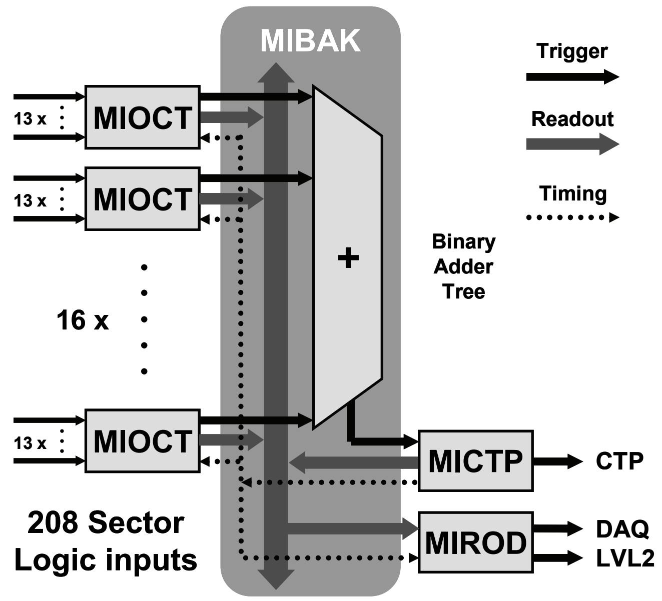

Figure 3: MUCTPI architecture

The different components of the MUCTPI system are introduced in the following sections.

A. MIOCT Module

Each of the 16 octant modules processes information on muon candidates received from 13 trigger sectors which cover one octant in φ and one half in η of the muon trigger detectors. It calculates the local muon candidate multiplicities and avoids double counting of muon tracks detected in overlapping sectors.

An early prototype of the MIOCT module exists, which provides most of the required functionality but misses some flexibility in the overlap handling and only supports a limited number of sector inputs. A complete redesign of the MIOCT module was therefore undertaken. The new MIOCT allows a seamless upgrade of the MUCTPI system since it is fully compatible with the existing backplane. The design and implementation of the final module are presented in section IV below.

B. MICTP Module

The CTP interface module receives the total multiplicity sums for the 6 p_T thresholds from the MIBAK backplane and sends them to the CTP. It also writes the multiplicities into a pipeline for read-out by the MIROD module on reception of a Level-1 Accept from the CTP. In addition the MICTP receives the external timing and triggers signals, such as the 40 MHz bunch clock (BC), the Level-1 Accept (L1A), the LHC orbit signal and the event counter reset, from the CTP and distributes them through the backplane to the other modules in the MUCTPI crate. The MICTP also provides features for monitoring the multiplicity sums through the VME bus.

C. MIROD Module

The readout driver module collects the muon candidates from the 16 MIOCT modules and the multiplicity from the MICTP for every L1A received. It then sends this data after formatting to the Level-2 trigger and the DAQ system. The are used for this purpose. The MIROD also allows reading out the selected muon candidate data via the VME bus for monitoring purposes.

The existing MIROD prototype also needed to be redesigned, since it was not directly compatible with the ATLAS standard version of the S-LINK [3] mezzanine cards (HOLA). The design and implementation of the final MIROD module are presented in section V below.

D. MIBAK Backplane

The dedicated active backplane calculates the overall multiplicity by adding the muon candidate multiplicities from the 16 MIOCT modules. The multiplicity summing is performed by a binary adder tree implemented using Altera MAX7000 CPLDs for low latency. In addition the backplane implements a bus for the transfer of readout data from the MIOCT modules and the MICTP to the MIROD. This shared readout bus uses a token passing protocol for arbitration and is based on Bus LVDS (BLVDS) [4] signaling. Finally the MIBAK distributes the trigger and timing signals with low-skew to all the modules in the crate. The MIBAK is mounted in the J3 position of the 9U VME crate.

IV. OCTANT MODULE (MIOCT)

The MIOCT is implemented as a 9U x 400 mm VME64x module. The 13 sector logic inputs use 32-bit parallel LVDS signalling at 40 MHz. Serial transmission was excluded because of the latency penalty of ~3 BC for serialization and de-serialization. Using 2x68-pin high-density dual-stacked VHDCI connectors and low-skew SCSI-3 twisted-pair cable [5], it is possible to fit all 13 sector logic inputs on the front-panel of the module. Figure 4 below shows the block diagram of the MIOCT module.

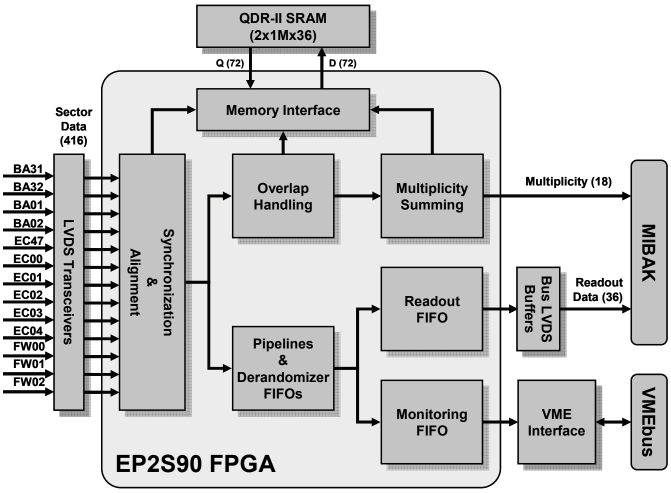

Figure 4: MIOCT block diagram

The main functionality of the MIOCT is implemented in one Altera Stratix II FPGA [6]. This chip features sufficient memory, logic and I/O resources to allow integration of the main MIOCT processing into a single device. There is an additional small Altera Cyclone-II FPGA for the VME bus interface, which is based on the firmware [7] developed for the modules of the CTP. Figure 5 below shows a picture of the final MIOCT module.

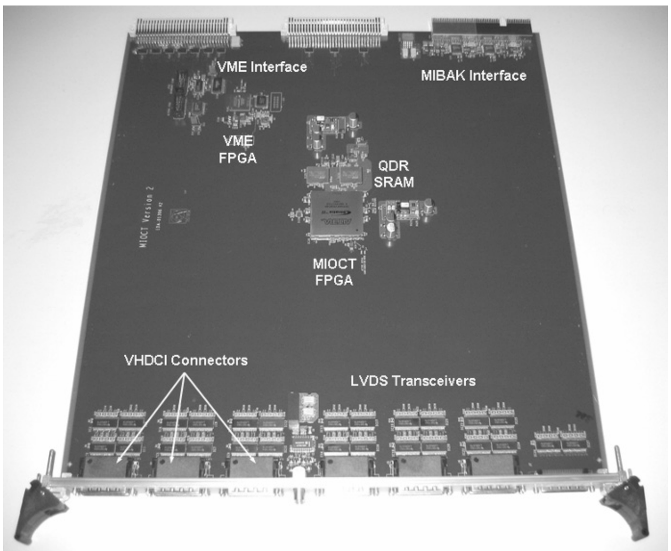

Figure 5: MIOCT module picture

A. Trigger Path

The signals received from the detector sector logic are resynchronized with the system clock received from the MICTP. The incoming sector words are aligned in time to compensate for the different latencies introduced by the RPC and TGC detector specific electronics and the different cable lengths. The MIOCT checks the alignments to be sure that the data words from each of the sector correspond to the same bunch crossing.

The multiplicity summing logic counts the number of muon candidates for each of the 6 p_T thresholds, taking into account possible overlaps between sectors. The overlap handling logic suppresses one of the muon candidates if there is a candidate in the corresponding overlap zone of an adjacent sector as well. More details on the overlap handling are given in section D below. The total number of muon candidates is encoded into six 3-bit words and sent to the MIBAK backplane for overall summing.

The internal logic is operated at 4 times the bunch clock (~160 MHz) in order to minimize the latency while maintaining a pipelined architecture. The latency of the trigger path is 3 BC, which is consistent with the existing demonstrator implementation.

B. Readout Path

All the data received from the muon sectors are stored in pipeline memories for the duration of the latency of the Level-1 trigger. In case of a Level-1 Accept, data of all input channels are read out from the pipelines and written into derandomizer FIFOs. The readout window is programmable up to ±2 bunch crossings around the trigger. The data in the derandomizer FIFOs are zero-suppressed in order to reduce the data rate on the backplane, formatted and buffered until they are read out via the MIBAK backplane. The data sent by the MIOCT module can also be read out for monitoring purposes using the VME bus.

C. Muon Candidate Overlap Handling

Each MIOCT module receives data from four barrel, six end-cap and three forward sectors of the muon trigger. The overlap regions of adjacent sectors of an octant that can be resolved by the MIOCT are illustrated the in Figure 6 below.

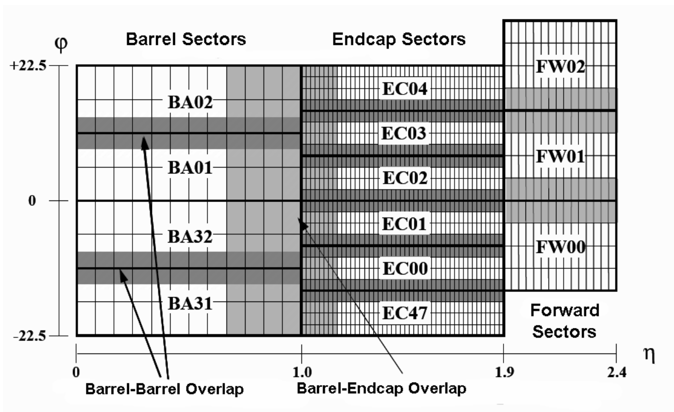

Figure 6: Overlap regions

Overlaps of chamber regions within sectors are handled by the detector sector logic. There are no overlaps between adjacent octants. The overlap handling logic detects overlaps between muon candidates from different sectors based on their location or sub-sector address and, in the case of the barrel/end-cap overlaps, their p_T threshold and charge sign as well. The result of the overlap detection together with a comparison of the p_T values is used to determine which of the two muon candidates in overlap should be suppressed in the overall muon multiplicity of the octant. The overlap handling logic is implemented using programmable look-up tables (LUT) and the overlap policy can therefore easily be changed by reloading these LUT through the VME bus interface. The contents of the LUTs will be determined from offline simulations.

D. Snapshot/Test Memory

The MIOCT also features a snapshot and test data memory. The memory can be used to store the data from all 13 input sectors as well as the calculated candidate multiplicity, the candidate suppression flags and a timestamp. This is useful during the timing-in of the system as well as for diagnostics and monitoring purposes during data taking. The depth of the snapshot memory is 128K bunch crossings per sector, which corresponds to ~36 LHC turns. For module test purposes, the memory can also be used to replay test data. The snapshot/test memory is implemented using two 1Mx36-bit Quad-Data Rate (QDR) SRAM devices.

E. Status

Initially two prototypes of the final MIOCT were built and fully tested, one of which is currently being used in the ATLAS counting room. Integration tests with the RPC and TGC sector logic modules have been successful. The final production of 34 modules has now also been completed and the cards are currently being tested.

V. MIROD/CTP MODULE

Figure 7 below shows the block diagram of the new MIROD/CTP module.

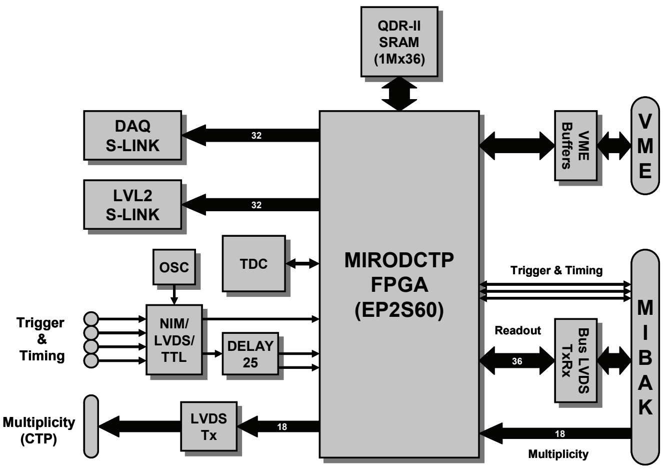

Figure 7: MIROD/CTP module block diagram

The design is based on a single Altera Stratix-II FPGA, which has ample memory, logic and I/O resources and therefore enables integration of the original design into a single device. Since all the necessary interfaces have been foreseen and are connected to the FPGA, the same PCB with a different firmware programming can also be used to perform the functions of the MICTP. This just requires mounting the front-panel connectors for the trigger and timing signals and the multiplicity instead of the S-LINK mezzanine cards. Figure 8 below shows a picture of the MIROD/CTP module with the S-LINK mezzanine cards mounted.

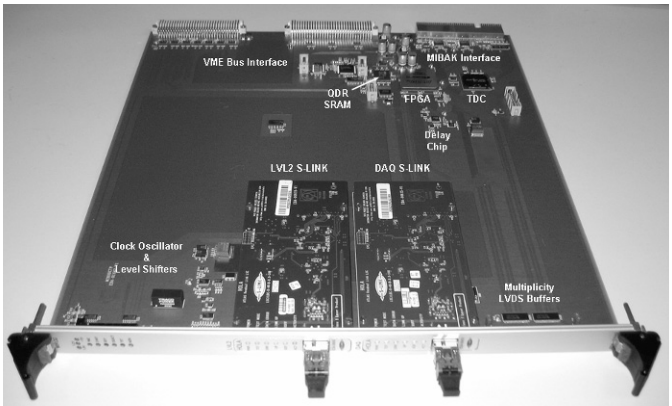

Figure 8: MIROD/CTP module picture

A. MIROD Functionality

When used to implement the MIROD, the FPGA receives the readout data via the BLVDS buffers from the MIBAK backplane and sends it after processing to the Level-2 and DAQ S-LINK mezzanine cards. It also receives the timing signals from the backplane.

B. MICTP Functionality

When using the board to implement the MICTP, the FPGA receives the trigger and timing signals from the front-panel through the appropriate level translators and distributes them after reshaping to the other modules in the crate via the backplane. The module also features a programmable delay chip (DELAY25) which allows clocks with different phases to be generated in order to latch signals at the optimum time. The design also included a TDC chip to monitor the phase of the external timing signals and the multiplicity which is useful during the timing-in of the system. Finally the FPGA receives the output of the multiplicity adder tree on the backplane, latches it and send it to the CTP via LVDS buffers. In case of an L1A the multiplicity is also written into a pipeline memory in order to be read out via the MIBAK bus.

C. Common Features

The VME interface is required for both applications and is based on the same design as the MIOCT, however without using a separate small FPGA. The module also features a snapshot and test data memory which can be used to capture data from the MIBAK backplane for monitoring and diagnostics or to replay data for module test purposes. The memory is implemented as a single 1Mx36-bit QDR SRAM device.

D. Status

A first prototype of the MIROD/CTP module has been assembled and is currently being tested. It is foreseen to produce a total of six of these module to allow for sufficient spares.

VI. SYSTEM INTEGRATION

A prototype of the MUCTPI was installed in the ATLAS underground counting room already in 2005. The MUCTPI is being incrementally upgraded to the final system. Integration tests of the MUCTPI with the CTP, the RPC and TGC trigger sector logic modules as well as the DAQ and Level-2 systems have been successful and the system has already been used in several combined cosmic ray data taking runs [8].

A full MUCPTI system has been assembled in the laboratory and integration tests are on-going. Figure 9 below shows a picture of the MUCTPI chassis with 16 of the final MIOCT modules installed. The MICTP and the final MIROD with the S-LINK mezzanine cards for the connection to the DAQ and Level-2 trigger systems are installed in the center slots. The crate also contains a single-board computer (SBC) in the leftmost slot for configuration, control and monitoring.

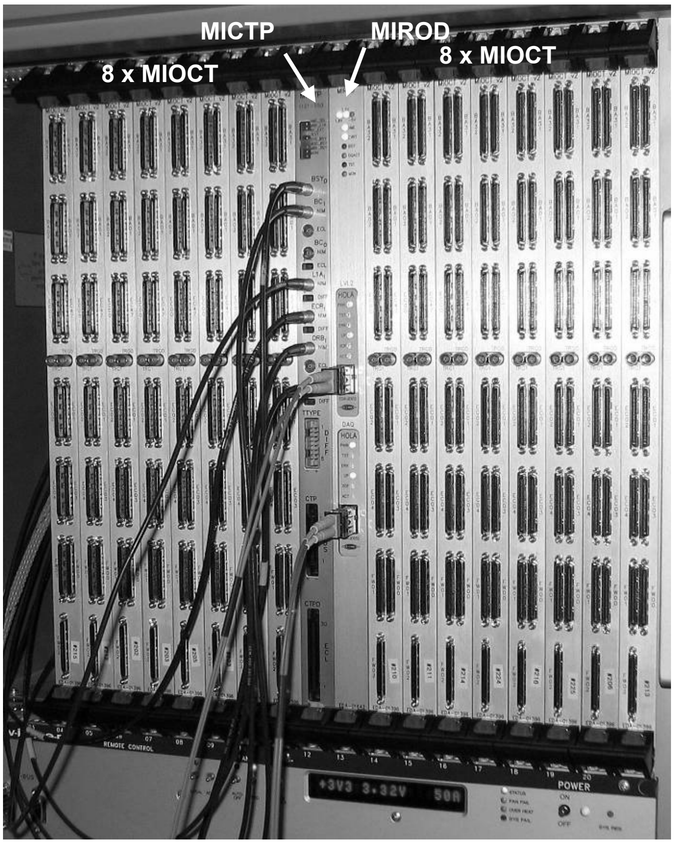

Figure 9: MUCTPI crate picture

VII. SUMMARY

The MUCTPI interfaces the 208 muon trigger sectors to the CTP. It calculates the muon candidate multiplicities for 6 p_T thresholds and avoids double counting of muons detected in overlapping sectors of an octant.

A partially populated MUCTPI system is installed in the ATLAS counting room and is regularly being used for commissioning tests and combined cosmic ray data taking runs with the muon trigger detectors as well as DAQ and Level-2 trigger. The system will be upgraded as more muon trigger sector inputs become available.

The final MIOCT module has been designed to replace the existing prototype. It features a flexible overlap handling architecture and the hardware implementation is highly configurable, being based on look-up tables in a large FPGA device. One of the modules is already installed in the MUCTPI system in the ATLAS counting room. The seriesl production of 34 modules is completed and the modules are currently being tested.

Finally the first prototype of the new MIROD/CTP module, which will replace the existing MIROD and MICTP modules, has been received and is being tested.

VIII. REFERENCES

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[2] P. Farthouat, "*Interfaces and Overlaps in the Level-1 Muon Trigger System*", ATLAS EDMS note ATL-DA-EN-0001.
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[4] National Semiconductor, "*LVDS Owners Manual*", http://lvds.national.com.
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[7] R. Spiwoks, "*The VMEbus Interface of the Central Trigger Processor*", ATLAS EDMS note ATL-DA-ES-0037. http://edms.cern.ch/document/428910
[8] R. Spiwoks et al., "*The ATLAS Level-1 Central Trigger*", these proceedings.