



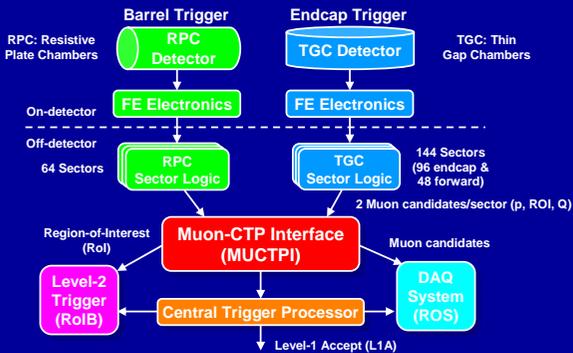
# The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)



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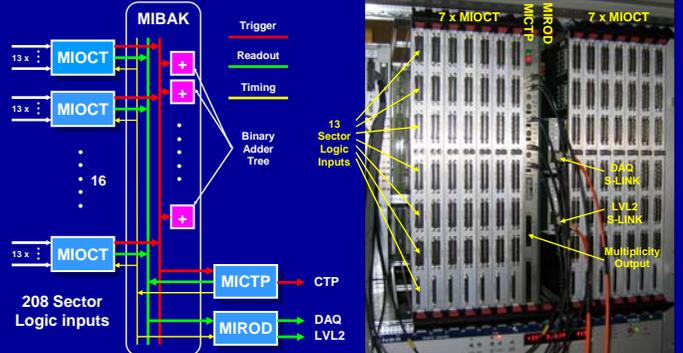
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## ATLAS Muon Trigger Overview



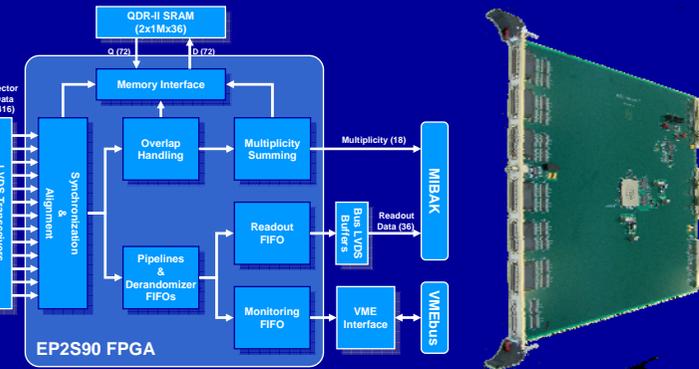
The Muon to Central Trigger Processor Interface (MUCTPI) is part of the ATLAS Level-1 trigger system and connects the output of muon trigger system to the Central Trigger Processor (CTP). At every bunch crossing, the MUCTPI receives information on muon candidates from each of the 208 muon trigger sectors and calculates the total multiplicity for each of six momentum thresholds. This multiplicity value is then sent to the CTP, where it is used together with the input from the Calorimeter trigger to take the final Level-1 decision. In addition the MUCTPI provides data to the Level-2 trigger and to the data acquisition (DAQ) system for events selected at Level-1. This information is used to define regions of interest (RoIs) that drive the Level-2 muon-trigger processing.

## MUCTPI Architecture & Implementation



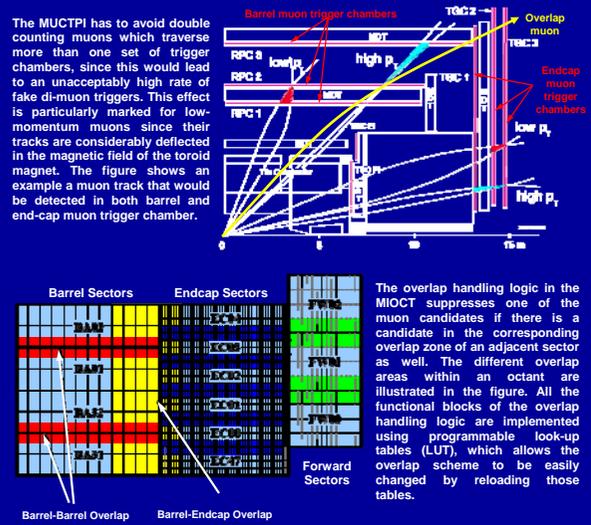
The MUCTPI system consists of a 9U VME64x chassis with a special backplane and 18 custom designed modules. Each of the 16 octant modules (MIOCT) receives and processes the muon candidate data from 13 sectors of the muon trigger detectors. It calculates the local muon candidate multiplicities and avoids double counting of muon tracks detected in overlapping sectors of an octant. The MIBAK backplane sums the multiplicity values of all MIOCT modules and also provides for readout data transfer and distribution of timing and trigger signals to all the modules in the chassis. The MICTP receives the external timing and triggers signals and sends the final multiplicity value to the CTP. The MIROD module collects information from the MICTP and the MIOCT modules and sends this data after formatting to the Level-2 trigger and the DAQ system via an optical S-LINK interface.

## MIOCT Module



The MIOCT is implemented as a 9U x 400 mm VME64x module. The 13 sector logic inputs use 32-bit parallel LVDS signalling at 40 MHz. Serial transmission was excluded because of the latency penalty of ~3 BC due to serialization and de-serialization. Using 2x68-pin high-density dual-stacked VHDCI connectors and low-skew SCSI-3 twisted-pair cable, it is possible to fit all 13 sector logic inputs on the front-panel of the module. The main functionality of the MIOCT is implemented in one Altera Stratix II FPGA which features sufficient memory, logic and I/O resources. The internal trigger path logic is operated at 4 times the bunch clock (~160 MHz) in order to minimize the latency while maintaining a pipelined architecture. The MIOCT also features a snapshot and test data memory which is implemented using two 1M x 36 bit Quad-Data Rate (QDR) SRAM devices. The memory can be used to store the data from all 13 input sectors as well as the calculated candidate multiplicity and various flags. This is useful during the timing-in of the system as well as for diagnostics and monitoring purposes. The depth of the snapshot memory corresponds to ~36 LHC turns. For module test purposes, the memory can also be used to replay test data.

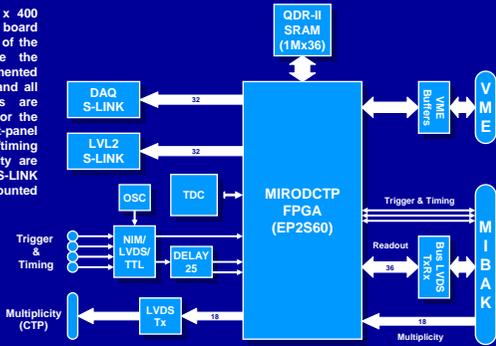
## Muon Candidate Overlap



The MUCTPI has to avoid double counting muons which traverse more than one set of trigger chambers, since this would lead to an acceptably high rate of fake di-muon triggers. This effect is particularly marked for low-momentum muons since their tracks are considerably deflected in the magnetic field of the toroid magnet. The figure shows an example a muon track that would be detected in both barrel and end-cap muon trigger chamber.

## MIROD/CTP Module

The MIROD/CTP is a 9U x 400 mm VME64x module. The board can perform the functions of the MIROD or MICTP, since the processing can be implemented in a single FPGA device and all the necessary interfaces are foreseen in the design. For the MIROD version, the front-panel connectors for the trigger/timing signals and the multiplicity are not required and the S-LINK mezzanine cards are mounted instead.



The MIROD collects the muon candidates from the 16 MIOCT modules and the multiplicity from the MICTP via the readout bus on the MIBAK whenever a Level-1 Accept is received from the CTP. It then sends the combined data after formatting to the DAQ and Level-2 trigger systems using the standard S-LINK optical link mezzanine cards. The MICTP module receives the total multiplicity sums from the adder tree on the MIBAK backplane and sends them to the CTP. It also writes the multiplicities into a pipeline for read-out by the MIROD module. In addition the MICTP receives the timing and triggers signals, from the CTP and distributes them through the backplane to the other modules in the MUCTPI crate. The module also features a memory for testing and monitoring purposes. A prototype of the board is currently in assembly.

## Commissioning

