Development of a selftriggered high counting rate ASIC for readout of 2D gas microstrip neutron detectors.

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Outline

- DETNI project
- Hybrid Micro-Strip Gas Chamber neutron detector
- MSGCROC ASIC

Goals of the DETNI project

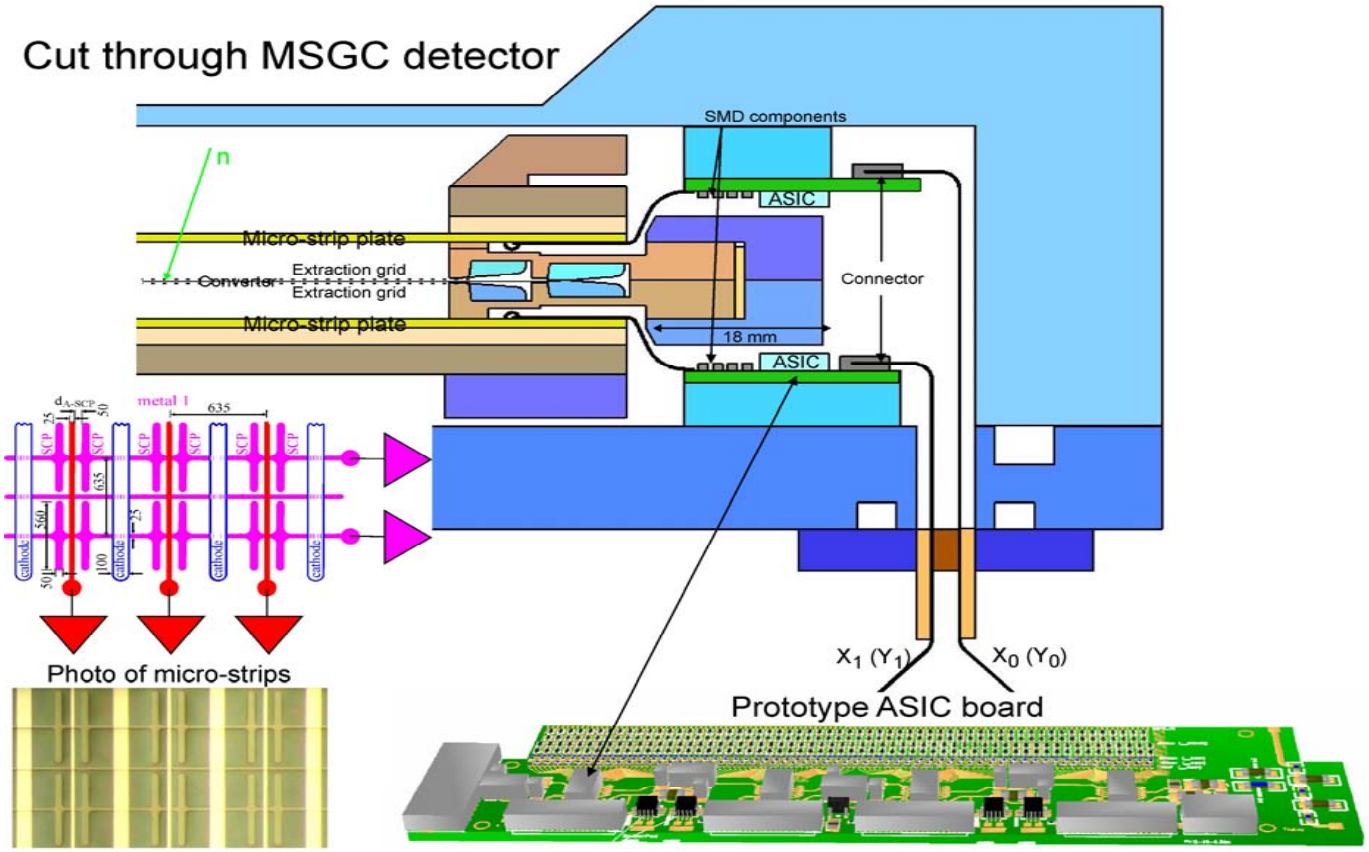
Development of 2D hybrid detectors for future high intensity neutron sources:

- ^{157}Gd/Si micro-strip detector (Si-MSD)
- ^{157}Gd/CsI micro-strip gas chamber detector (MSGC)
- Cascaded ^{10}B-coated GEM detector (CASCADE)

Development of readout ASICs:

- *n-XYTER* (Si-MSD & CASCADE)
- *MSGCROC* (MSGC)

^{157}Gd/CsI MSGC neutron detector

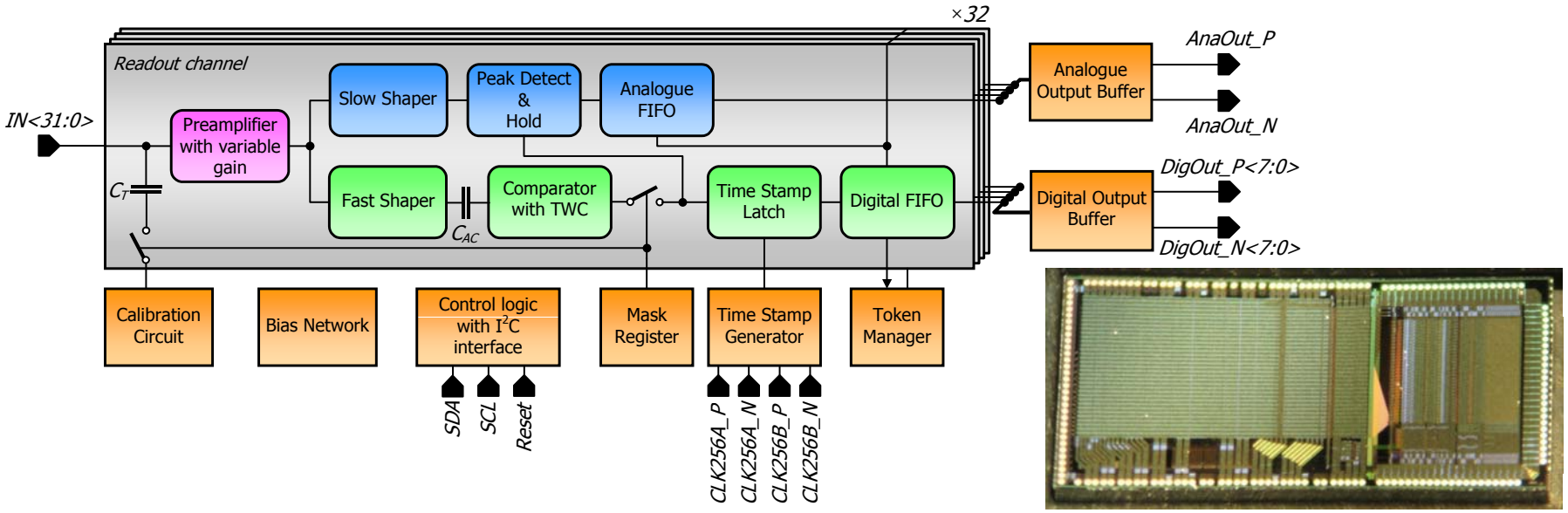


- Composite ^{157}Gd/CsI neutron converter foil, on negative electrical potential with extraction grids on either side, located in the central detector plane
- Two adjacent low-pressure (p~20mbar) preamplification gas gaps on either side of the converter followed by amplification at constant reduced field strength E/p.
- Two micro-strip gas detector planes, which function as third amplification and readout elements (400 stripes per detector module).

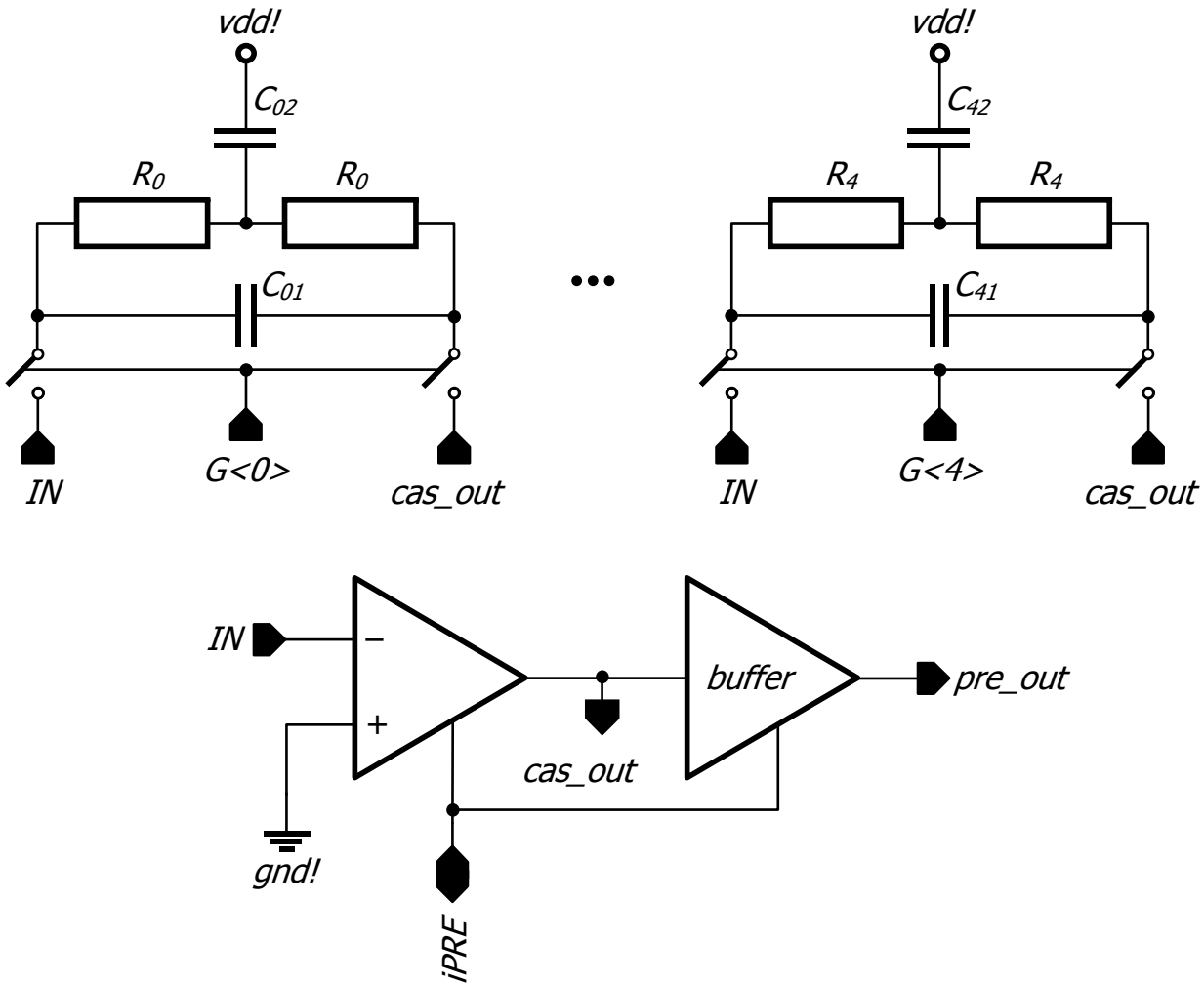
MSGCROC ASIC

- Parameters to be measured: X/Y,T, E_X/E_Y
- Detector strip capacitance: ~ 23 pF
- Strip multiplicity per event: ~ 3.5 (c.o.g.)
- Hit rate per strip: ~ $9 \cdot 10^5$ /s
- Input signal charge: $2 \cdot 10^5$ e^- - $5 \cdot 10^6$ e^- (depending on gas gain)
- ENC required for E (5σ threshold): ~ 2000 e^- rms

- X/Y coincidence window 2 ns + (E_X = E_Y)
- Discriminator: time walk < 2 ns, jitter < 1 ns FWHM.
- The preamp-shaper circuits must handle both polarities of the input signal and deliver signals of one polarity to the discriminator and peak detector circuit.
- Variable gain to cope with different detector gas gains

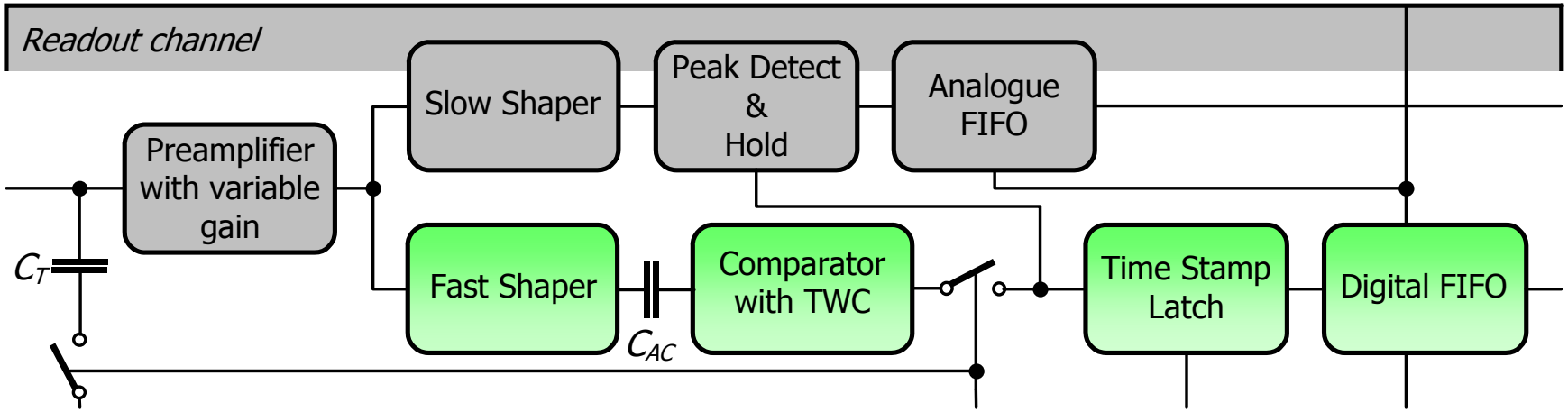


Input stage



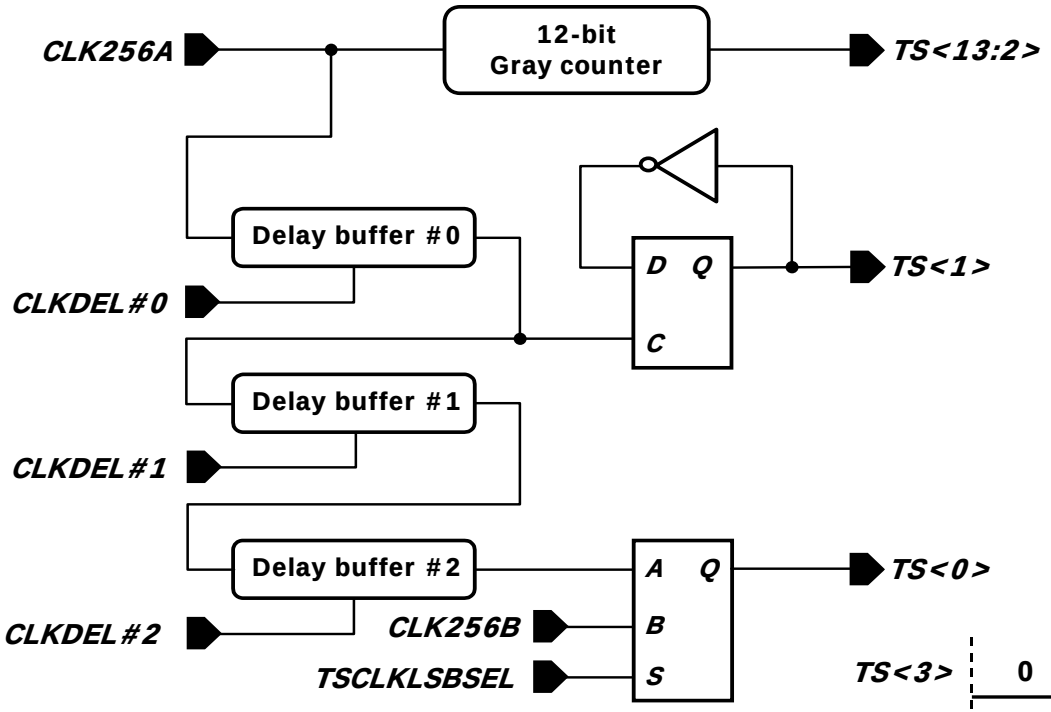
- The input stage is a transimpedance amplifier built around a folded cascode wide band amplifier with a bridged-T low-pass filter in the feedback loop.
- Gain factors: ×1, ×2, ×4, ×8, and ×16.

Timing channel



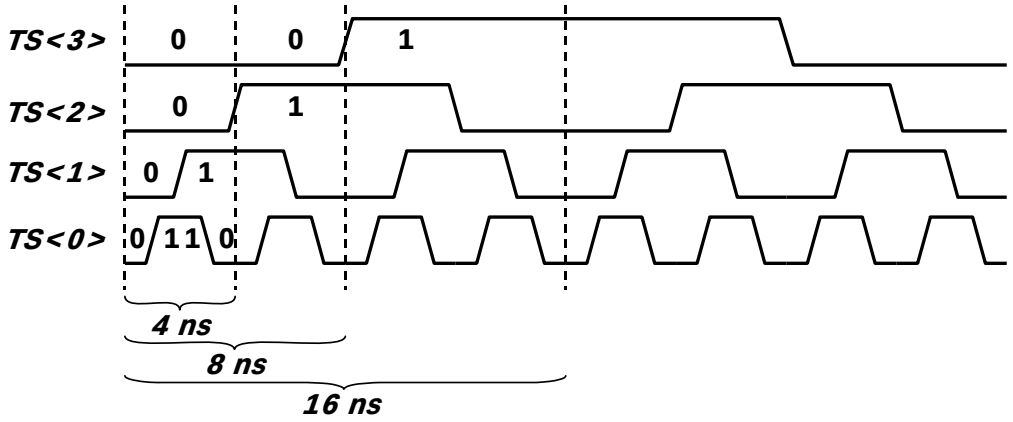
- T_{peak} = 25 ns
- T_{walk} < 2 ns
- Each comparator is equipped with a 5-bit trimming DAC, which allows to correct the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC common for all channels

Time Stamp Generation



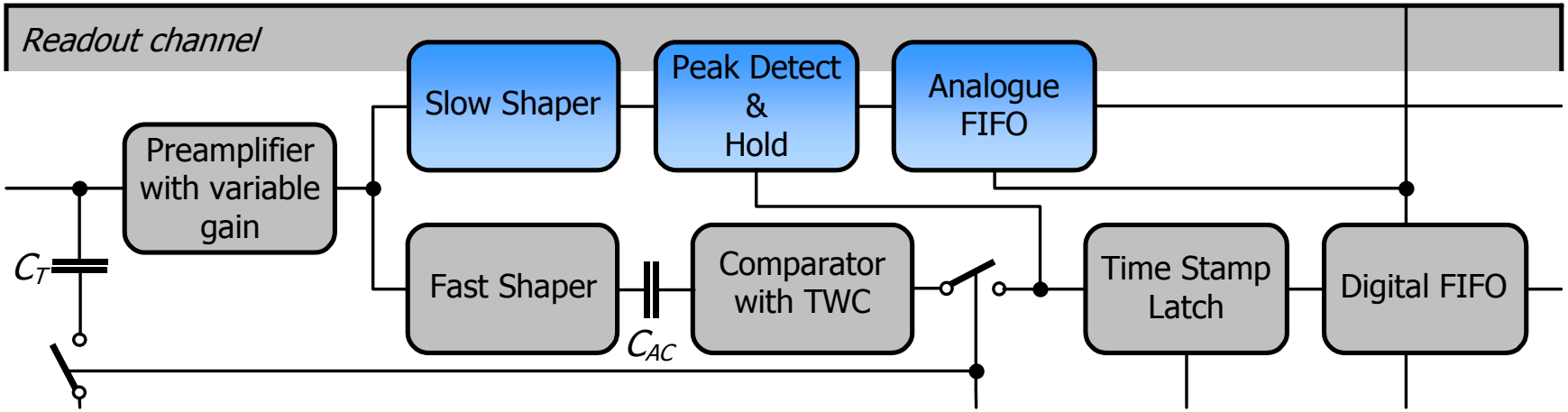
The 14-bit time stamp signature is combined of:

- 12-bit Gray-encoded counter,
- toggle flip-flop
- and input clock.



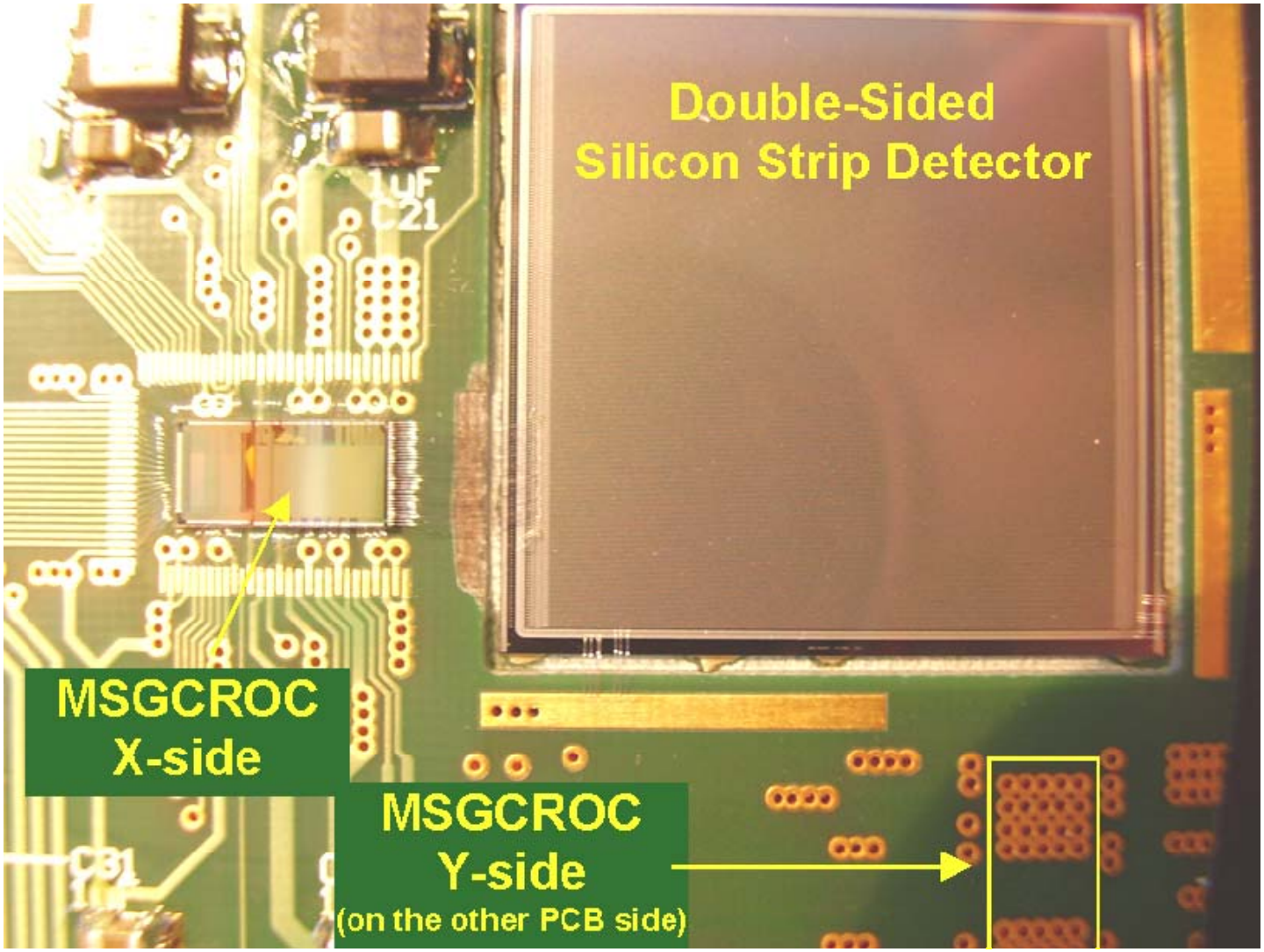
In this scheme we can achieve 1 ns resolution at 256 MHz input clock frequency.

Energy channel

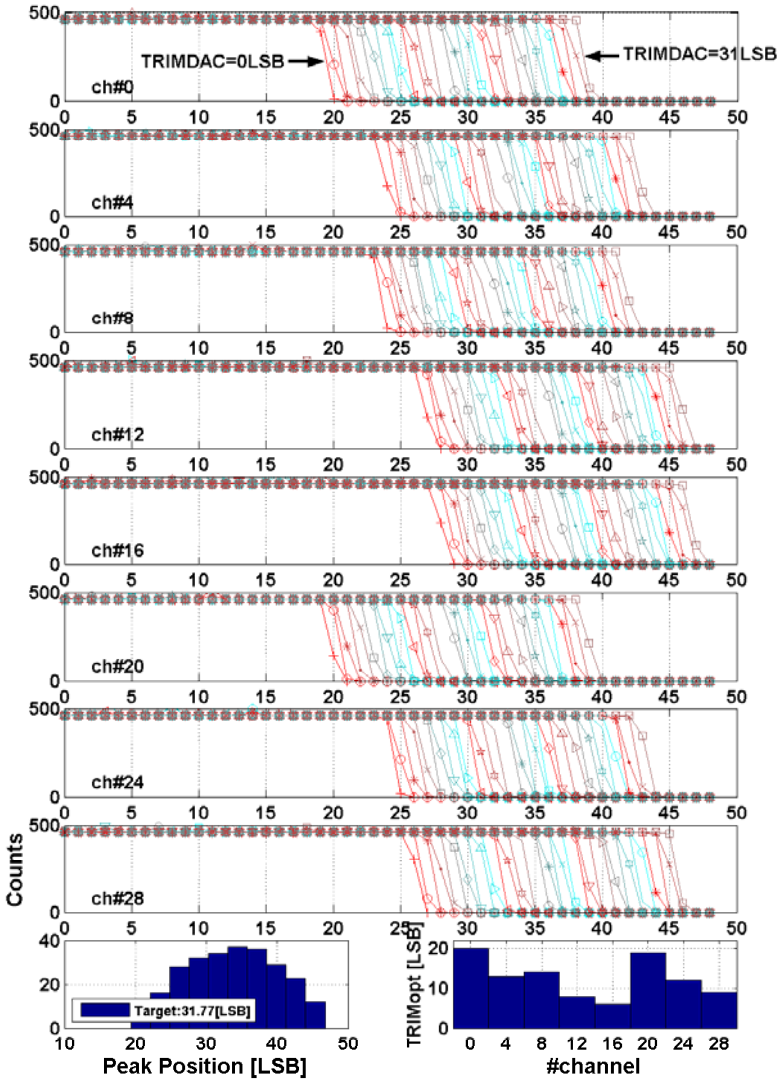


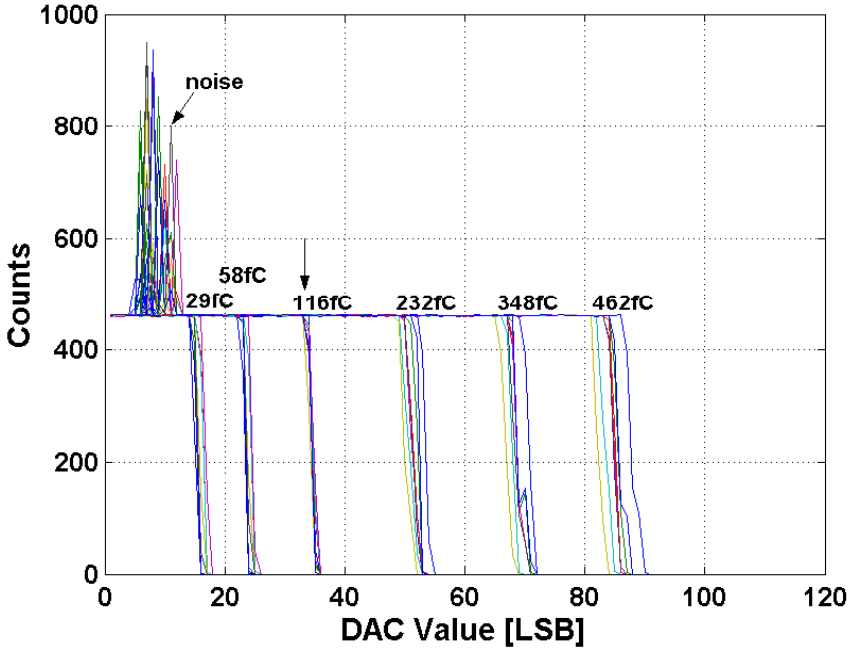
- T_{peak} = 85 ns
- The PDH circuit detects peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel.

Test bench

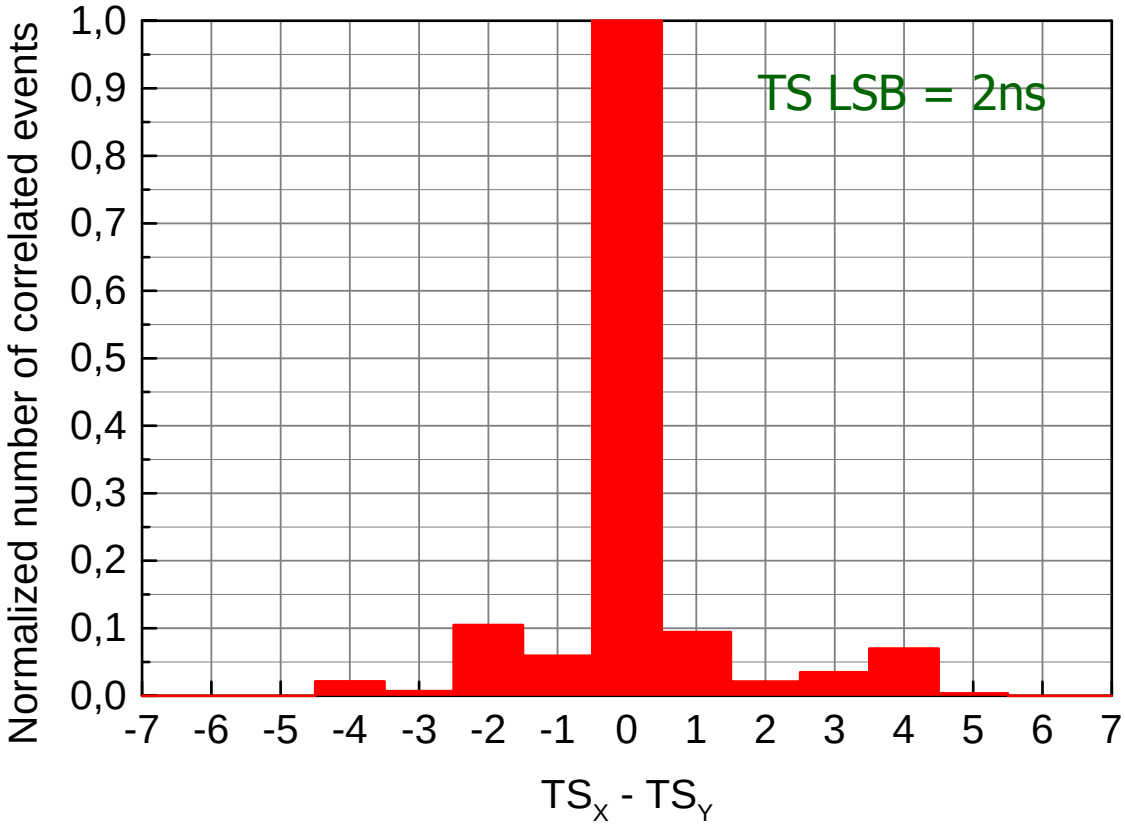

Double-Sided
Silicon Strip Detector
MSGCROC
X-side
MSGCROC
Y-side
(on the other PCB side)

Trimming procedure



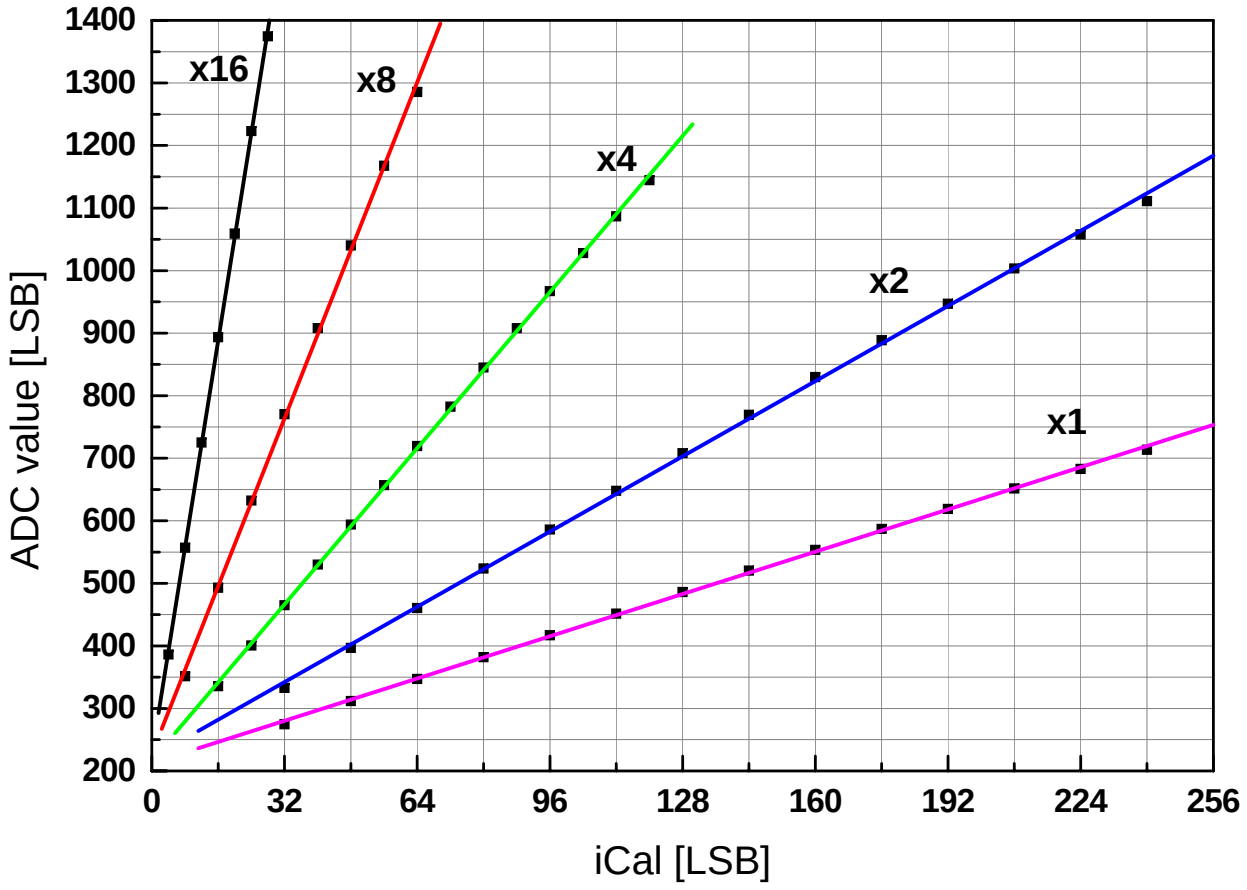


Timing measurements



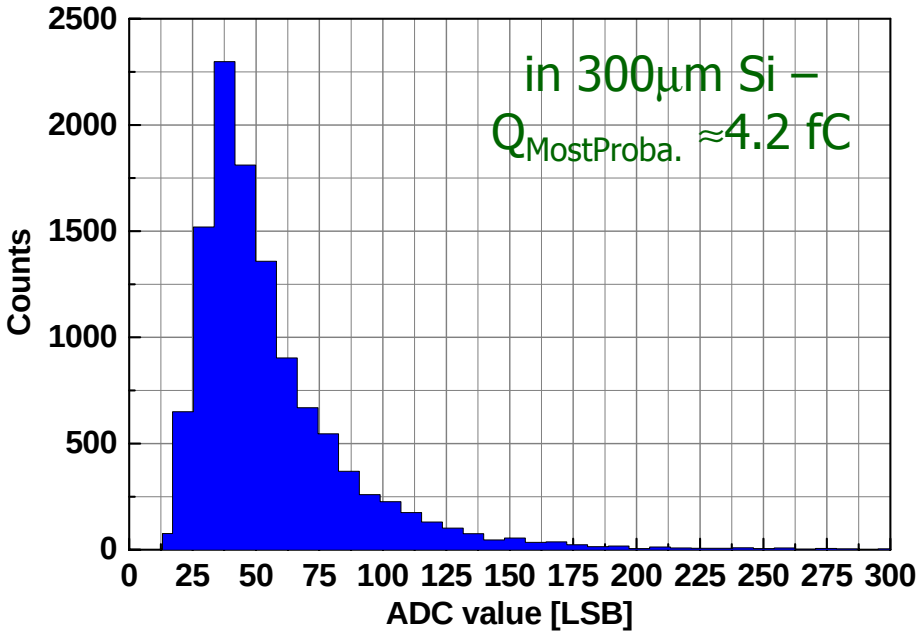
The histogram of Time Stamp coincidence between X and Y strips demonstrates the coincidence resolution of 2 ns as expected for the clock frequency of 128 MHz

Energy channel linearity



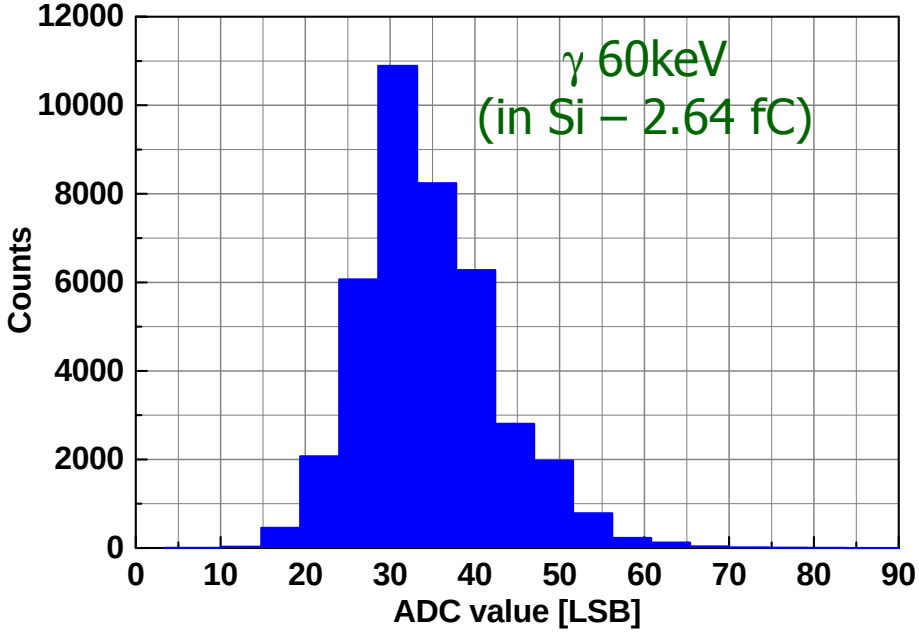
Measured gain factors: ×1, ×1.78, ×3.70, ×7.94, and ×19.58

Energy measurements



Amplitude distribution
Electrons ^{90}Sr source
Landau distribution

Amplitude distribution
γ-rays ^{241}Am source
Gaussian distribution



Summary

- Future high intensity pulsed neutron sources require novel detectors with higher counting rate capability and high time and position resolution. Novel detectors and dedicated advanced readout ASICs are developed in the frame of the European DETNI project.
- A first 32-channel ASIC with complete functionality required for readout of double sided MSGC detectors with composite ^{157}Gd/CsI converter has been designed and manufactured.
- The performed electrical tests of the ASICs as well as the measurements performed for a test bench module based on a double sided silicon strip detector have confirmed correct functionality of all building blocks and compliance of the ASIC parameters with the design specifications.
- The developed MSGCROC ASIC is a first experimental proof of the novel method of readout of double - sided strip detectors, which makes these technologies suitable for high count rate measurements with count rates up to 10^8/s per detector segment and 2-D spatial resolution below 100 mm FWHM. With these parameters the double - sided strip detector technology becomes competitive with the technologies based on pixelated detectors.