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Development of a selftriggered high counting rate ASIC for readout of 2D gas microstrip neutron detectors.

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In the frame of the DETNI project a 32-channel ASIC suitable for readout of a novel 2D thermal neutron detector based on a hybrid low-pressure Micro-Strip Gas Chamber and solid 157Gd converter has been developed. Each channel delivers position information, a fast time stamp of 2 ns resolution and signal amplitude proportional to the energy. The time stamp is used for correlating the signals from X and Y strips while the amplitude is used for finding center of gravity of a cluster of strips. The timing and energy information are stored in derandomizing buffers and readout via token ring architecture.

Summary

In the frame of the EU project DETNI (DETectors for Neutron Instrumentation) of NMI3 three hybrid 2D thermal neutron detectors for future high intensity pulsed neutron sources (like ESS) are developed. One of these detectors is a low-pressure Micro-Strip Gas Chamber (MSGC) with solid 157Gd/CsI converter suitable for applications in imaging, quasi-Laue diffraction, very high resolution single crystal diffraction and very high resolution focusing low-Q small angels scattering. The very demanding requirements of global counting rate of 10ˆ8 cps and two-dimensional position resolution of 50-100 um FWHM over a detector segment area of 25x25 cmˆ2 covered with 400x400 strips can be met only provided that the readout electronics is realized as multi-channel Application Specific Integrated Circuits (ASICs).

Reconstruction of a neutron position requires timing, spatial and energy data from both (X/Y) detector planes. To extract these data, after the preamplifier each readout channel is split into a timing and an amplitude (energy) channel. The preamplifier incorporates a transimpedance amplifier with a folded cascode core and a switchable feedback loop employing bridged-T lowpass filter. One can choose between 5 different loops to cover possible variation of the internal multiplication gain of the detector. The timing channel consists of a fast shaper (Tp = 25 ns) and a comparator with a Time Walk Compensation circuit (TWC) while the energy channel comprises a slow shaper (Tp = 85 ns) and a classical peak detector and hold circuit (PDH) which detects the peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel. To compensate the threshold offsets on the channel basis, each comparator is equipped with a 5-bit trimming DAC.

The output signal from the timing channel is used to latch a 14-bit time stamp with 2 ns resolution and to enable the PDH circuit in the energy channel. The 14-bit time stamp signature is combined of a 12-bit Gray-encoded counter (TS<13:2>), a toggle flip-flop (TS<1>) and the buffered input clock (TS<0>). The correct timing of bits TS<1> and TS<0>, to ensure Gray encoded of all 14 bits, allows us achieve 1 ns resolution at 250 MHz clock frequency.

The output signals from the PDH and the time stamp are stored in analogue and digital derandomizing buffers (four-stage FIFOs), respectively. The readout of the memories is performed via a token-ring based multiplexer which ensures data sparsification, so that only non-zero data are read out from the buffers.

The MSGCROC ASIC has been designed and manufactured in the 0.35um CMOS process from Austria Microsystems. The dimensions of the ASIC are 3.2×6.7 mmˆ2.

In the paper we present the functional architecture and critical aspects of the ASIC design, results of electrical testing as well as examples of physical measurements.

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