A Circuit Topology suitable for the Readout of Ultra Thin Pixel Detectors at SLHC and Elsewhere

M.Campbell, R.Ballabriga, E.Heijne, X.Llopart, L.Tlustos, W.Wong

CERN, 1211 Geneva 23, Switzerland

michael.campbell@cern.ch

Abstract

Hybrid pixel detectors provide unrivalled track finding capabilities for the LHC vertex detectors. Further reducing the material budget is of crucial importance among the many challenges which must be addressed by the vertex systems at the SLHC. Here we propose a two stage front-end readout architecture whereby the discrimination is performed on the sum of the total charge deposited in a number of pixels prior to readout of the analog or binary hit information per pixel. The readout concept is based on ideas developed in the framework of the Medipix3 project which aims to mitigate the effects of charge sharing in single photon processing systems. We indicate that it should be possible to obtain 100 % hit detection efficiency using a 50 μm thick Si detector segmented into pixels of 20 μm x 150 μm using a threshold of ~ 1 200 e^-. The paper focuses on simulations of the new circuit architecture using planar sensors

I. Introduction and Motivation

Hybrid pixel detectors provide unrivalled track finding at the LHC vertex detectors. This capability is derived from the use of a discriminator in each pixel with a threshold of some thousands of electrons on channels which have readout noise of a few hundreds of electrons only. Even in systems with 10^7 - 10^8 channels it is possible to keep the noise hit rate to a manageable level (<10^{-5} hits/pixel/s) while maintaining ~ 100 % detection efficiency. However, if the detector thickness is reduced and/or radiation damage degrades charge collection in the sensor it becomes more and more difficult to maintain this performance. Moreover, with the planned luminosity increase foreseen at the SLHC track finding will only become more difficult.

In parallel with the construction of the LHC vertex detectors the Medipix2 Collaboration [1] has been exploring the use of pixel detector techniques for energy sensitive single photon processing [2]. The primary limitation to the energy resolution in such systems comes from charge diffusion in the sensor: when a photon impinges on the sensor near to the edge of a pixel diffusion during collection causes the deposited charge to be shared between neighbouring pixels. The Medipix3 Collaboration [1] aims to overcome this limitation by using a sophisticated front-end architecture whereby the charge deposited simultaneously in neighbouring pixels is summed prior to a threshold being applied. This results in each pixel detecting an undistorted spectrum providing simultaneously high spatial resolution and good energy resolution [3].

In particle physics experiments the Landau distribution, which is produced by Minimum Ionising Particles (MIP's) in a semiconductor sensor, is similarly distorted when the sensor is highly segmented. Therefore in order to obtain 100 % hit detection efficiency most pixel vertex detectors run with a threshold which is at least 3 times lower that the most probable peak of the Landau distribution. Moreover, optimum spatial resolution is obtained when single and double hit clusters are equally prevalent and this condition is obtained by reducing the threshold even further [4]. Given the move towards thinner detectors for SLHC, it would appear interesting to consider the impact of using an architecture similar to that of Medipix3 in pixel vertex detectors.

Section II describes the Medipix3 architecture and how it resolves the charge sharing issue in single photon counting systems. In section III we describe how a similar architecture may be applied to vertex detectors at SLHC. In Section IV we present results of a design study of a front-end circuit which uses the new architecture in the SLHC environment. Finally, in Section V we will draw some conclusions from this work and indicate possible future developments.

II. The Medipix3 Architecture

The schematic of the Medipix3 prototype chip is shown in fig.1.

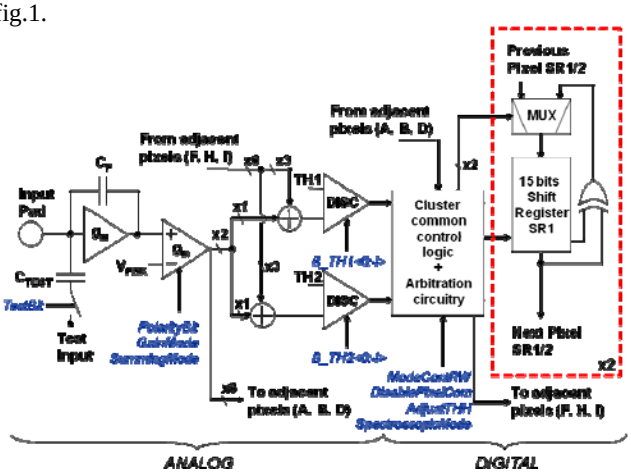

Figure 1: The block diagram schematic of the Medipix3 pixel readout architecture.

Charge collected on a pixel is integrated by a Charge Sensitive Amplifier (CSA) on a feedback capacitance. The CSA is based on the Krummenacher architecture [5]. The output of the CSA is filtered by means of a first order semi-gaussian shaper which acts both as a transconductance and as a noise filter. The shaper also AC couples the output of the preamplifier to the rest of the circuit and makes the system

less sensitive to the variations of the preamplifier characteristics. Furthermore the shaper generates 8 currents whose amplitude is proportional to the charge collected on the input electrode.

The currents generated in the shaper are sent to nodes common to a cluster of 4 pixels, the adding nodes being located effectively at each pixel corner. As there are 2 discriminators associated with each pixel, there are 2 adding nodes per pixel corner.

The discrimination process is done by applying an offset (threshold) to the sum of the four currents. Each summing node is connected to its own independent discriminator. Once the discriminator signal is active the charge is assigned to the summing circuit with the biggest charge sum in the local neighborhood. The charge assignation decision is based on the operation of a system of arbitrators. Arbiter circuits decide between two requests (inputs), activating an acknowledgement for only one of them even if they arrive simultaneously.

When a given discriminator wins the arbitration decision a pulse is fed to a shift register which is controlled by the *Shutter* signal: when the *Shutter* is high the shift register is configured as a 15-bit pseudo-random counter which counts the discriminator pulses (with a dynamic range of 32768 counts). When the *Shutter* is low the data can be shifted from pixel to pixel and read out externally.

In this way the decision to count a hit as being above the threshold is taken based on the sum of 4 pixels and - providing the charge is fully collected within those pixels - a threshold scan would reproduce the full undistorted incoming spectrum. Thus a sophisticated front-end circuit mitigates the effect of charge diffusion within the sensor. The main disadvantage of this approach is that the effective front-end noise is doubled as the hit/no hit decision is taken on the sum of 4 uncorrelated amplifier outputs.

III. THE MEDIPIX3 FRONT-END CONCEPT APPLIED TO VERTEX TRACKING AT SLHC

Vertex tracking pixel detectors at SLHC aim to provide higher spatial resolution using less material but still maintaining the track finding properties of the existing detectors while dealing with an order of magnitude increase in particle track density. Monolithic Active Pixel devices have been proposed as a possible solution but it remains an extreme technical challenge to maintain a sufficient separation of noise, threshold and signal to allow for clean and in-time hit detection. Not only is the peak of the Landau distribution in the order of a few hundred electrons in such devices but charge collection time is often longer than the foreseen SLHC bunch crossing interval of 25 ns. Here we examine the possibility of using a 50 µm thick hybrid pixel sensor combined with the new architecture.

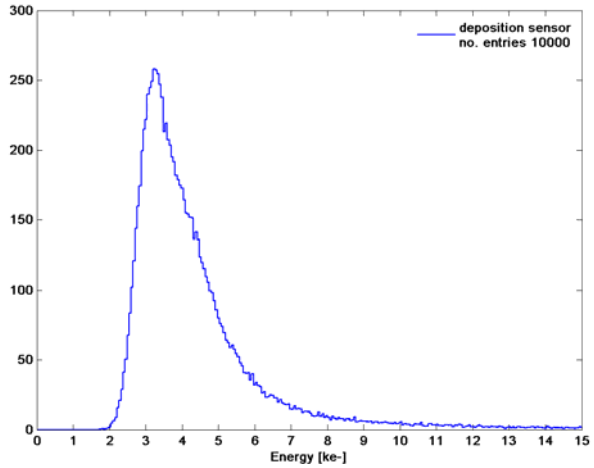

Figure 2: The spectrum of deposited charge in a 50 µm thick Si sensor.

Charge deposition simulations were performed using PENELOPE [6] illuminating the surface of a 50 µm thick silicon sensor uniformly with 10 000 perpendicularly impinging 20 GeV electrons (to simulate MIP's). PENELOPE fully reproduces charge deposition in the sensor. The charges deposited in each cubic micron of the material are assigned a random diffusion induced lateral offset with an rms of sqrt(2 D t_drift). The input signal at the collecting electrode is the sum of all of those charges delayed by the respective drift times. This is an adequate approximation to the incoming charge signal provided the total collection time is significantly smaller than the electronic shaping time. The collected signal is fed in turn to a circuit simulator.

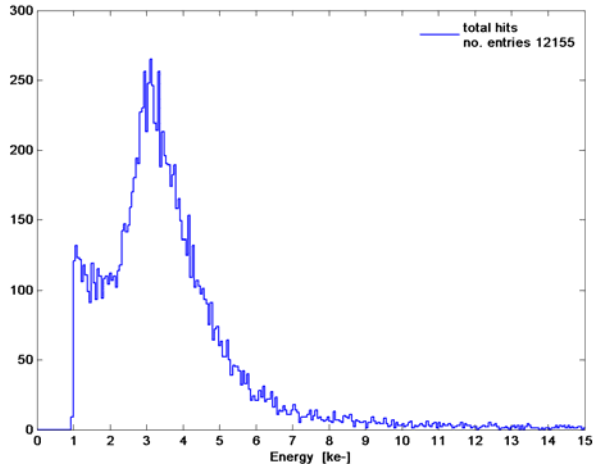

Figure 3: The spectrum at the output of a 50 µm thick hybrid Si pixel readout channel with dimensions 20 µm x 150 µm, equivalent input noise of 100 e^- rms and shaping time of 25 ns. Note that the simulation cuts off at a threshold of 1 000 e^-.

Figure 2 shows the spectrum of deposited charge for a 50 µm thick unsegmented Si sensor. The figure shows the expected Landau distribution with a most probable peak of around 3 500 e^- and a minimum deposited charge of ~ 2 000 e^- The silicon sensor was then subdivided into pixels with dimensions of 20 µm x 150 µm and connected to a readout channel with an equivalent input noise of 100 e^- rms and a shaping time of 25 ns. The results are shown in figure 3. Note that the simulator cuts off all hits below 1 000 e^-. It is clearly

difficult to determine the exact position of the threshold which will provide full detection efficiency and optimum spatial resolution while keeping sufficiently far from noise for track finding purposes. As can be seen from the number of entries in the plot there are only ~ 20 % of events producing more than one hit at a threshold of 1 000 e^-. However, if one now simulates the same data set applying the new architecture to the detection process (figure 4) the situation becomes quite different. It is fairly evident that applying a threshold of between 1000 e^- and 1500 e^- will result in full detection efficiency while maintaining a good separation between signal and noise. (One can see from the number of entries that there are 8 noise hits only at a threshold of 1000 e^-.) Although the summing circuit results in a noise figure of double the single channel noise, the threshold can be kept at least 5 sigma higher while still having full detection efficiency. Moreover, there are no or very few hits just above the threshold; this mitigates timewalk issues. An obvious extension of this concept is to use the charge summing decision to 'freeze' the analog contents of the 4 pixels which contributed to the hit providing simultaneously clean, in-time hit detection along with optimum spatial resolution.

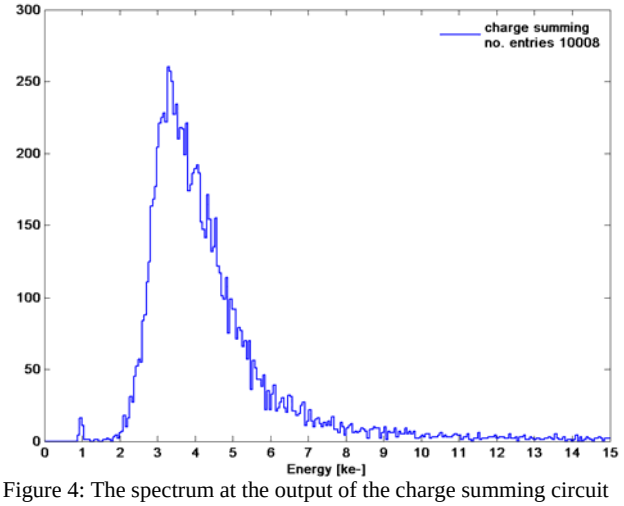

Figure 4: The spectrum at the output of the charge summing circuit

IV. Design Study for SLHC

The existing Medipix3 prototype chip was designed in a 130 nm CMOS process with a front-end rise time of 25 ns and a shaping time of 100 ns. We carried out a design feasibility study using the same process parameters to understand if the same concept could be applied to an SLHC detector with 25 ns shaping time while maintaining a reasonable power budget.

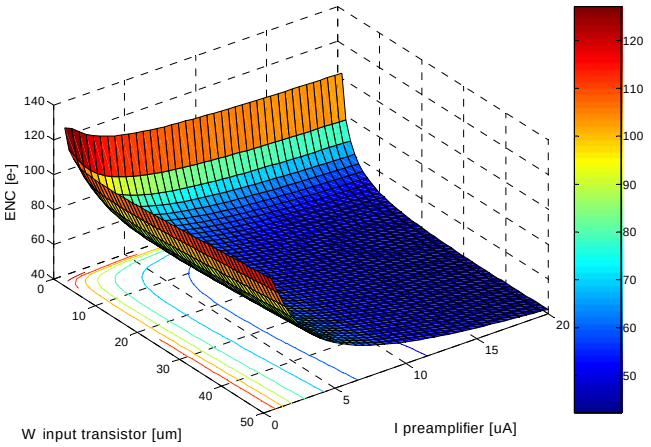

Figure 5: Simulated noise for a differential front end amplifier versus input transistor width, W, and total drain current, $I_{preamplifier}$.

A power budget of 1 W/cm^2 was assumed for pixels of 20 µm x 150 µm (roughly the same area as the 55 µm x 55 µm pixels of Medipix3) with a (pessimistic) estimate of the input capacitance of 80 fF. If the power supply is 1.5 V and ½ of the power is dedicated to digital circuitry, then there is 10 µA per pixel remaining for the analog front-end. It was further assumed that each differential front-end can have ~ 100 e^- rms noise, implying ~ 200 e^- rms at the output of the summing circuit (the quadratic sum of 4 uncorrelated front-end amplifiers). The simulations of noise versus input transistor width, W, and total preamplifier drain bias current, $I_{preamplifier}$, of the input transistor pair are shown in figure 5. For a W of 10 µm and an $I_{preamplifier}$ of 2 µA the noise is ~ 90 e^- rms.

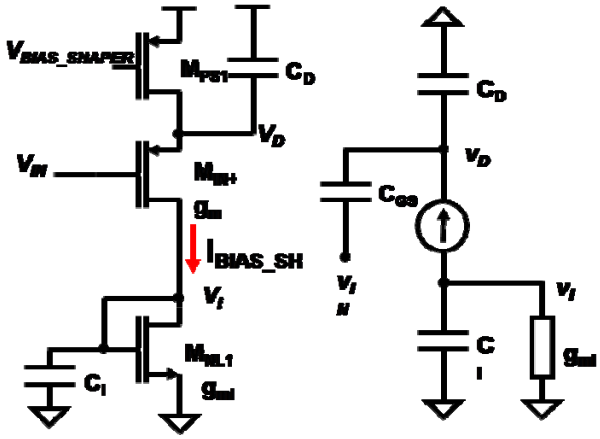

Figure 6: Schematic diagram of the single sided version of the shaper input branch and its small signal equivalent circuit (right).

This leaves 8 µA for the shaper circuitry. As the shaper circuit is also differential and provides 4 copies of its current to the summing nodes, 0.8 µA is available per branch. Figure 6 shows the schematic of the single ended equivalent of the shaper input branch along with its small signal equivalent circuit. Note that the output branches of the shaper are provided by transistors which mirror the current in M_{NL1}. Based on the available power budget it is possible to achieve reasonable sizes for the input and mirror transistors (W/L =

11/0.12 and 1/7.7 respectively) as well as for the coupling capacitor, C_d (~300fF).

V. Conclusions

We have described how the Medipix3 architecture can be applied to tracking at vertex detectors for the SLHC. Using this architecture one trades off a doubling of front-end noise against the possibility to place a threshold which is well separated from the front-end noise and the incoming signal spectrum even for very highly segmented and thin sensors. This in turn avoids having to deal with hits just above the threshold which would be shifted in time to subsequent bunch crossings. The system provides clean and in-time hit information helping to solve pattern recognition at SLHC Furthermore, the decision of the presence of a hit from the summing circuit could be used to 'freeze' the contents of the pixels contributing to the hit to enable sub pixel spatial resolution.

VI. References

[1] http///www.cern.ch/medipix

[2] X. Llopart, "Design and Characterization of 64K Pixels Chips Working in Single Photon Processing Mode," *Sundsvall : Mid Sweden Univ. : 2007, CERN-THESIS-2007-062.*

[3] R. Ballabriga, et al., "The Medipix3 Prototype, a Pixel Readout Chip Working in Single Photon Counting Mode with Improved Spectrometric Performance," *IEEE Trans. Nucl. Sci., Vol. 54, No. 5, October 2007.*

[4] D. Elia et al., "Performance of ALICE silicon pixel detector prototypes in high energy beam," *Nucl Instr and Meth. A: Vol 565, Issue 1, 1 September 2006, Pages 30-35.*

[5] F. Krummenacher, "Pixel Detectors with Local Intelligence: an IC Designer Point of View," *Nucl. Instr. and Meth. A: Vol 305, 1991, pp.527-532.*

[6] J. Baró et al., "PENELOPE: An algorithm for Monte Carlo simulation of the penetration and energy loss of electrons and positrons in matter," *Nucl. Instr. and Meth B: Volume 100, Issue 1, 1 May 1995, Pages 31-46.*

VII. Acknowledgements

The authors gratefully acknowledge the help and support of our colleagues in the Medipix2 and Medipix3 Collaborations.