A circuit topology suitable for the readout of ultra thin pixel detectors at SLHC and elsewhere

Wednesday, 5 September 2007 17:35 (25 minutes)

Hybrid pixel detectors provide unrivalled pattern recognition capabilities at LHC vertex detectors. Further reducing the material budget is of crucial importance among the many challenges which must be addressed by the vertex systems at SLHC. We propose a two stage front-end pixel readout architecture whereby the discrimination is performed on the sum of the total charge deposited in four neighbouring pixels prior to readout of the analog or binary hit information per pixel. In this way it may be possible to reduce the detector thickness from some 100um to 50um while maintaining a high separation of signal, threshold and noise.

Summary

Hybrid pixel detectors provide unrivalled pattern recognition capabilities at the LHC vertex detectors. Further reducing the material budget is of crucial importance among the many challenges which must be addressed by the vertex systems at the SLHC. On the detector side a compromise must be found between providing a sufficiently large and prompt signal to permit clean, in-time discrimination and minimising material. The task is complicated by the distortion of the MIP (Landau) spectrum by charge sharing between pixels - even if charge sharing contributes to enhanced spatial resolution. This issue is akin to the charge sharing which limits the spectral resolution of single photon counting systems.

Here we propose a two stage front-end readout architecture whereby the discrimination is performed on the sum of the total charge deposited in a number of pixels prior to readout of the analog or binary hit information per pixel. The architecture is very similar to that proposed for the Medipix3 development [1]. Each pixel provides four identical currents which are proportional to its input charge to summing circuits located at the pixel corners. Discriminators are connected to the output of each summing circuit. The discriminators communicate with each other event-by-event permitting only one pixel corner to claim a given hit. This implies that the discrimination is performed on the full MIP spectrum allowing the threshold to be placed at around ½ of the Landau peak - as opposed to between ¼ and 1/8th of the peak in existing systems. Although the front-end noise is effectively increased by a factor of 2 due to summing the uncorrelated contributions of 4 front-ends there is still a significant improvement in the separation of signal, threshold and noise. In this way it may be possible to reduce the detector thickness from a few 100 um to around 50 um while working with a threshold of 1 000 e- to 2 000 e-. The approach can be applied to planar or 3D sensors which, being only 50 um thick, are depleted easily even after high radiation doses. Moreover, the new system avoids hits occurring just above the threshold which would be wrongly allocated in time because of discriminator timewalk.

Further material budget reductions can be expected from thinning the readout wafer to an absolute minimum. Also the use of wafer bonding techniques together with deep via interconnect may simplify the mechanical construction of the detector avoiding bump bonding while at the same time allowing thin single chip tiles to be produced.

The paper will focus on simulations of the new circuit architecture using planar sensors and outline some technology options which may in future permit the construction of ultra thin pixel sensors.

[1] R. Ballabriga, M. Campbell, E. H. M. Heijne, X. Llopart, L. Tlustos, "The Medipix3 Prototype, a Pixel Readout Chip Working in Single Photon Counting Mode with Improved Spectrometric Performance," proceedings of Nuclear Science Symposium IEEE 2006, October 2006, San Diego, USA, published on CDROM

Primary author: Dr CAMPBELL, Michael (CERN)

Co-authors: Dr HEIJNE, Erik (CERN); Dr TLUSTOS, Lukas (CERN); Mr BALLABRIGA, Rafael (CERN); Ms WONG, Winnie (CERN); Mr LLOPART, Xavier (CERN)

Presenter: Dr CAMPBELL, Michael (CERN)

Session Classification: Parallel session B6 - ASICs 3 future