Microelectronics User's Group @ TWEPP 2007, Prague

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Agenda

- Status of Design Tools (slides from Kostas)
- MPW pricing and Plans

News

- 130 (CMOS and BiCMOS) and 90 nm contract available since 6/2007
- Design Kit for digital and mixed-signal ready for distribution
  - Already installed in 5 Labs + CERN
- Level of demand still below threshold for CERN-organized MPW

Status Of Digital Design Kit

Distribution of Digital Tools
for CMOS 130nm process

K Kloukinas / PH-ESE-ME

Introduction

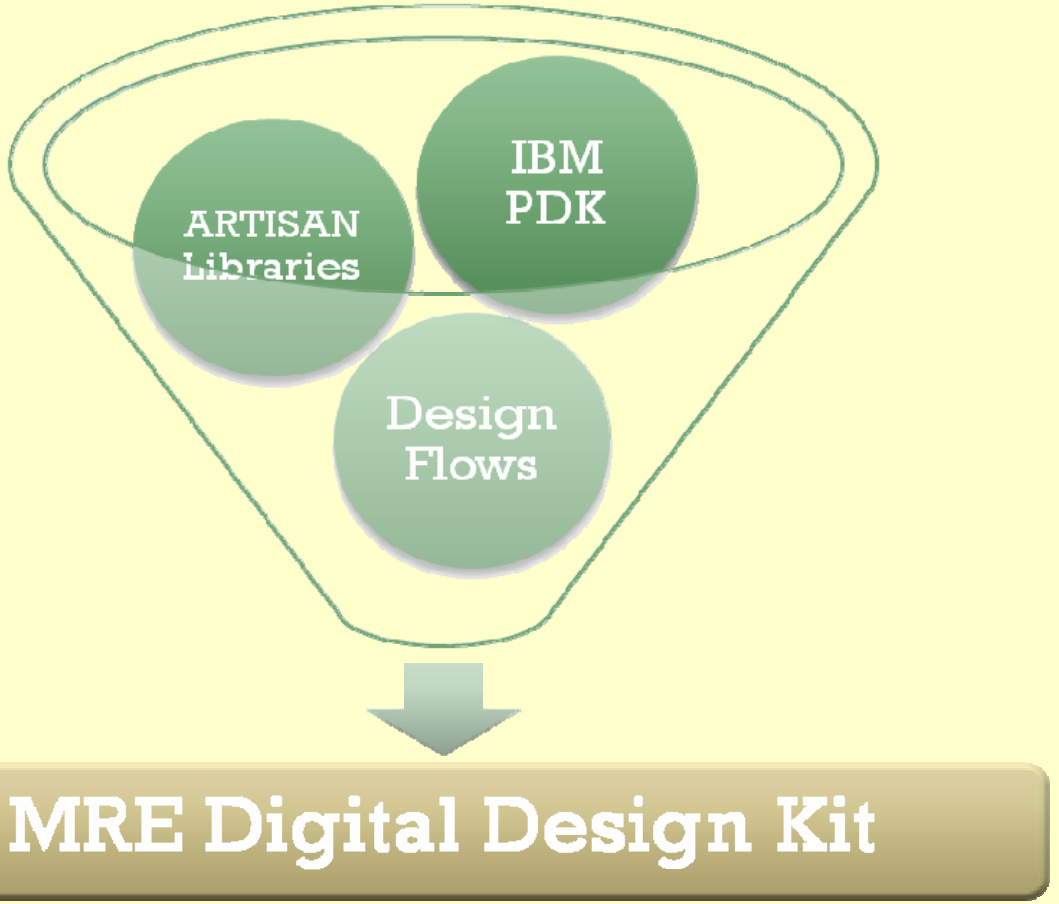
- The Digital Design Kit
- Development Status
- Distribution & User Support

Digital IC Design Project

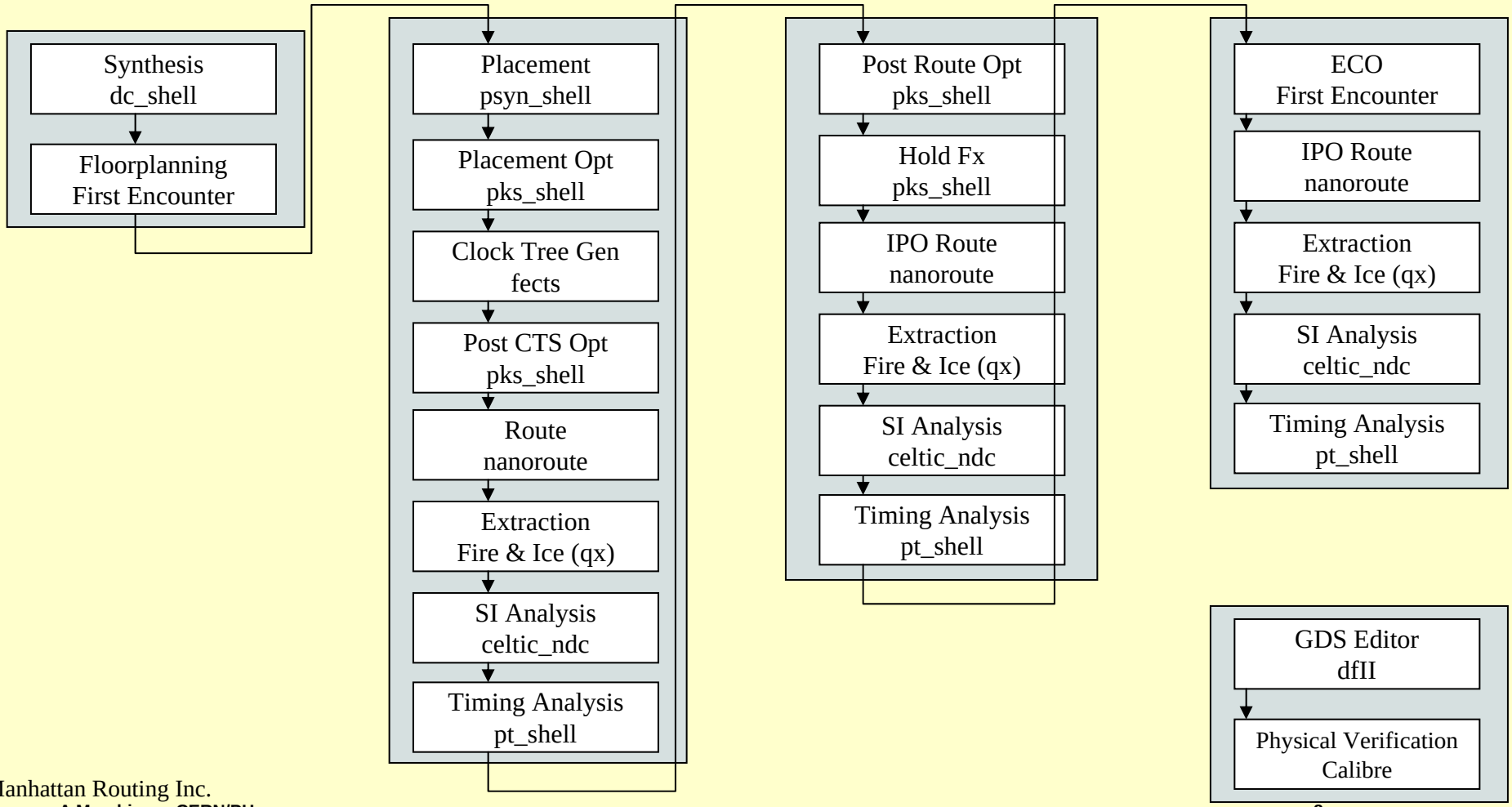
Rationalize the Digital Design Flow in our work environment.

Provide a common platform for design tools.

The Digital Design Kit



The MRE PnR flow in Detail



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CAE Design Tools

Design Tools Required for the Digital Design Kit V1.3

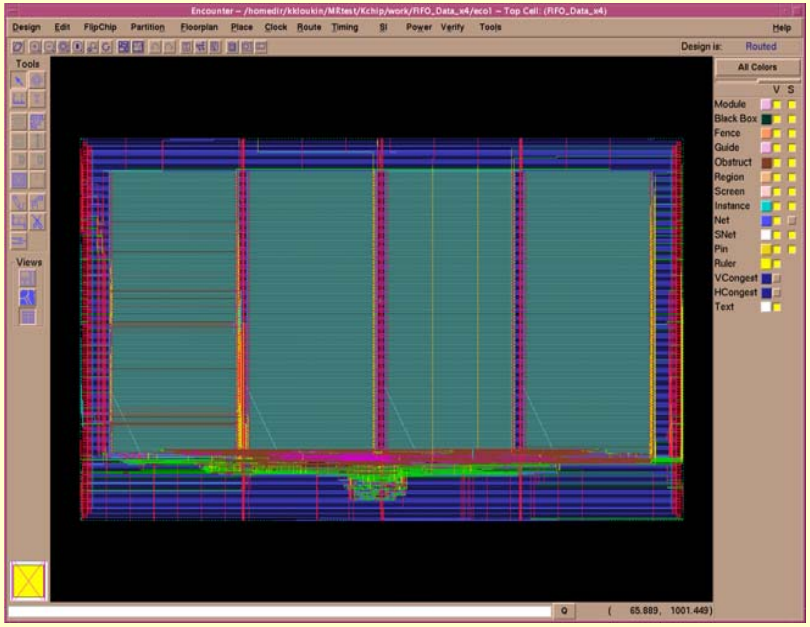
Tool	Version
CADENCE DFII	IC5.1.4.1
First Encounter	4.1.USR5
Fire & Ice	SEV_3.2
Prime Time	X-2005.12-SP2
CeltIC	TSI42_USR1
Calibre	2004.3_9
Synopsys DC, PC	2004.6.SP1
CADENCE Incisive Simulator	IUS_5.7

Status of the Digital Design Kit

- 1st release is Ready.
- Version: V1.3
  - Includes:
    - » ARTISAN package, with 6 & 8 metal layer DFII std. cells and IO libraries.
    - » IBM PDK V1.3.1.0, with patch file for V1.3.1.3. Build for IBM CMOS8SF/SFG process.
    - » MRE PnR flow scripts
    - » IO cells can be automatically placed
    - » Can LVS and DRC the IO cells

Design Kit validation

- Two Designs used as test benches:



- CCU25
  - Core logic P&R O.K.
- Preshower Kchip
  - Third party IP core integration (DP SRAM).
  - FIFO controller P&R O.K.
  - Work in progress for full chip implementation.

Digital Simulation

- The MRE Design Kit does not include a simulator tool.
- Recommended tool:
  SimVision for CADENCE Incisive Unified Simulator v 5.7
  - Functional
  - Post Synthesis (*parasitic extraction file from Design Kit*)
  - Post Layout (*parasitic extraction file from Design Kit*)

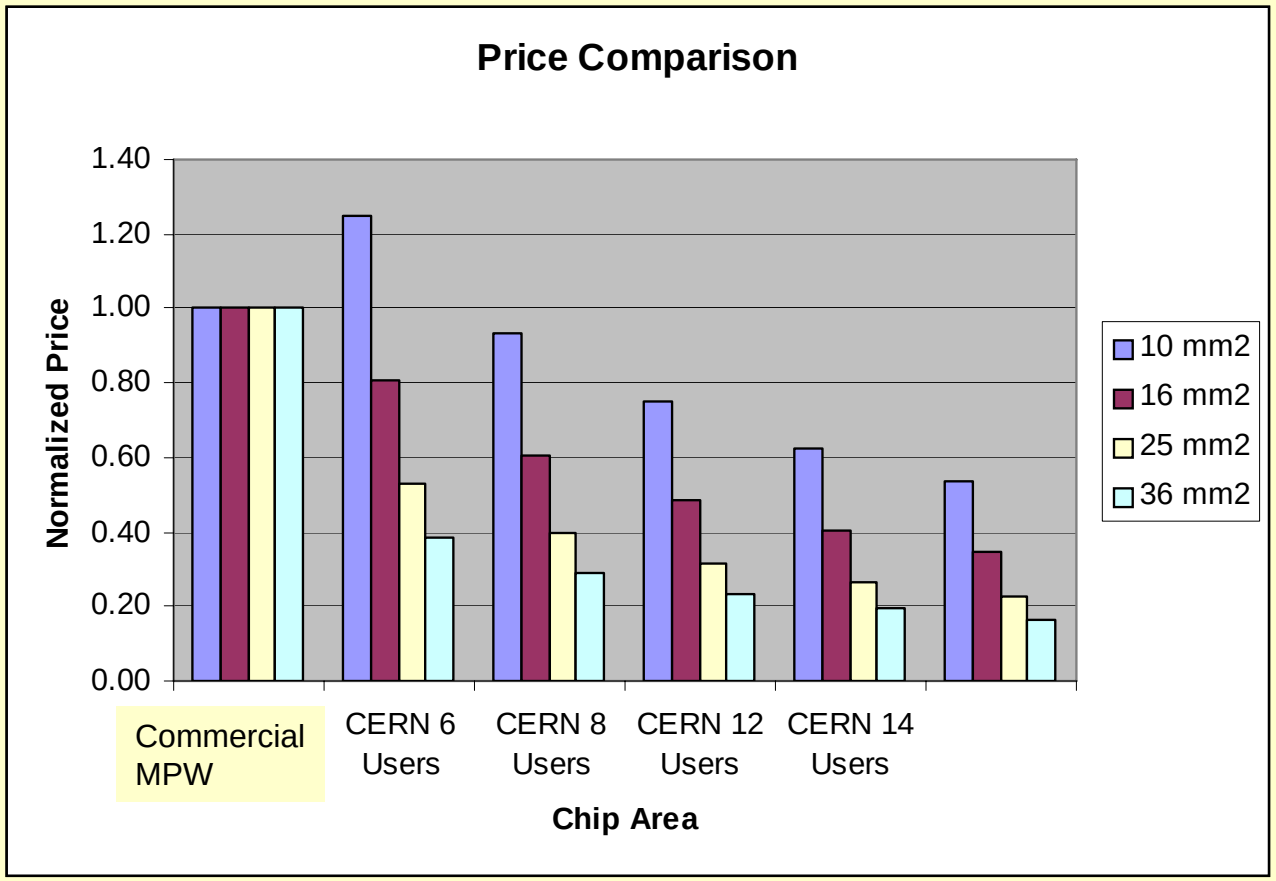
Future Plans

- Flow scripts modifications to permit users to skip selected steps (for instance no automatic scan-path) in the design flow.
- Enhance documentation material.
- Next Training Course: Late November/early December
  If interested please send email to Alessandro.Marchioro@cern.ch

Design Kit Distribution

- Acquiring the Digital Design Kit:
  - Contact Bert.Van.Koningsveld@cern.ch or Kostas.Kloukinas@cern.ch
  - Acquire commercial license from MRE
  - You will be given an account on CERN's LXPLUS.
  - You will be able to "sftp" the Design Kit.
- Users Support
  - Limited to the distributed Design Kit version, running under the supported versions of the CAE design tools.
  - Distribution of:
    - » Design Flow patches for bug fixes.
    - » Technology file updates for DRC verification.
    - » Updates to accommodate for foundry and IP vendor newer releases as well as CAE tools upgrades.
  - SUN SOLARIS platform only will be supported (no Linux, sorry!).

MPW-Pricing


Price Comparison
Normalized Price
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
10 mm2
16 mm2
25 mm2
36 mm2
Commercial MPW
CERN 6 Users
CERN 8 Users
CERN 12 Users
CERN 14 Users
Chip Area

130 nm MPW run details

- CMOS8-RF process including:
  - poly and diff resistors
  - triple well
  - Low-Vt N and PMOS
  - Zero-Vt NMOS
  - e-fuses
  - Thick (5.2 nm) transistors for IO @ 2.5 V
- 6 metals with LM upper stack, all Cu
  - Vertical metal to metal cap: 1.3 fF/um^2
  - 8 metals possible for private runs (+ 70K$)
- C4 bonding if desired (run split possible)
- Hundreds (or thousands!) of chips from proto run
- Preferred chips sizes: multiple of 2x2 mm^2
- Cost below MOSIS at about 70-80 mm^2.

Future runs

- 130 nm:
  - 1 small MPW run in February 2007
  - If enough users, CERN-MPW?
- ¼ micron
  - 1Atlas run

Spare slides

Standard Flow Stages

- Synthesis
  Converting RTL to gate level Verilog
- Placement
  Assignment of a physical location to each standard cell in the design
- CTS – Clock Tree Synthesis
  "The physical realization of the clock tree network constrains the chip design, and it directly impacts the control of clock skew and jitter. Further, the clock network impacts overall chip power and area because of the large number of buffers and repeaters that are inserted."
- SI – Signal Integrity
  "Unwanted noise that may wreck a design. Power grid noise, crosstalk among various types of signals and electro-migration can result in anything from lower time-to-failure to a design that is impossible to converge. Signal integrity issues can limit yield and profits, and generally involve trading off issues dealing with the following areas: some kind of performance (speed, power or area); yield or reliability; and design productivity.
- DFM – Design For Manufacturability
- STA – Static Timing Analysis
  Static timing analysis uses fixed delays for gates and wires derived from best-case, worst-case and nominal parameter sets constructed using Spice simulation. Static timing analysis takes in netlists, assertions, delays and slew models, and produces reports on slack and diagnostics.
- DRC/LVS/Antenna Verification
- Formal (LEQ) Verification
  Compares original RTL netlist against physically optimized netlist to verify they are logically equivalent

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Tools Used in Standard Flows

- Design Compiler - dc - dc_shell -tcl
  - Used to convert functional RTL to gates using WLM to size output drivers
- Physical Compiler - pc - psyn_shell
  - Can synthesize RTL and perform placement simultaneously using steiner routes to estimate parasitics instead of WLM.
  - Can perform placement of gate level netlist
  - Can perform placement based optimization
- First Encounter - fe - encounter
  - Used for prototyping digital designs, producing physical information for optimizing logic, complete power-grid realization, and hierarchical controls for partitioning and budgeting, and hierarchical clock tree synthesis.
- Physically Knowledgeable Synthesis - pks - pks_shell
  - Optimizes the critical paths, taking congestion information into account, and uses true global routing to determine interconnect timing.

Tools Used in Standard Flows

- Nanoroute
  - All-purpose router for top-level and block-level routing
- Qx/Fire & Ice - qx
  - 2.5D extractor based on validated tech files available from major foundries. Outputs RCs in DSPF/SPEF format for timing, signal integrity, power, and reliability sign-off verification
- Celtic
  - SI-aware delay calculator that provides a unified timing solution that accurately accounts for the impact of crosstalk and IR drop on both delay and functionality. CeltIC NDC combines crosstalk analysis from CeltIC signal-integrity analyzer with the delay calculation capabilities of SignalStorm® NDC. Celtic NDC can be used to complement both Cadence and non-Cadence static-timing analysis and place-and-route flows.
- PrimeTime - pt - pt_shell
  - Full-chip, gate-level static timing analysis tool optimized to analyze millions of gates in a short time, allowing multiple analysis runs in a single day
- Calibre
  - Industry standard physical verification tools. DRC/LVS

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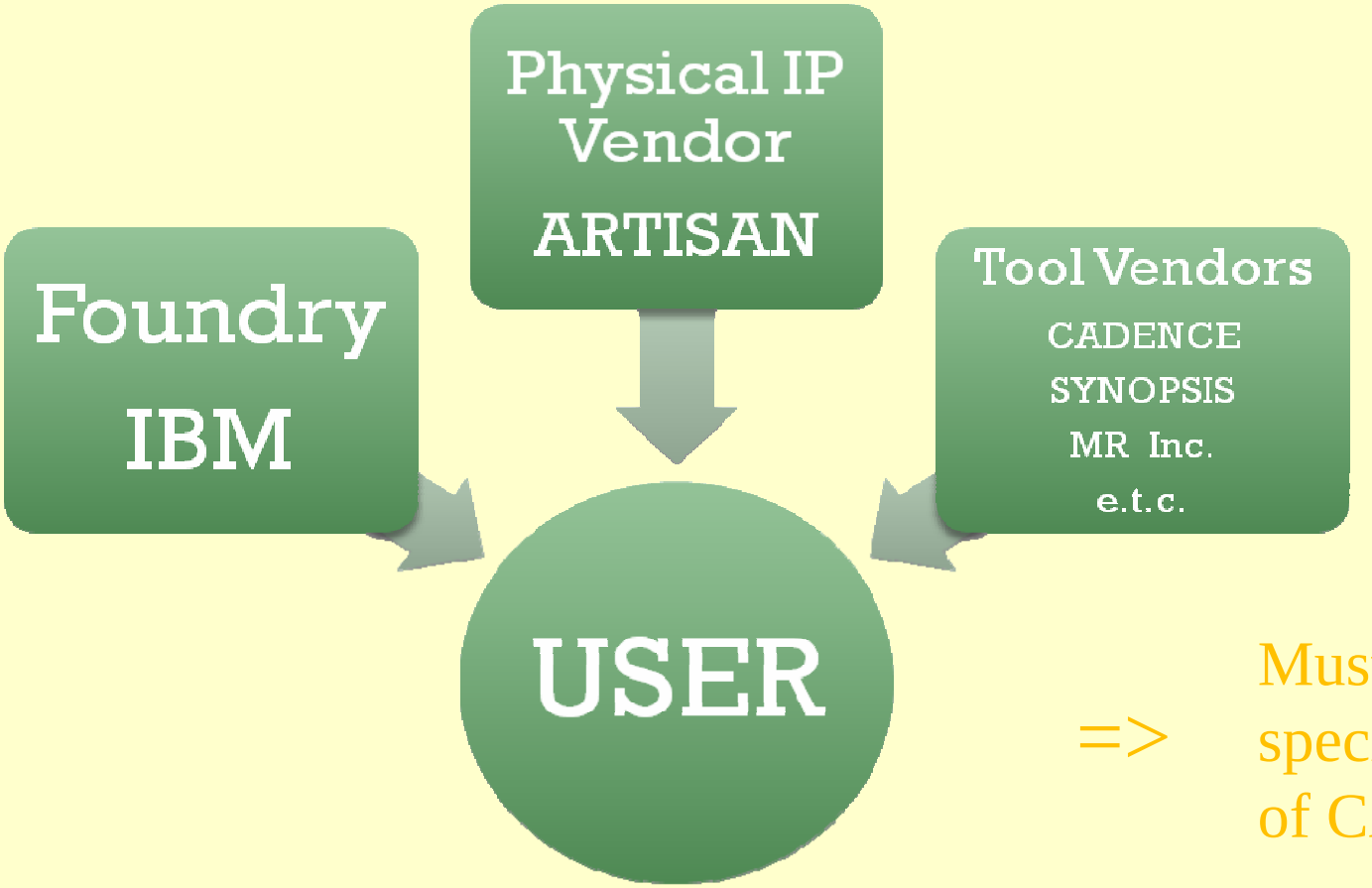
The User's point of view !



=> Must adhere to specific versions of CAE tools.