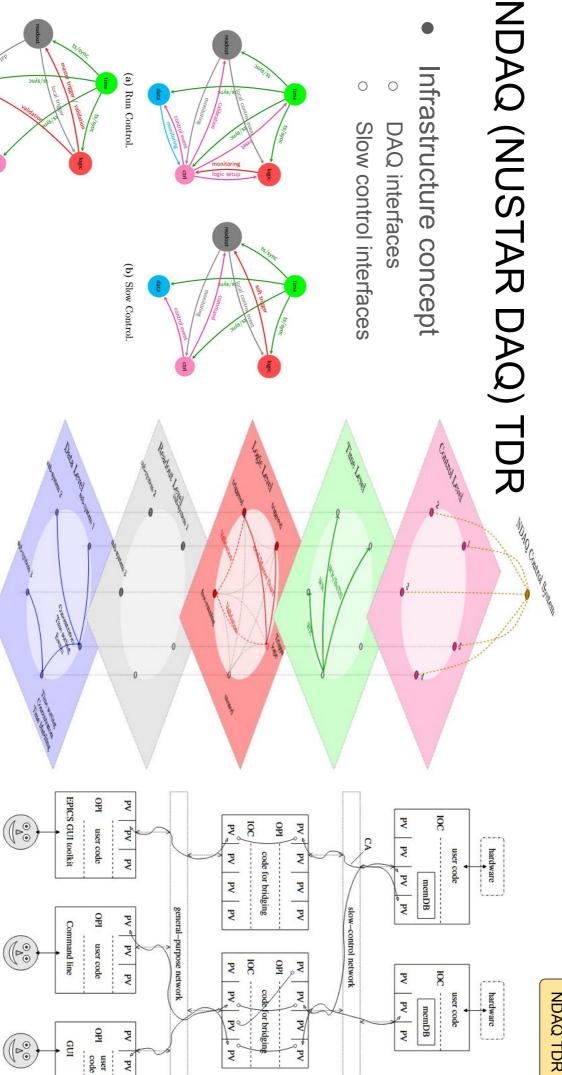
NUSTAR DAQ and slow control developments at GSI/FAIR

Mostly R3B and FRS...

Hans Törnqvist, Chalmers University of Technology
On behalf of the NUSTAR collaboration

NDAQ TDR

- Infrastructure concept



https://fair-center.de/user/experiments/nustar/documents/technical-design-reports

GUI

code

B. Löher, R3B collab. meet. 2020

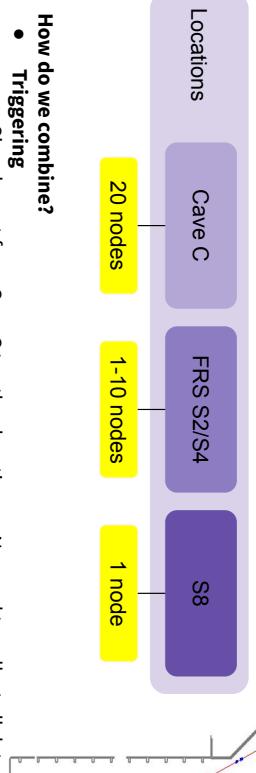
FRS

S2/S4

FOCUS

FR

Locations



ESR

DIRECT

TRANSFER

LINE

SS 8

- Signals sent from Cave C to other locations → No need to collect all data at S2

Event synchronisation with timestamps

- White Rabbit time is used everywhere (NEW: Now also available at S8)
- **High resolution Time-of-Flight**
- Derive phase-stable clock from White Rabbit or BuTiS → 30 ps jitter
- **Experiment data**
- **Central Timesorting**

Who are the users?

- R3B
- FRS (FRS detectors)
- Gamma spectroscopy (FRS detectors)

B. Löher, R3B collab. meet. 2020

Common infrastructure

Common Trigger Clock Time

Pulser

What's provided?

- Trigger and master start signal distribution from Cave C
- 200 MHz phase-stable synchronised clock in each location
- Connection to White Rabbit network in each location
- Logic pulser distribution from Cave C
- Analog signal simulator in Cave C, with recorded spill pattern (including micro spill structure)

How do we know it works?

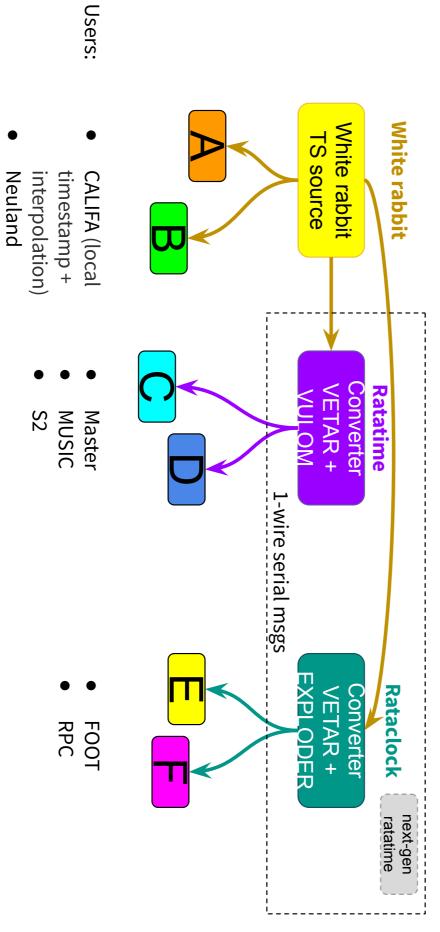
- Check clock synchronisation via coarse counter tracking (ucesb: unpacking and event-data processing tool)
- Check timestamp correlation in the time sorter, displayed in tree view (drasi)





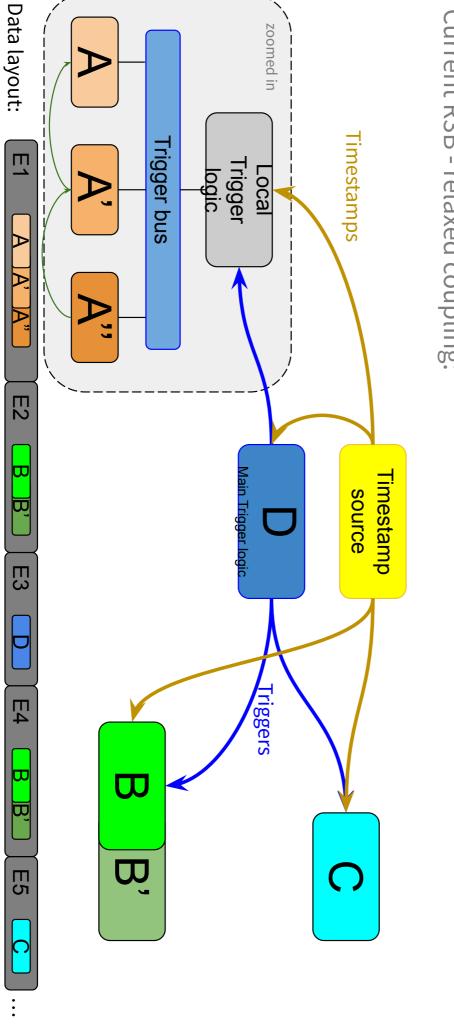
High precision timestamp distribution system

1 ns granularity timestamps across GSI



Event synchronisation – Time distribution

Current R3B - relaxed coupling:



Timesort & Store

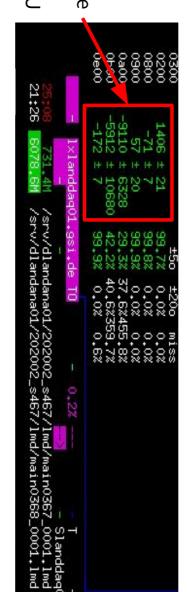
Store Timesort &

timesorter drasi

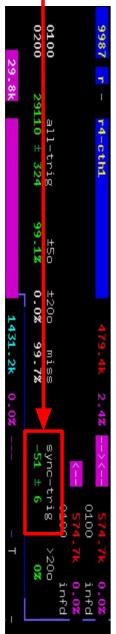
LMD format

What's in the drasi timesorter?

- time, will not halt the TS Timesorter sources can come and go at any
- to a reference Timestamp differences / distribution relative
- Time tracking per system, correlation to CPU
- time in tree view Report offset of local clock to NTP
- 0 Check WR timestamps for monotonic increase and alignment with local CPU clock scale
- down to +- 5 ns (currently trigger 7) correlation and delay without beam Additional time sync trigger to check



Alert user on error!



B. Löher, R3B collab. meet. 2020

Electronics

Electronics VFTX

Mesytec

TAMEX

FEBEX

:

1/1

Who uses what, and why?			7
GSI FEBEX3	CALIFA, X5 PSP	digital processing / PID	70
GSI FQT + TAMEX3	NeuLAND, R3B ToF wall, LOS	high time res, density, ToT	
MCFD + GSI TAMEX2	ToF wall tests	high time resolution, ToT	
GSI PaDi + Clock-TDC	SiPM fiber, drift chambers	high channel density	
GSI PaDi + KILOM	Fiber detectors	highest integration & density	
GSI VULOM	ROLU, SEETRAM, ionisation chamber, TRLO II	low cost	
Mesytec VMMR8	Sofia MWPC	custom front-end, high density	
Mesytec MDPP16	Sofia Twin/Triple MUSIC, R3B MUSIC	digital processing	
GSI VFTX	S2, S8, Sofia START, Sofia ToF wall, LOS	highest time resolution	
GSI SIDEREM + SAM	AMS (alternative: INFN DAQ)	hardware constraint	VMT ×
			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

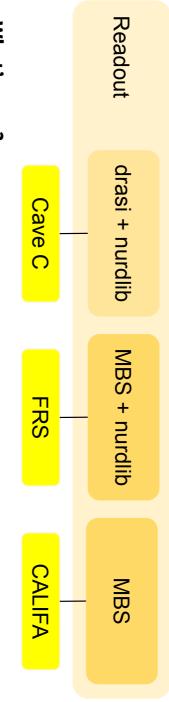
Electronics

Electronics VFTX Mesytec **TAMEX FEBEX** :

	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \				
0	VMT o	onstraint	hardware constraint	AMS (alternative: INFN DAQ)	GSI SIDEREM + SAM
		e resolution		• Attibe - Mooric - Spin pixel, lested at Chivia How	GSI VFTX
		essing	but	 FOOT – ADC-board + DE10 – microstrip charge readout 	Mesytec MDPP16
		nt-end, high density			Mesytec VMMR8
				 GSI TRB3 – RPC – high time res, density, ToT 	GSI VULOM
		highest integration & density	hiahest inte	Fiber detectors	GSI PaDi + KILOM
		iel density	high channel density	SiPM fiber, drift chambers	GSI PaDi + Clock-TDC
		high time resolution, ToT	high time re	ToF wall tests	MCFD + GSI TAMEX2
		high time res, density, ToT	high time re	NeuLAND, R3B ToF wall, LOS	GSI FQT + TAMEX3
	7	digital processing / PID	digital proce	CALIFA, X5 PSP	GSI FEBEX3
	D)			ind why?	Who uses what, and why?

B. Löher, R3B collab. meet. 2020

Readout



What's new?

- Rimfaxe VME controller / trigger logic hybrid (Aarhus contribution)
- First two prototypes at GSI, testing is ongoing
- Single-cycle access up to 2x faster than RIO4
- Native integration of TRLO II
- Sequencing logic work in progress (Håkan) I/O onboard: 24 ECL + 4 LEMO
- I/O with expansion: additional 96 (ECL and/or LEMO, TTL or NIM)
- RIO4 is reaching end of life (can not be purchased)







DAQ – readout library nurdlib

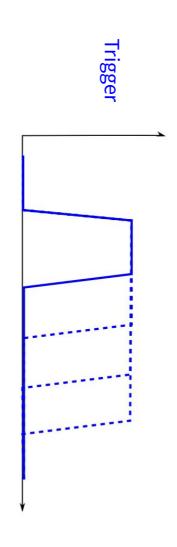
- 2014 January: copy-paste templates and scattered libraries
- 2014 April: nurdlib (NUstar ReaDout LIBrary) collected all readout into one library
- Initially named vmelib, but VME only goes so far...
- weird readout modes, in one place Collects all support, all experiences, all tests, all fixes, all
- Has seen several core overhauls to support growing feature list, but rather stable in the last few years
- Documentation and examples...

```
CRATE ("LOS ROLU") {
                                                                                                                                                                                                                                                                                                                                                                                                      #log_level = debug
                                                                                                                                                                                                                                                                                                                                                                                                                              .and@lxir123:r41-56 > cat main.cfg
                                                                                                                       BARRIER
                                                                   GSI_VULOM(0x03000000) {
                                                                                             TAGS ("1", "3", "10", "11", "12", "13")
                                                                                                                                                                                                                                                                                 GSI_VFTX2(16, 0x04000000) {
                                                                                                                                                                                                                                                                                                                                                          deadtime release = true
                                                                                                                                                                                                                                                                                                           # SMA connectors
                                                                                                                                                                                                                                                                                                                                    TAGS ("1")
                                                                                                                                                                                                                                                                GATE (
                                                ec1 = (0..7, 12..15)
                           pulser = (3)
input_coinc = (0)
                                                                                                                                                                  clock_input = external
                                                                                                                                                                                                                                    time_after_trigger =
                                                                                                                                                                                                                   width = 4.5 us
```

```
#log level = verbose
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        land@lxir123:202205_s509 > cat x861-101/main.cfg
                                                                                                                                                                                                                                                                                                                                                                                                        TAGS ("1", "3")
                                                                                                                                                                                                                                                                                                                                                                                                                                                                             GSI_PEX() {
                                                                                                                                                                                                                                                                                                                                                            GSI_TAMEX(0, TAMEX3) {
                                                                                                                                                                                                                                                                                                                                                                                # (SFP=0..3, version=2|3)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     deadtime_release = true
                                          GSI_TAMEX_CARD(8)
                                                             GSI_TAMEX_CARD(7)
                                                                                                                                                      GSI_TAMEX_CARD(2)
GSI_TAMEX_CARD(3)
                                                                                                                                                                                                                        include "$EXP_PATH/nl_gate.cfg"
GSI_TAMEX_CARD(0) {}
                                                                                                                                                                                                                                                                   long_range = true
                                                                                                                                                                                                                                                                                                                     ref_ch0 = true
                                                                                                                                                                                                                                                                                                                                       data_reduction = true
                                                                                                                                                                                                                                                                                                                                                                                                                                                       include "$EXP_PATH/nl_pex.cfg"
GSI_TAMEX_CARD(10)
                    GSI_TAMEX_CARD(9)
                                                                                       GSI_TAMEX_CARD(6)
                                                                                                             GSI_TAMEX_CARD(5)
                                                                                                                                 GSI_TAMEX_CARD(4)
                                                                                                                                                                                                        GSI TAMEX CARD(1)
                                                                                                                                                                                                                                                                                               clock_input = backplane
```

Anti-event-mixing - Sync check signal

TRLO II generates trigger signal with known variable length

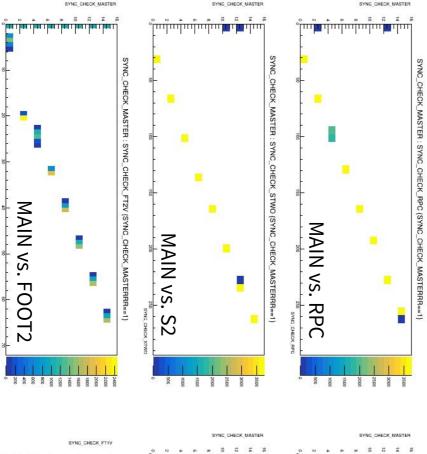


- Detectors measure length for every trigger and include in data stream
- Directly via front-end (TDC or TAC/ADC) <- nice for testing full electronics chain
- Via TRLO II <- if front-end does not support this
- User, DAQ and unpacker can analyse and check the measured values
- Measured values should agree between all systems for every trigger

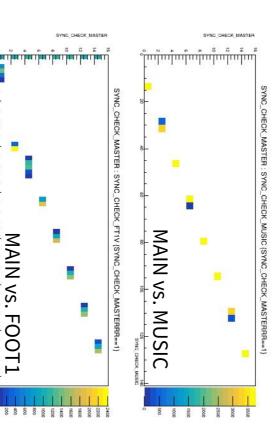
Trigger

Sync check signal plots

Correlations (online, nearline, offline)



SYNC_CHECK_FT1V: SYNC_CHECK_FT2V (SYNC_CHECK_MASTERRR==1)



FOOT1 vs. FOOT2

B. Löher, R3B collab. meet. 2022

Sync check signal analysis

DAQ monitoring (online):

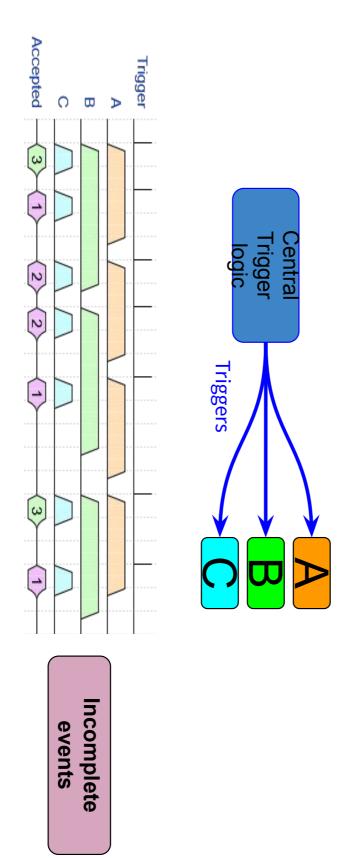
			(
10	Master	ncv	nrf	good	amb	bad	mis	spu	rel	#0
01	?			2815		-2	2785			13
02	S2	269		5327						60
03	RPC			5596						62
04	?			2815		L	-2783			13
06	?			2815		L	2785			13
07	?			2817		-1	2785			13
9	?			2815		1	2785			15
0a	CAL_M	101				_	5496			
Øb	CALW	101				1	5496			6
0 c	?			2815		-	2785			14
Ød	?			2815		-	2785			14
0e	Music			5596						32
0f	?			2815		-	2785			13
12	?			2817			2785			16
13	?			2815		-2	785			14
14	?			2815		1	2785			12
15	?			2815		1	2785			11

UCESB output (online, nearline, offline):

ocoref	ref	_	local	e	extra	1	nofit		ambig		mism	В
000	noaref	ref		spur		noval	ou:	outfit	1	noref		match
15												

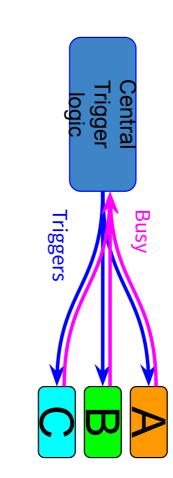
Live time (de)synchronisation

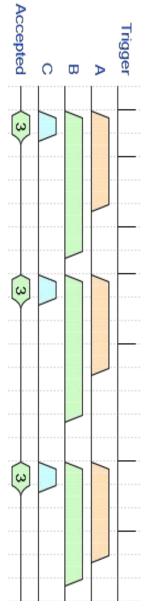
Unaligned local deadtimes leaves parts of the setup blind to certain triggers



Live time (de)synchronisation

Pay attention to busy signal of subsystems

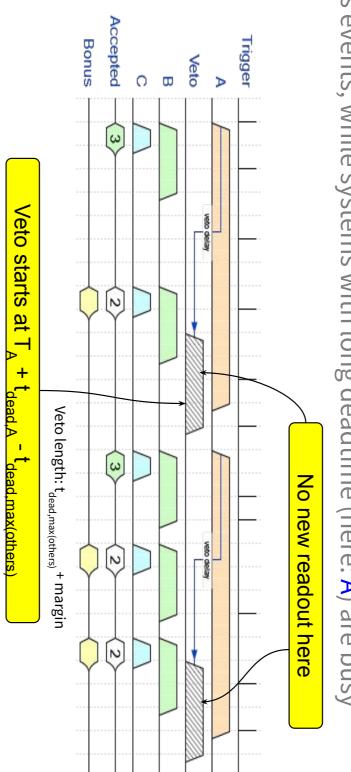




More complete events

Live time (de)synchronisation

Bonus events, while systems with long deadtime (here: A) are busy



DT and rate

- Full readout DT per system type:
- Master VME: 19 us
- LOS negligible
- Tamex 1-6 cards (TOFD): 21 us
- CTDC 4 cards (Fibers): 21-23 us
- Febex 16 cards (PSPXs): 43 us
- Tamex ~50 cards (NeuLAND): ~60 us

s444/s473 max uniform rate → 17 kHz

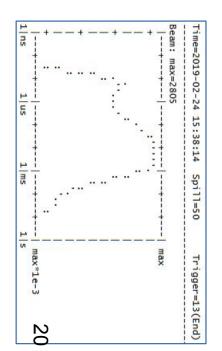
s454 max uniform rate → 43 kHz

General news

- DAQ scripts for many domains in parallel
- E.g. main + LOS + NeuLAND with all event builders on one host
- Structure ASCII-file based
- Nurdlib shadow readout
- Original implementation and investigations by M. Munch at Aarhus
- CAEN v775 32-ch -> 51.4 kHz
- Mesytec MDPP16 zero-suppressed -> 156 kHz
- With MBLT -> 220 kHz, the setup physically screams, also a bit unstable
- (Not useful for our current electronics, but imagine the things we could do...)
- Firmware updates
- Less data from TAMEX, slow control auto-thresholding on CTDC
- 200 MHz clock from BUTIS and White Rabbit

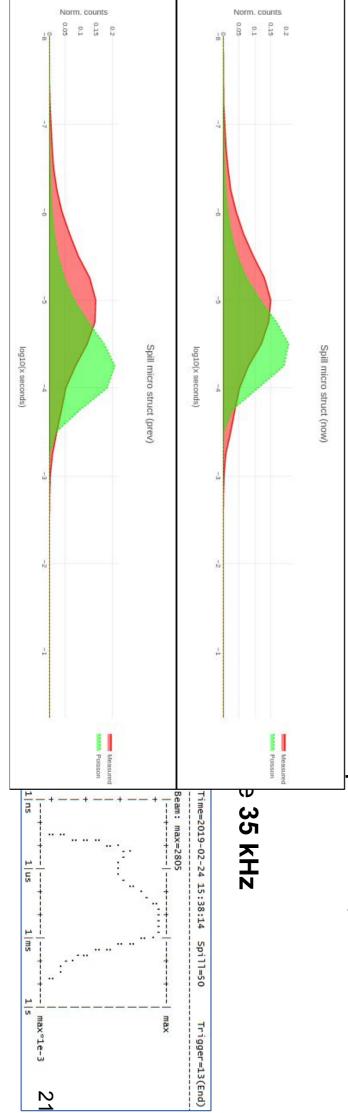
Beam micro-structure and dead-time (DT)

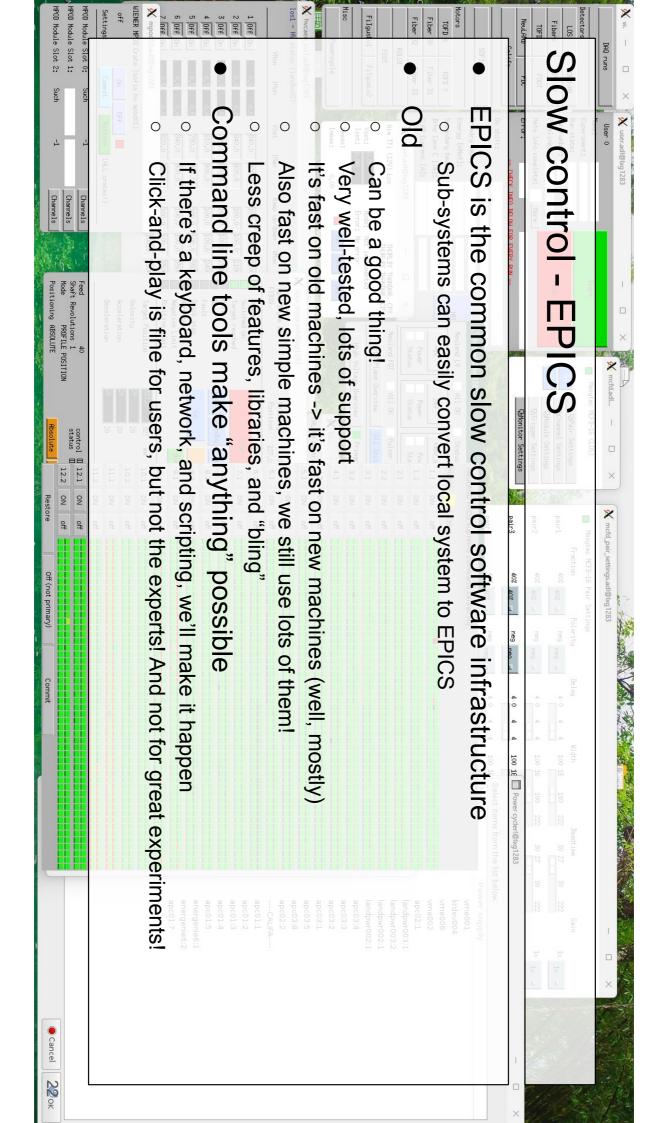
- apart → nearby particles lost during long DT Incoming particles distributed in tight bunches average 10-100 us
- TDC conversion <3 us, single event readout 20..60 us
- But cannot release DT with GOSIP until token trip finished, i.e. **∼17 us** dead (otherwise data garble)
- Considering s454-style DAQ:
- Under controlled unsafe conditions, 48 kHz, in real life 35 kHz
- VME headers and counters in DT (+misc) \rightarrow **8 us**, buffers read out off DT **~10 us**
- Use few modules to reduce in-DT readout, or more crates in parallel (Triva bus limits?)



Beam micro-structure and dead-time (DT)

- apart → nearby particles lost during long DT Incoming particles distributed in tight bunches average 10-100 us
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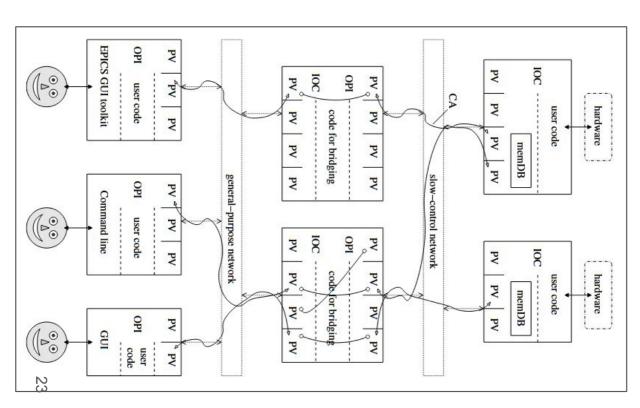


Slow control hierarchy

- IOC Input/Output controller
- Speaks with hardware/service
- Transforms to/from EPICS Process Variables (PV:s)
- Gateway
- Network and naming segmentation/isolation
- Access control
- Technical IOC names switched to logical human names
- As human as we can...

Archiving, snapshotting, restoring

- Log everything!
- Presentation and controls
 Graphical tools
- with backup hardware Network infrastructure + services built in cave C



Gateway

- Official gateway not quite enough
- R3B has >100,000 PV:s!

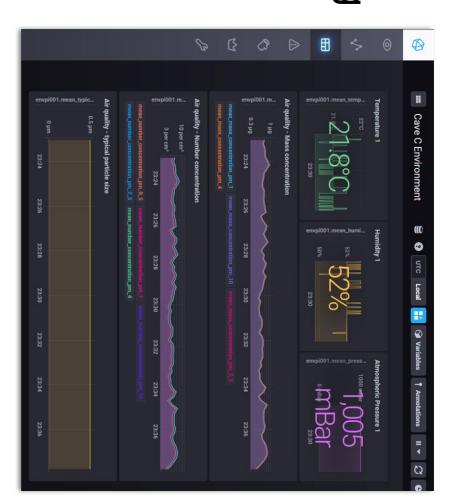
r3bcagw!

- Written from scratch with EPICS base PV comm libs
- No more regexps, every single PV directly aliased
- Move CPU from runtime to setup
- 0 "Splitter" chops and groups PV:s by prefix (host?) in separate gateway processes
- Lib/process caring about fewer nodes seems more stable?
- The ultimate tech power "Did you try turning it off and on again?"
- EPICS PV comm library not 100%
- Huge beast, let's leave it for now...



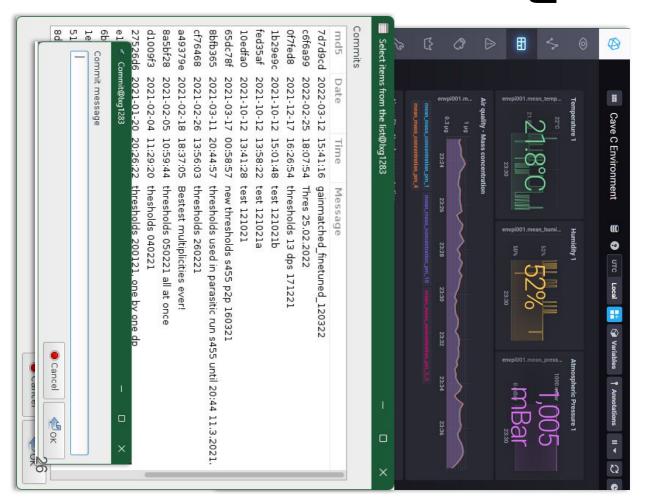
Archiving, snapshotting, restoring

- Archiving: store changes in fluxdb, visualised online with eg. Chronograf
- Snapshotting: record PV set values
- Mass "caget" invocations with stdout -> text file
- Text file add + commit to params git repo
- Can run anywhere
- Restoring: read and write PV set values
- git selection of file version
- Output is written with "caput"
- Slow, but unsafe fast writes not an option
- Need to implement "verified" fast writes



Archiving, snapshotting, restoring

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EPICS – Visualisation

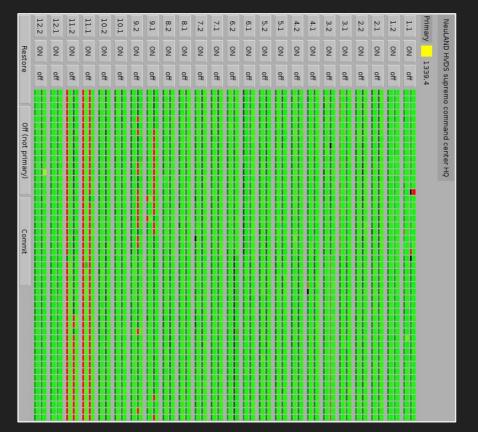
- Most detectors still manageable with eg MEDM
- Text-based file to setup GUI with controls and monitors
- NeuLAND currently has 2,600 channels
- General-purpose tools can not handle this!

r3bcavalcade!

- SDL-based renderer
- Much simplified version of MEDM, but expensive operations gone
- EPICS expression support
- Can handle NeuLAND many times over on a single host
- NeuLAND will eventually have 6,000 channels, don't get lazy!

Faster HV status display

- Problem: Neuland HV status display has lots (thousands!) of little lights
- Limitation: MEDM is not made for this and uses a lot of CPU
- Solution: Replace HV MEDM display with custom GUI based on efficient SDL library, actually a mini-MEDM with configurable layout
- Outcome: MEDM used 100% CPU on landgw01 r3bcavalcade < 10% CPU on lxg1290
- Side effect: More colors, more information, faster update rate possible, easier to add requested



Most of the red stuff is fine...

Bulk mapping – r3bmap

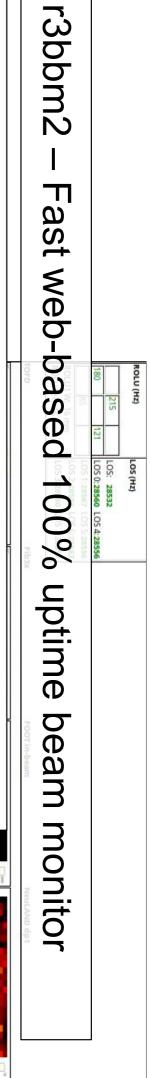
- Huge number of channels and crazy detector mappings
- NeuLAND 13x double planes, split among 13 TAMEX cards in different sequential chains on different DAQ PC:s, and 4 HV modules split between two HVDS system (with sub-chains...)
- Fibers Fiber swizzling, mask rotation, MAPMT rotation, for thousands of fibers
- Ever-changing host-names for LV supplies, motor controllers, failing raspberries etc

r3bmap!

- Scripts/programs that made life easier eventually collected
- One place to generate all mapping (unpacking, slow-control, GUI:s...) for all detectors, no need to hunt in someone's temp working dir
- git of course..
- Super pre-alpha and sheltered so far
- (General point, we need courses in computing hygiene)

Overkill: 1.17 Evaluation: 17% Transmission: 3.0e-7 rate: 21384Last update: Tue jul 13 2021 07:06:47 GMT+0200 (Central European Summer Time) Server status Connected ROLU2 W: 30 mm ROLU1 H: 30 mm ROLU1 W: 30 mm Beam quality R3B Beam Monitor (V2) ROLU2 H: 30 mm r3bbm2 - Fast web-based 100% uptime beam monitor 4605 13734 9582 55232 Last 113277 Last 120156950 19408 103 CIF-Or CIF-And TRLOII scalers (average over spill in counts per second) ROLU (Hz) euLAND OSIROLU nspill (Hz) 28066.3 615.3 2100.5 199.1 31771.7 51573.3 28787.5 50995.7 19.05.22, 04:58:14 Before LMU LOS 0: 28560 LOS 4: 28556 +Frag +P2P +P2Pv +OR 6171.9 5866.9 321.8 223.3 14766.9 13544.7 293.3 Before DT 200.4 4205.3 3967.5 73.7 289.3 5624.6 After DT 289.3 200.4 1051.5 991.8 73.7 Downscaled CIF-And Offspill Input CIf-Or VeuLAND 540.6 1447.1 14475.8 3508.6 19.05.22, 04:58:15 +ORV +Frag +P2P +P2Pv -Min Bias

Chill



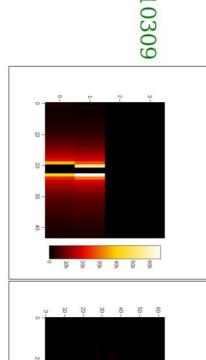
R3B Beam Monitor (V2)

Last update: Tue jul 13 2021 07:06:47 GMT+0200 (Central European Summer Time) Server status Connected

Beam quality

Overkill: 1.17 Evaluation: 17% Transmission: 3.0e-7 rate: 21384

19408 55232 10309 5354 Last 113277 Last 120156950 TOFD Fiber temperatures (threshold = 90 deg) 61.0 - 51.7 - 57.2 Fib23a/b



+Frag +P2P +P2Pv +OR

Before DT

Crill

ROLU2 W: 30 mm ROLU1 H: 30 mm ROLU1 W: 30 mm

4605

13734

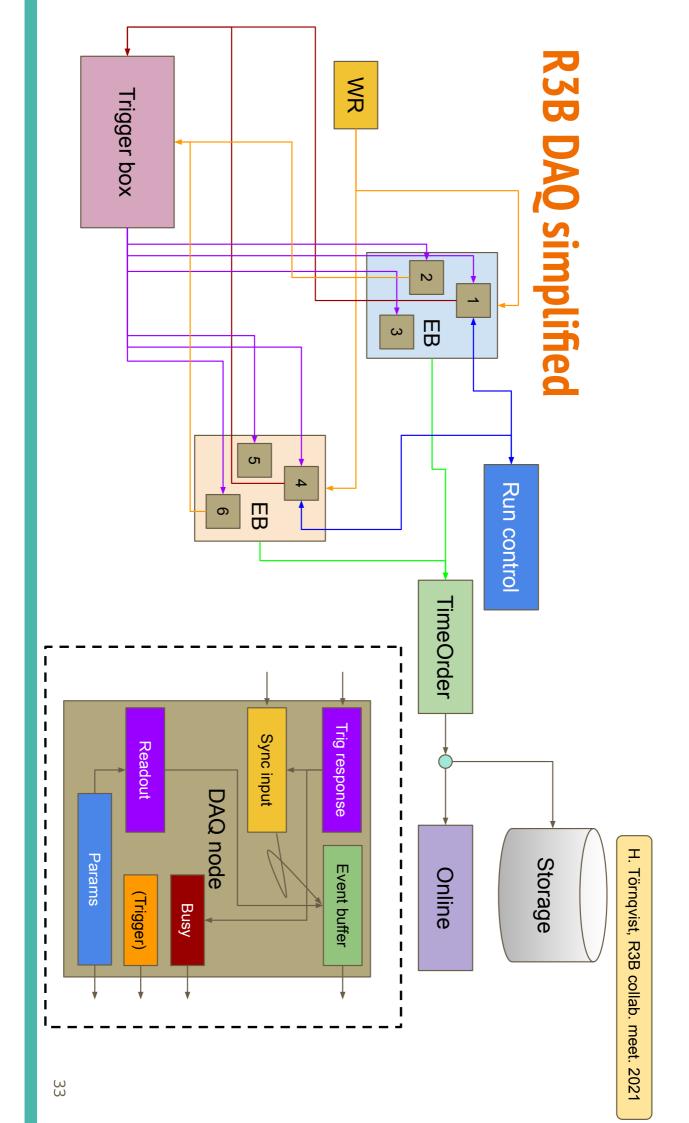
9582

ROLU2 H: 30 mm

THE END

Thanks for listening!

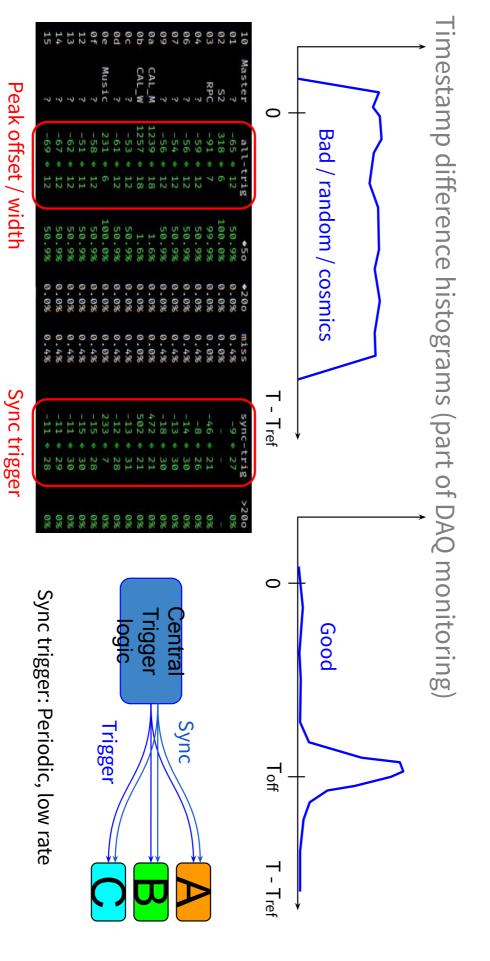
Also thanks to B. Löher, H. Johansson, M.Munch, H. Simon, A. Heinz, S. Petri, the R3B@GSI group, the GSI EE dept., and many many more!



Why timestamped+triggered?

- Flexibility systems can come and go, broken systems don't harm everyone
- Pro: Local failure has no effect on the rest, especially helpful during preparations
- Con: Local failure can go undetected -> Shift crew must be vigilant!
- Integrity trigger is a common reference point
- Pro: Common reference time available everywhere
- Con: Different cabling required -> Prepared in advance
- Sparse data only data of interest is recorded
- Pro: Unrelated data (cosmic / noise) is dropped from unrelated systems, moderate storage/computing requirements
- Con: Region of interest needs to be correct -> Requires monitoring
- Event-wise data in single file
- Pro: Simplifies analysis
- Con: Time sorting and time stitching is required for correlations -> Part of DAQ software + UCESB

Monitoring - Timestamp differences





DAQ — MBS and drasi

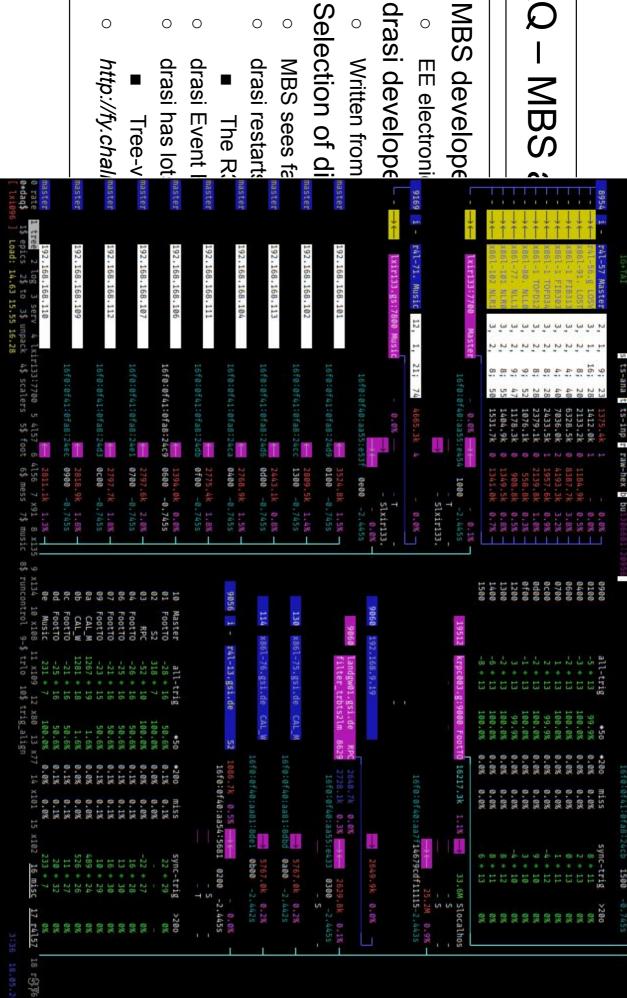
- MBS developed by the EE at GSI
- EE electronics shipped with MBS readout
- drasi developed by H.T. Johansson at Chalmers
- Written from scratch with ideas and interfaces compatible with MBS
- Selection of differences
- MBS sees faster implementation of EE developments
- drasi restarts very fast, esp. for multi-branch systems

0

- The R3B DAQ main branch restarts typically in a few seconds
- drasi Event Builder and Time Order processes can build and execute "anywhere"
- 0 drasi has lots of monitoring tools
- Tree-view, incoming + outgoing rates of all connections, deadtimes
- 0 http://fy.chalmers.se/~f96hajo/drasi/doc/

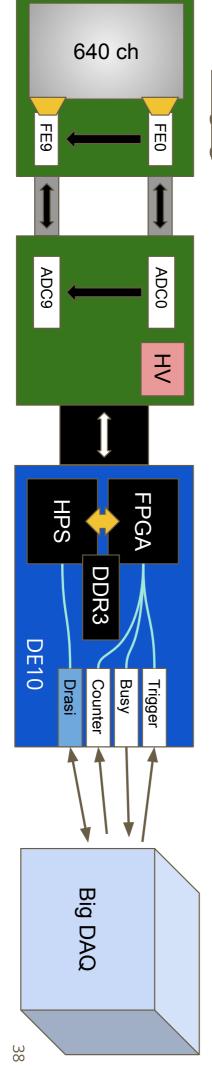


DAQ - MBS



FOOT building blocks

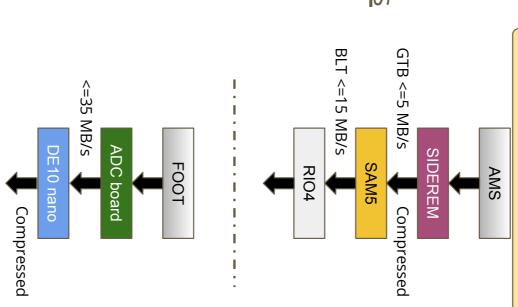
- Detector 640 ch
- Front-end (FE) IDE1140, charge + hold muxing 10 MHz ASIC, 64 ch/chip, 10/detector
- <u>ADC</u> AD7276, single-channel 12-bit 48 MHz ADC, 1/FE
- FE and ADC actually clocked at 1.25 & 25 MHz
- <u>DE10-FPGA</u> busy locking, trigs and clks FE:s + ADC:s, creates events, fills DDR3
- <u>DE10-HPS ("CPU")</u> Init + config, LMD-event building, unique ID, networking
- Syncing FPGA 50 MHz counter, can be driven externally
- <u>Merging</u> defiled ucesb



FOOT data rate & compression

H. Törnqvist, R3B collab. meet. 2021

- FE <-> ADC <-> FPGA <-> HPS max xfer rate ~35 MB/s
- Makes 3 TB/day!
- Sometimes just 16 MB/s until restart, don't know why yet
- That is 1 detector, 10 detectors... Just no
- AMS had only 5 MB/s over GTB, slower than FE
- Compress already in SIDEREM
- **FOOT** xfer lines much faster than FE, compress later
- dptc by H.T. Johansson, G. Bruni et al (<u>http://fy.chalmers.se/subatom/dptc/</u>)
- Fast "smooth" lossless trace compression
- Due to ADC swizzling and endianness, reshuffle data before
- ∼5.5 MB/s
- compressed / raw data Upexps can do unpacking and decompression of



FOOT single system stability

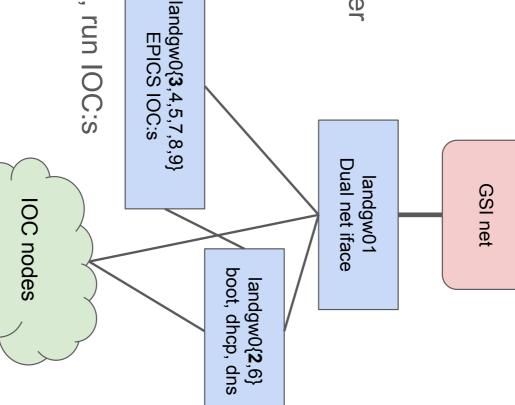
- The original FPGA comm / readout code was very unstable
- Event corruption beyond a few kHz incoming triggers, not accepted
- Also seen by FOOT collab during several tests with two DAQ:s
- An interplay of two sources:
- New FW, have no idea what the original DE10 FW was
- Simpler DDR3 buffering code, the original tests were incorrect
- Now fills 10 MB buffer, extracts events, shifts, repeat, no exaggerated tests needed
- Went from initial unstable 2 kHz incoming + accepted to rock-solid

1 MHz incoming + 14 kHz accepted

- Recorded more than a billion events without a single corruption
- (Again, we don't really have 14 kHz... But the readout works *thumbs up*)

Network in Cave C

- "Private net", "slow control net"
- Current gateway is an old repurposed boot server
- Struggled badly with many IOC:s + GUI:s
- Was too easy, security and efficient practices nil
- Currently only EPICS gateway
- 1x gateway and network server + identical copy
- Boot server, dhcp server, DNS etc
- 1x IOC server + identical copy
- Runs IOC:s for "dumb" devices
- Computers, including loooads of Raspberry PI:s, run IOC:s
- No slow-downs or crashes since



Outside R3B

Locations Cave C **FRS S2/S4** SS 8

We are not developing inside our R3B bubble:

- nurdlib used by FRS
- nurdlib + drasi used by AP
- parts of control system soon used by DESPEC
- **Aarhus University**
- o nurdlib/drasi
- CERN
- o nurdlib / drasi used at ISOLDE (developed in Aarhus)
- IKP / TU Darmstadt
- nurdlib / drasi used at NEPTUN tagger & DHIPS NRF setup
- nurdlib / drasi used by microcalorimeter readout for FAIR
- **Duke University**o nurdlib / drasi used by HIGS setup at TUNL