# **CMM++** specification and status

Y. Ermoline et al. L1Calo Joint Meeting, Cambridge, 23-25 March 2011

# CMM++ project specification



- The first version of the CMM++ project specification available:
  - http://ermoline.web.cern.ch/ermoline/CMM++/
- This document specify:
  - CMM++ functional requirements,
  - CMM/CMM++ differences,
  - technical aspects of the CMM++ implementation.
- The engineering solutions will be reflected in the detailed hardware and firmware specifications.
- Documents time schedule:
  - Now Jun 2011: clarifications and additions (e.g. data formats)
     ⇒ June 2011: Preliminary Design Review (L1Calo Upgrade meeting)
  - Jul 2011 Jan 2012: engineering specification, design documentation
     ⇒ Sep 2012: Production Readiness Review

# CMM++ functional requirements



### Backward compatibility :

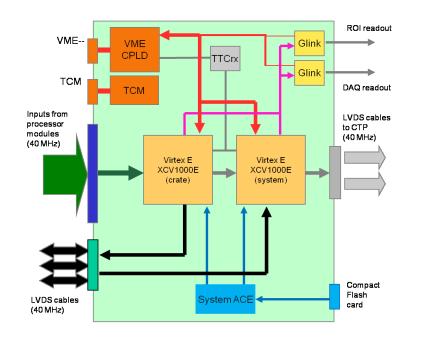
- be designed to fit in the CMM positions in the processor crates ,
- inherit all main logical components, electrical interfaces, programming model and data formats of the current CMM,
- be able to implement all different version of CMM FPGA logic, adapted to new hardware.
- Data source for topological processor:
  - receive extra data from upgraded processor modules over the crate backplane at higher data transfer rate (160Mb/s),
  - transmit data to the TP via multi-fiber optical ribbon link(s),
    - ⇒ "Test" and "Upgrade" modes
  - transmit extra data from upgraded processor modules to the L1Calo Read-Out Drivers.

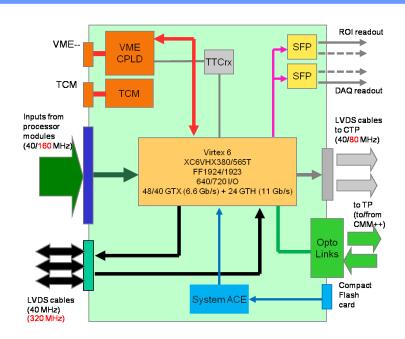
#### Standalone mode

- receive data via additional multi-fiber optical ribbon links,
- provide interface to the new upgraded CTP.

### CMM/CMM++ differences





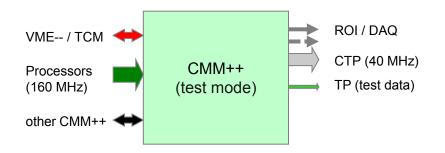


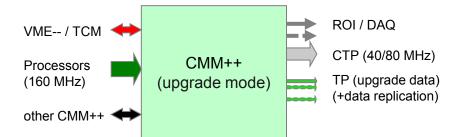
#### Main modifications to the CMM hardware:

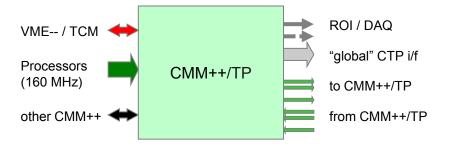
- replacement of the obsolete FPGA devices by new parts to receive data at 160Mb/s from the backplane, transmit and receive data via multi-fiber optical ribbon link using transceivers in FPGA,
- implementation of the G-link protocol in firmware,
- implementation of multi-fiber optical ribbon links,
- selection of FPGA(s) configuration according to the mode of operation.

### CMM++ modes









#### ■ Test mode:

- backward compatible mode
- backward compatible data format
- data to the TP for test purposes.

## ■ Upgrade mode:

- new data format
- data processing/reduction
  ⇒ to fit in a single TP module
- data replication to multiple TPs
- Standalone (CMM++/TP) mode :
  - no TP available
  - data processing/replication
  - data reception from other CMM++
    ⇒ passive fibers re-grouping
  - multiple (CMM++/TP)s

# CMM++ updated development schedule



- 2011: Project and engineering specifications
  - CMM++ project Preliminary Design Review
  - Preliminary design studies
  - Test rig installed, checked out at MSU
- 2012: Prototype design and fabrication
  - CMM++ schematics and PCB layout
  - Production Readiness Review
  - Prototype fabrication, CMM firmware ported on CMM++
  - Tests in basic test stand at MSU
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Prototype tests in test rig at CERN
  - CMM++ firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMM++ modules
- 2014: Final commissioning in the L1Calo trigger system