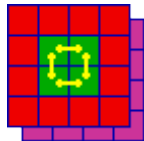


# *MCM Upgrade Status*



R. Achenbach, V. Andrei, P. Hanke,  
K. Schmitt, P. Stock, A. Khomich

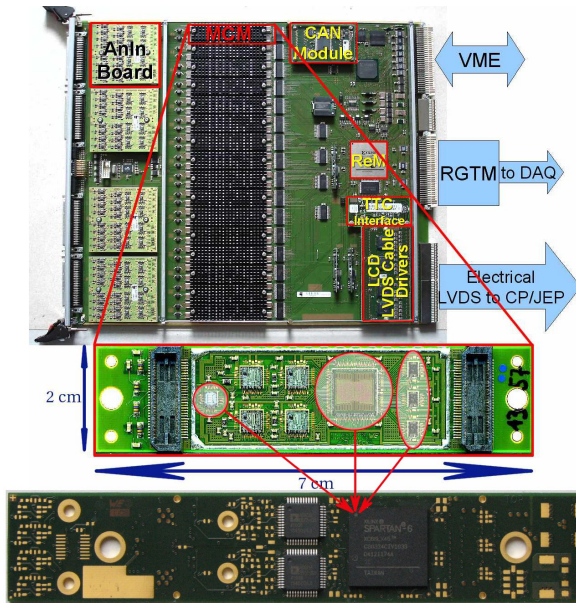
Kirchhoff-Institut für Physik  
Universität Heidelberg



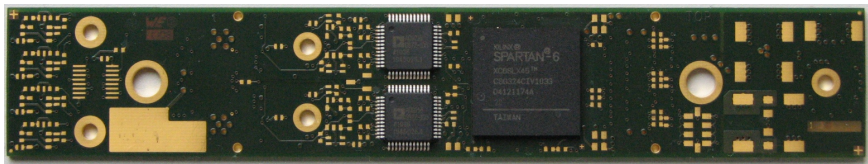
**Level-1 Calorimeter Trigger Joint Meeting**  
Cambridge, 23-25 March 2011

- 1 PREPROCESSOR MODULE
- 2 NMCM FIRST PROTOTYPE
- 3 EARLY IDEAS FOR THE ADDITIONAL FUNCTIONALITY
  - Test signal generation
  - DC Offset Subtraction
- 4 SCHEDULE

# PreProcessor Module and the New MCM

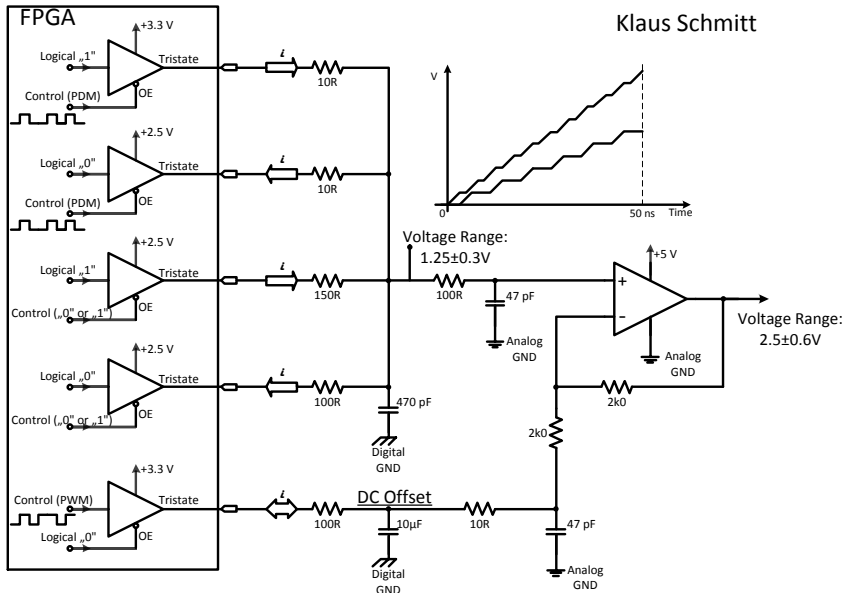


## Selected *n*MCM Components



- AD9218 – dual 105MHz 10bit FADC (running at 80MHz)
- ADA4939-2 OpAmp's (Single-ended-to-differential conversion)
- Xilinx Spartan-6 (SC6SLX45) FPGA in the CSG324 (15x15) package
- Numonyx M25P16 Serial Flash Memory (for the FPGA configuration bitstream and the Module ID)
- LTC3521 DC/DC Converters
- Analogue 1ns delay line

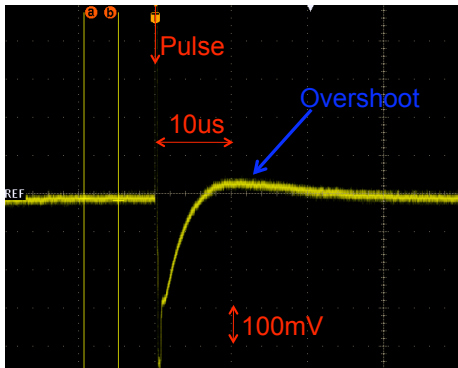
# Test Signal Generation



Monica Dunford:

## Pulse Shapes at Receivers

- At large charges the increase in the baseline after the undershoot is clear



Using the baseline before the pulse as a reference

At 10us  $\rightarrow \Delta V \sim 40\text{mV}$

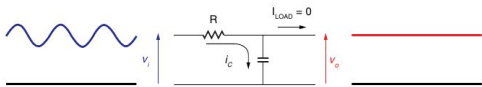
At 30us  $\rightarrow \Delta V \sim 0\text{mV}$

Exists even at the lower charges. For 50 pC per PMT

At 10us  $\rightarrow \Delta V \sim 3\text{mV}$

At 30us  $\rightarrow \Delta V \sim 0\text{mV}$

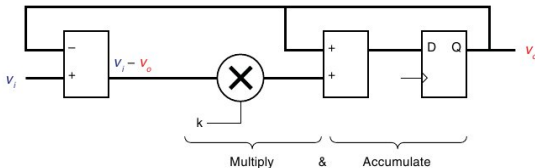
# DC Offset Subtraction



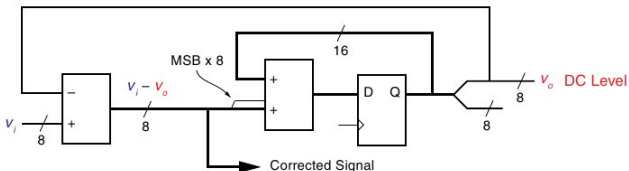
$$k = \frac{\Delta T}{R \times C}$$

$\Delta T$  is defined by the digitisation frequency.

Digital representation of this circuit is:



or, if  $k = \frac{1}{2^n}$ :



# Schedule

