GOLD status

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OUTLINE

- L1 CALO Upgrade
- Generic Opto Link Demonstrator “GOLD” status
- Trigger Topological cuts (simulation)
- Data Format
- Summary

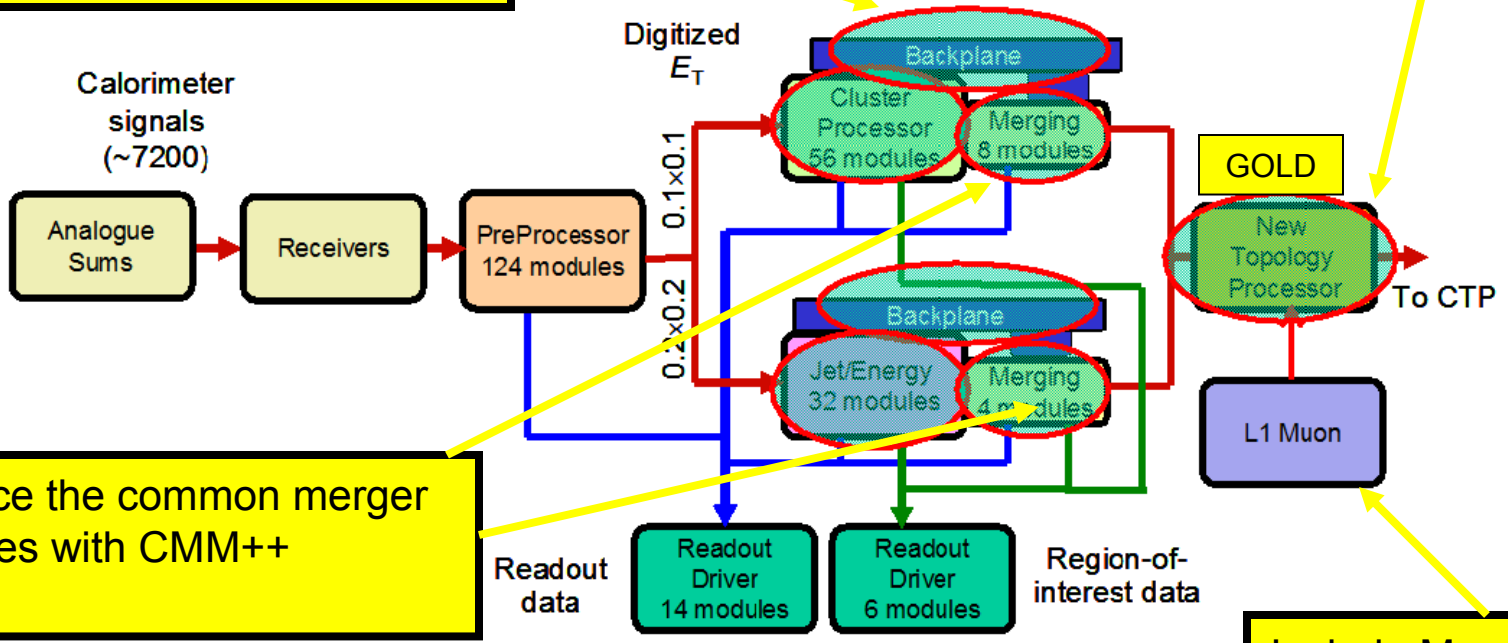
Upgrade of L1 Calo

- **Use of RoIs into the real time data path at L1 and apply topology cuts**
  - fix spatial overlap between e/tau clusters and jets
  - local Et jet sum to estimate the energy overlap of e and tau
  - muon isolation
  - physics signatures
    - angular correlation of jets
    - etc…
- **Transmit full ROIs information will require additional bandwidth**
- **System density will rule out additional electrical cabling**
- **Latency might get critical**
  - Go for optical connections
  - Increase system density by use of FPGA-internal Multi-Gigabit Transceivers
  - Optimize the data replication scheme
  - Explore options for latency reduction on the FPGA (about extra 2BX per MGT)
- **Latency optimization**
  - Data replication schemes
  - FPGA on-chip MGT operation modes and fabric interfaces

Upgrade of L1 Calo trigger

Increase backplane bandwidth from 40Mb/s to 160Mb/s (only modifying FPGA code)

Add a topological processor and increase real time data path bandwidth



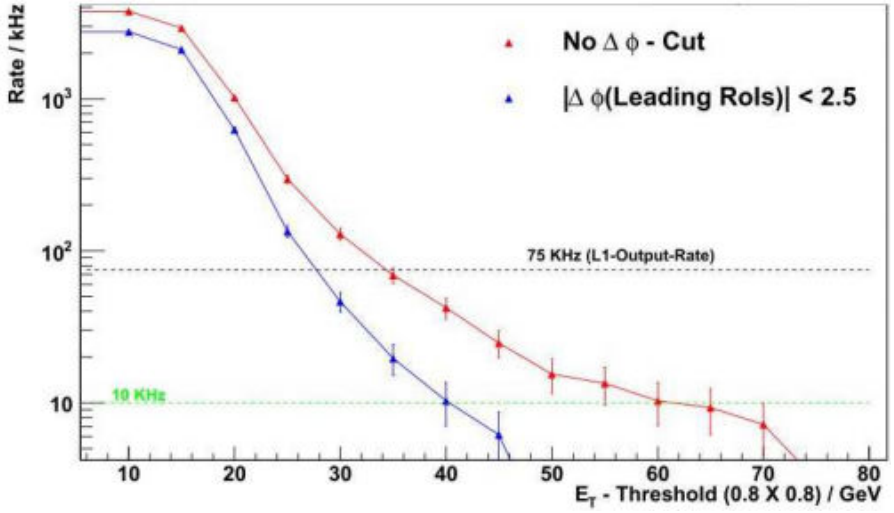
Replace the common merger modules with CMM++

Include Muon processing capability on topological processor

- **Backward compatible to current scheme (for staged installation)**

TP performance in simulation

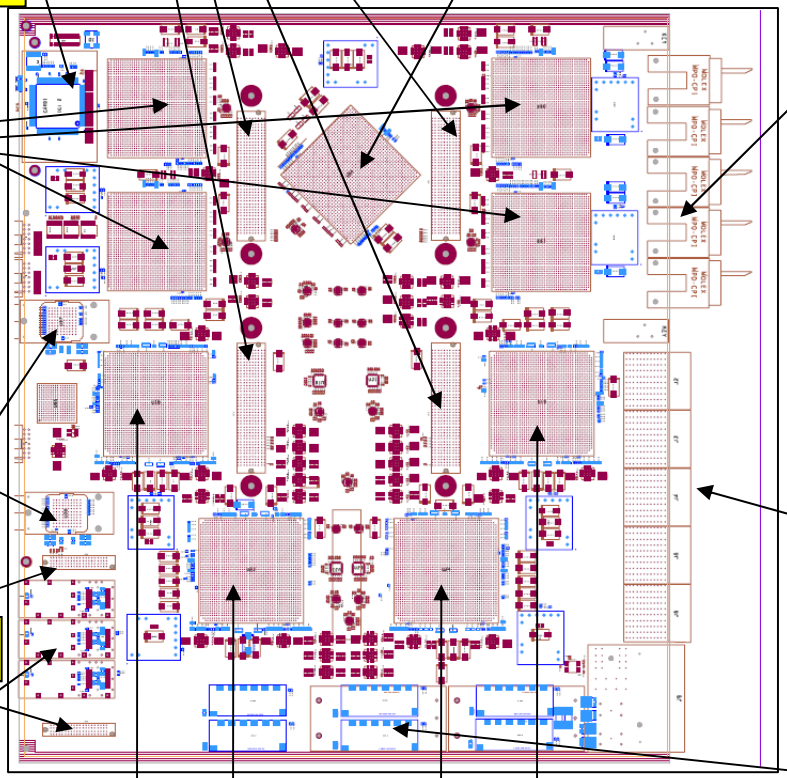
- **Identify trigger processes which benefit from topological trigger**
- **Simulation of physics processes at $1x10^{34}$ $cm^{-2}s^{-1}$ and $3x10^{34}$ $cm^{-2}s^{-1}$**
  - $\Delta\phi$ in Jet + MET at 10^{34} $cm^{-2}s^{-1}$ (QCD bkg reduction)
    - Leading jets RoI at π
    - MET aligned to one Jet RoI



- **Work ongoing on the use of the muons RoI**
  - **Tagging b-jets (for muons at high pt)**
  - **MET from muon (match with Calo info)**
- **Use of transverse mass cuts at L1**

Study total Rate vs. ET, threshold of the 2nd Leading Jet-RoI for various windows size

Design of a Generic Opto Link Demonstrator "GOLD"



opto mezzanine module

FPGA configuration (System ACE) monitoring, module control

One main processor

Four input FPGA **VLX240(550)T Xilinx V6**

Five **optical backplane connectors**

Front panel

backplane

parallel on-board multi Gb links

ATCA form factor

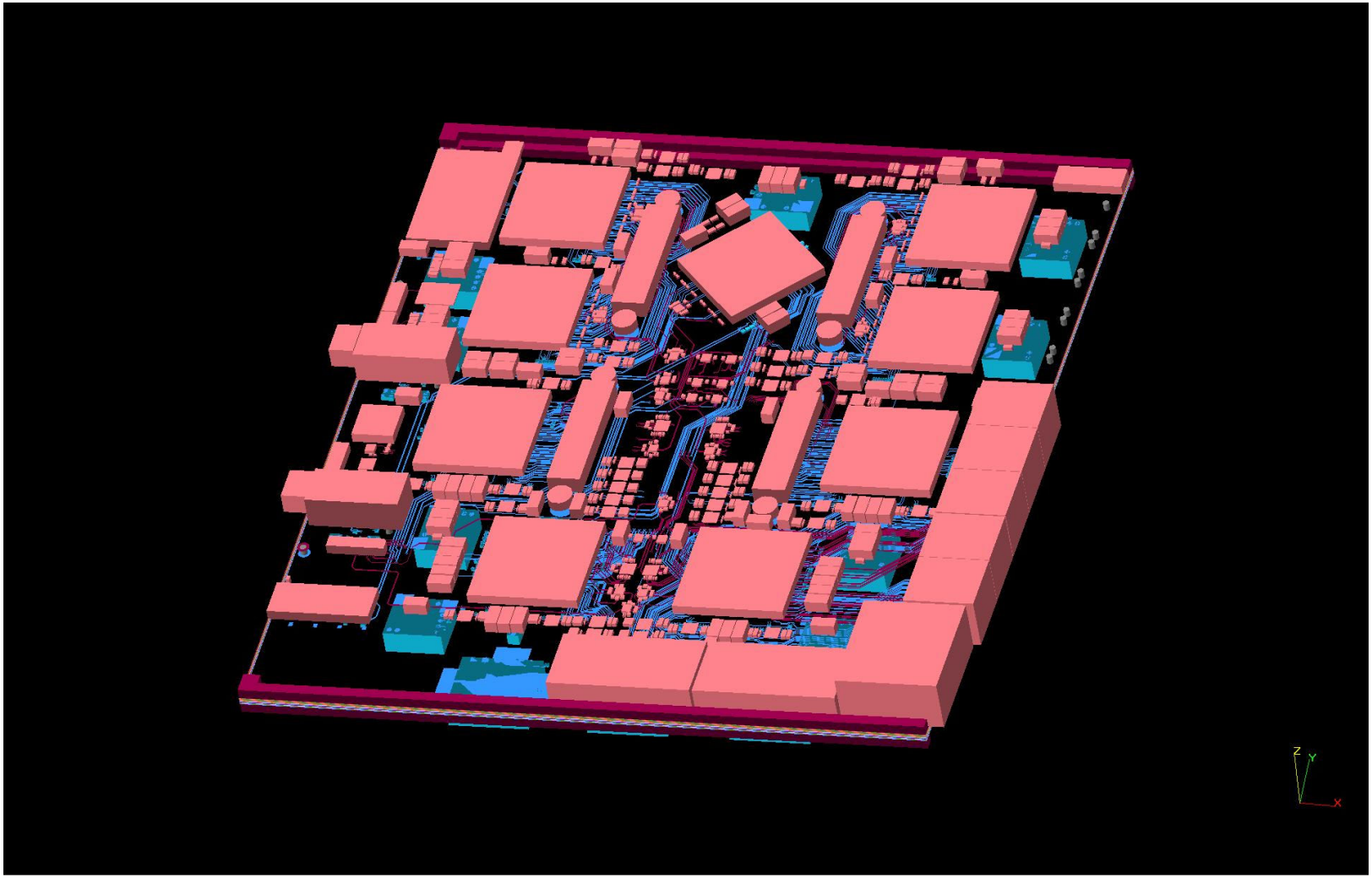
Clock/control mezzanine module

Power regulators

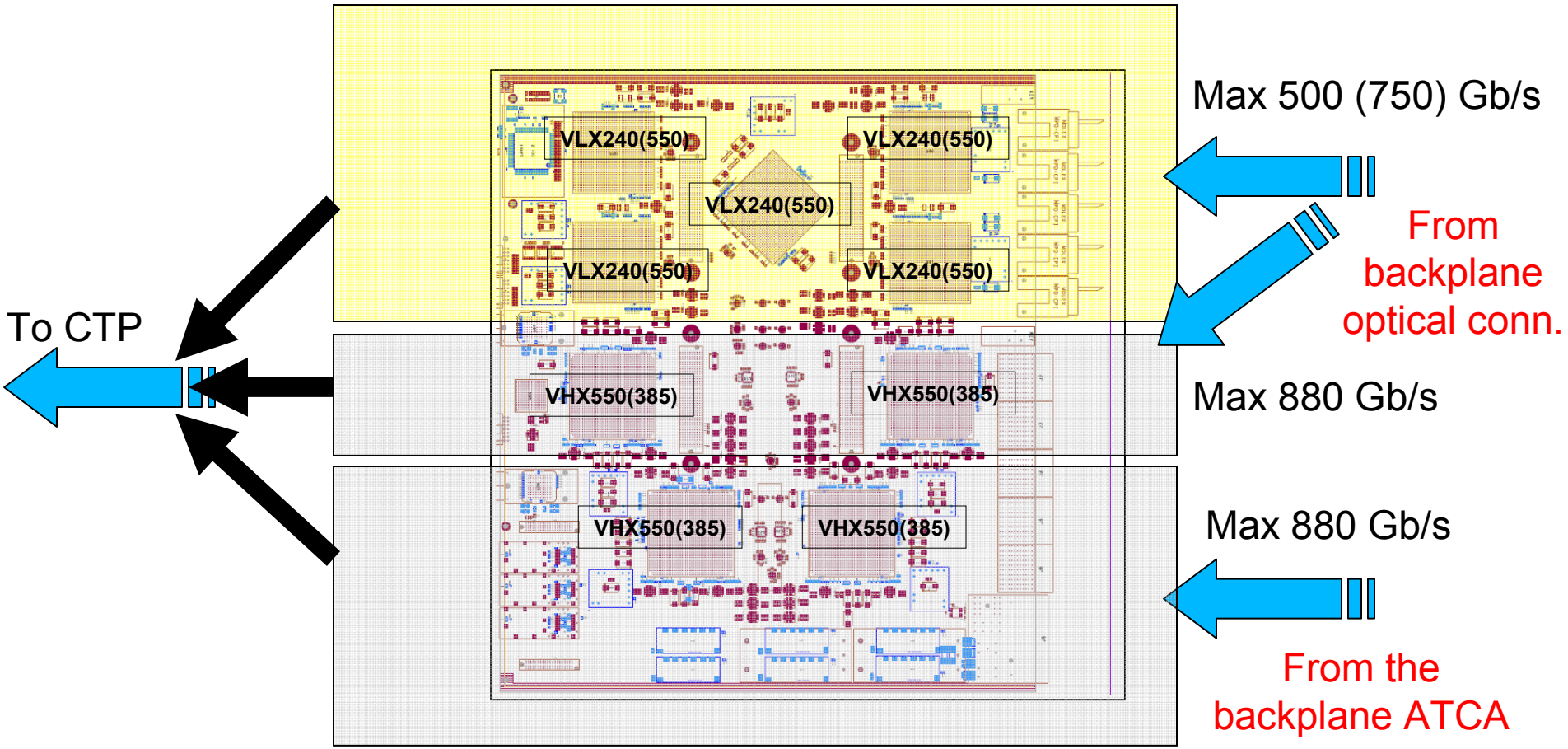
SFP 1/2/3

four extra input FPGA **VHX380(565)T** (not yet available)

3D GOLD



GOLD bandwidth capability



GOLD production status (I)

- **GOLD board design conceptually completed, waiting for final review**
  - Check of the design library and the the components documentation (done)
  - Production issue at the company: needed larger vias (done)
  - Changed power regulators on the FPGA MGT (done)
- **Mezzanines modules 100% routed, waiting for final review**
- **All components available**

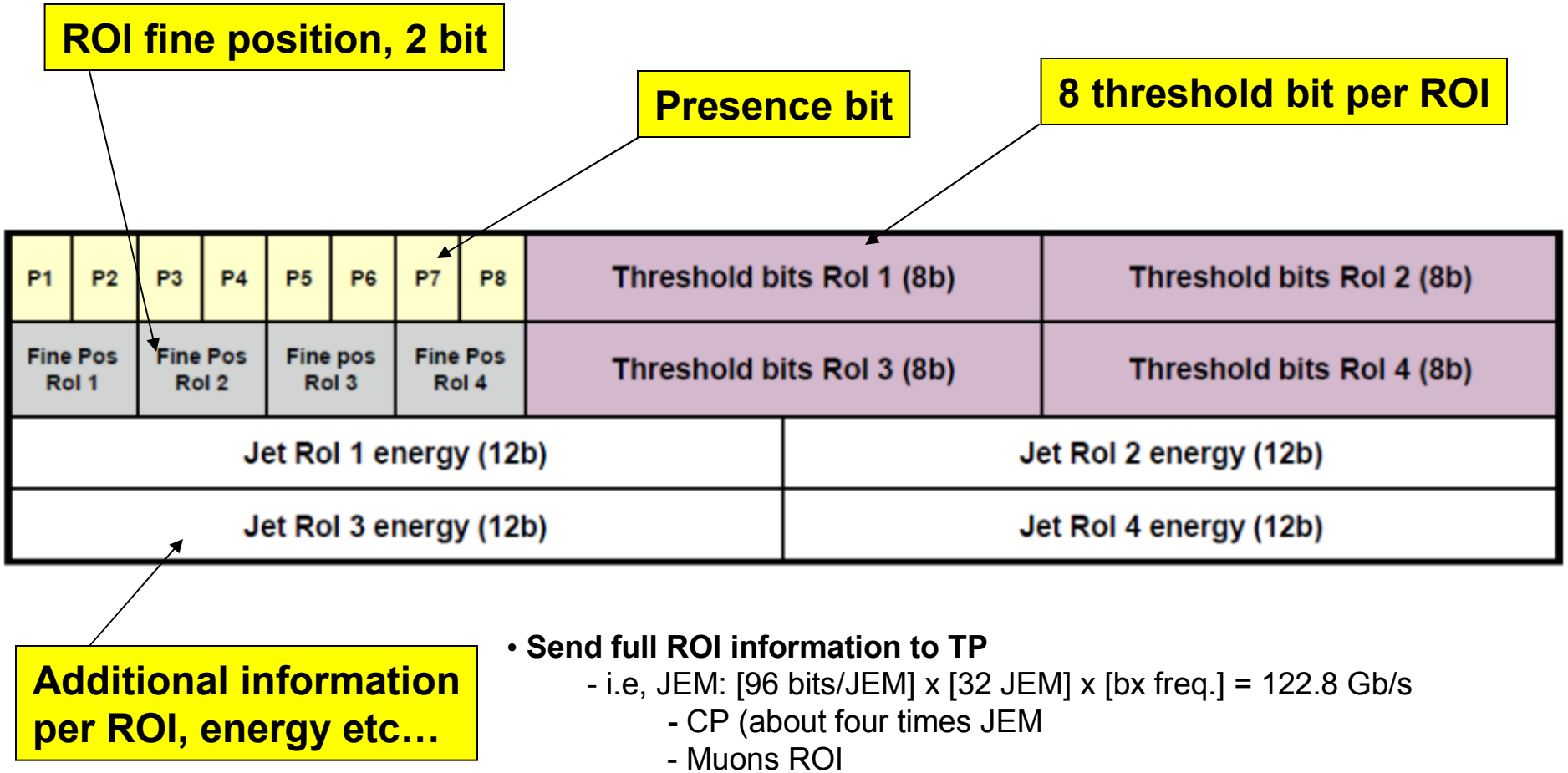
- **Plans for testing**
  - JTAG boundary scan (Goepel tool)
  - Playback/spy tests through BLT (parity, test vectors)
  - GTX/H characterization
    - eye diagrams
    - bit rate error (IBERT tool)
  - Electric tests: cross-talk, reflections, jitter etc…

GOLD production status (II)

- **Firmware**
  - Starting GOLD top design
  - MGT in low latency mode
    - tested the MGT(GTX) at the BLT with and without 8b/10b encoding and phase-alignment up to 6.4 Gbps (low Latency)
    - On Virtex6-VLX phase-alignment also successful (tested up to 5 Gb/s)
    - For phase-alignment one clockbuffer needed per GTX

    (this can be a problem for the VHX)
  - Implementation in VHDL of the $\Delta\varphi$ cut
    - Sorting 2 leading jet according to the Energy information
    - Reconstruct (η,φ) position and constrain $\Delta\varphi$ of the leading Jets
    - Output 2 leading jet information (position bits + Threshold Bits + Energy Bits …)
  - More test firmware

Input data format (JEM preliminary)



- **Send full ROI information to TP**
  - i.e, JEM: [96 bits/JEM] x [32 JEM] x [bx freq.] = 122.8 Gb/s
    - CP (about four times JEM
    - Muons ROI
- **ROI zero suppression and data reduction?**

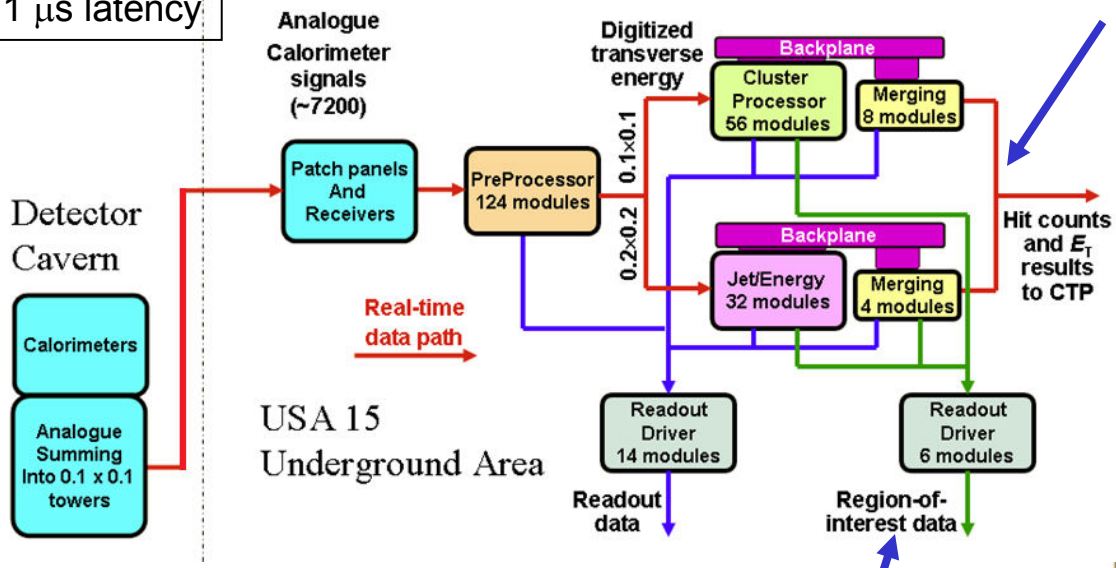
Summary

- **A Topological Processor is required to improve the L1 trigger algorithms at higher lumi**
- **Explore FPGA built in high-speed opto-link (high bandwidth)**
- **Low latency dense optical interconnection**
- **The production of the GOLD prototype about to get started (spring 2011)**
  - many problems fixed
  - review still pending
- **Starting testing the first GOLD prototype during spring 2011**
  - All components are in the lab
  - Design only need to be finalized
- **First TP prototype expected on 1st quarter 2012**
- **Final TP prototype expected to be produced on 3rd quarter 2012**
- **Commissioning of TP on 2nd quarter 2013**
- **Definition of the I/O TP data format in the way of being defined**
- **Simulation studies to investigate applications of the topo-processor are on**
- **Future developments on wish list**
  - Adoption of new generation Virtex-7 FPGA, MGT up to 28Gb/s
  - Recentely joined a German initiative for high density/speed optical readout scheme

ATLAS Trigger

L1 CALO TRIGGER

2.1 μs latency

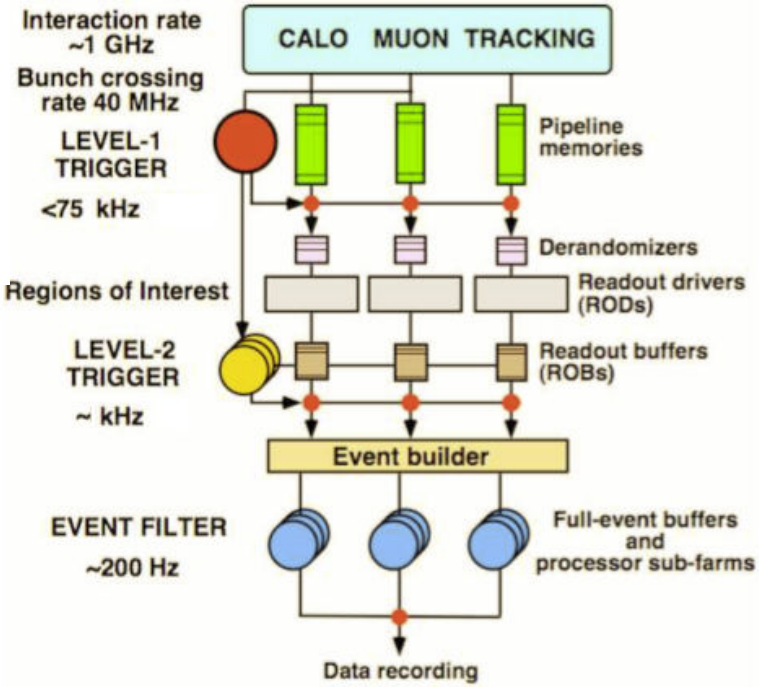


•Final results of electromagnetic and hadronic object count (at given thresholds), and total MT and MET to CTP

• Sliding windows algorithms for jet and em cluster detection on processor modules at granularity ≥ 0.1×0.1 (η×φ)

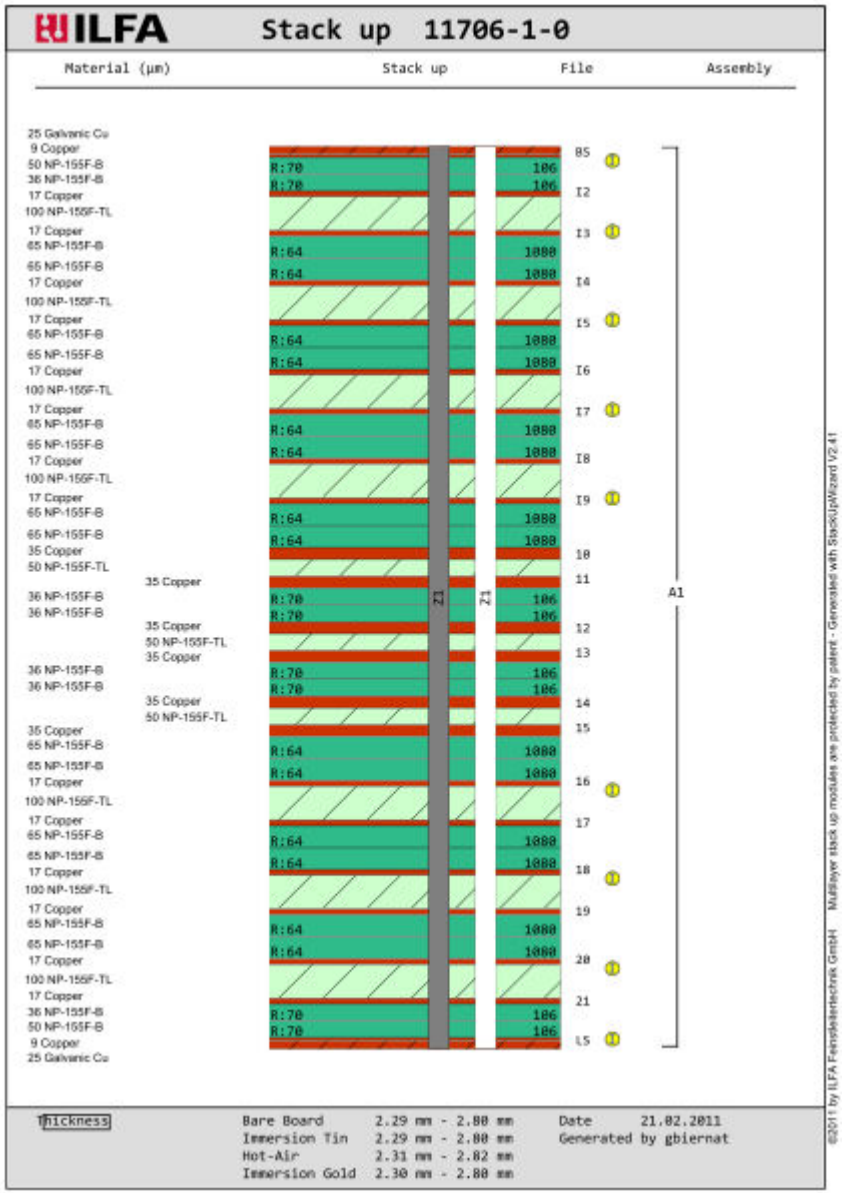
• Topological information (Regions of Interest – ROIs) sent to 2nd level trigger

TRIGGER CHAIN



4 μs buffer depth

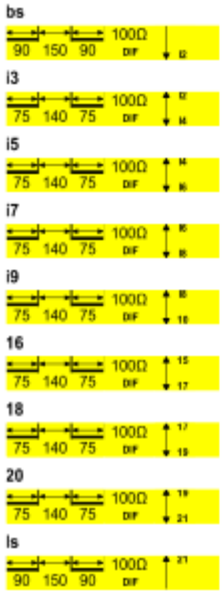
ILFA Stack up 11706-1-0



Thickness

Bare Board	2.29 mm - 2.80 mm	Date	21.02.2011
Immersion Tin	2.29 mm - 2.80 mm	Generated by gbiernat	
Hot-Air	2.31 mm - 2.82 mm		
Immersion Gold	2.30 mm - 2.80 mm		

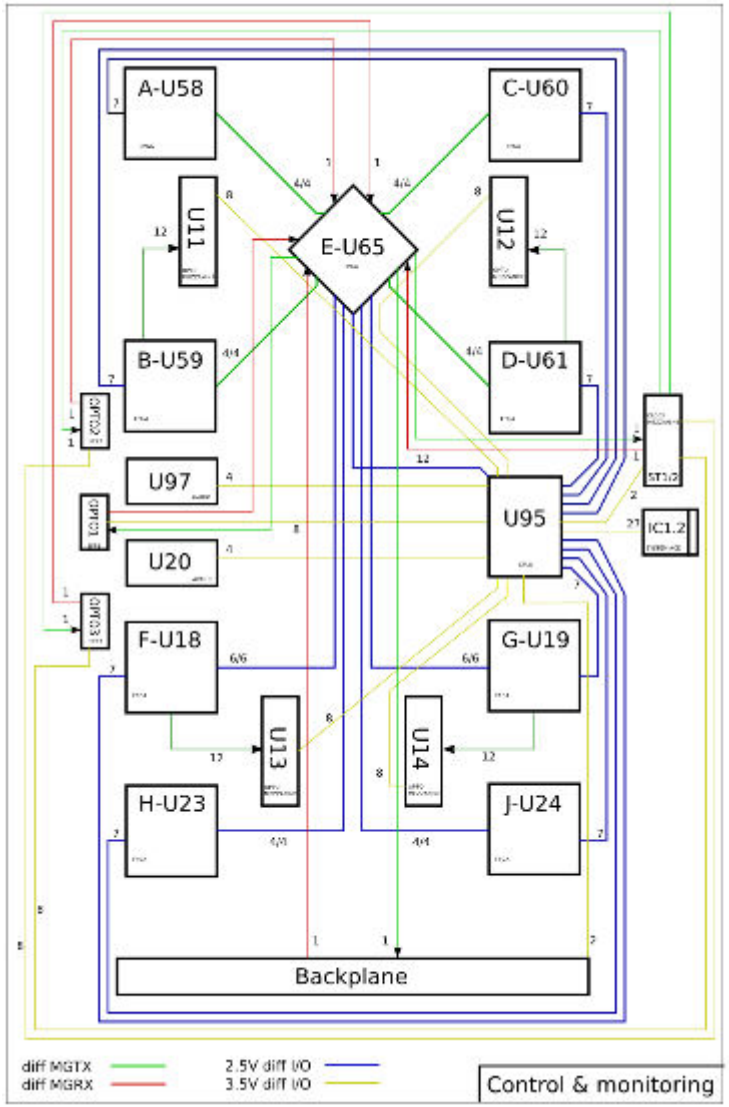
ILFA Impedanzen 11706-1-0

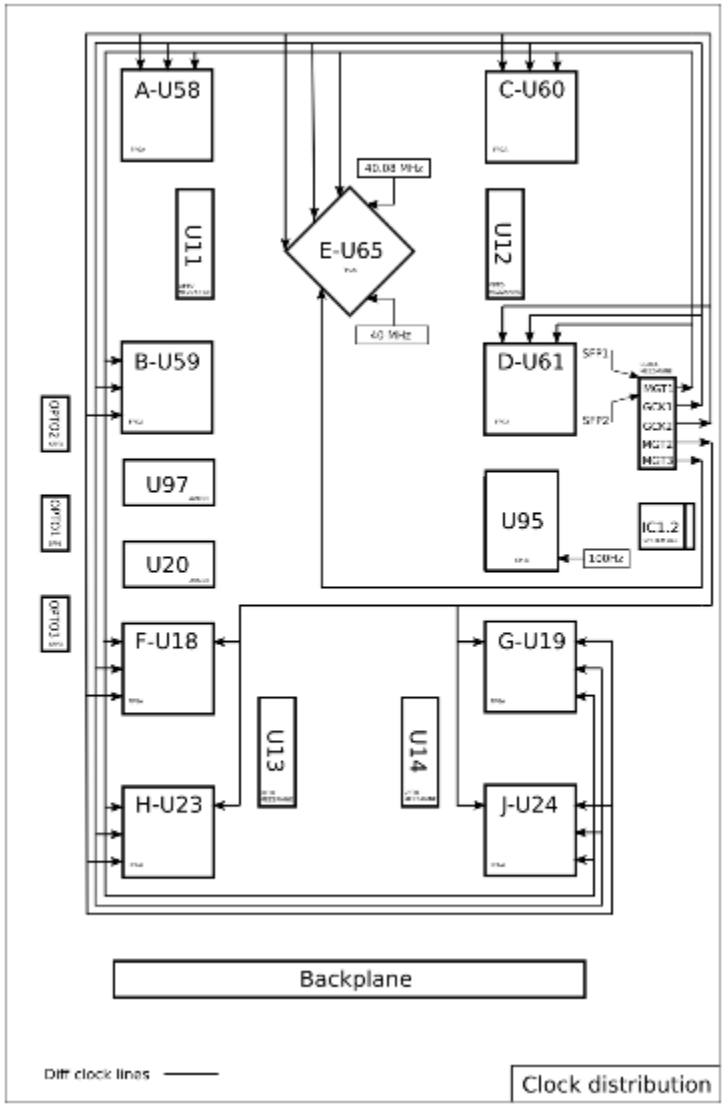


Backplane Link Tester

- In 2010 a backplane and link tester, equipped with Avago opto-link interface (12-channel, 6.4Gb/s) and LHC bunch clock jitter cleaning hardware was built in Mainz.
- Successfully verified backplane data reception (160Mb/s) and opto link operation.

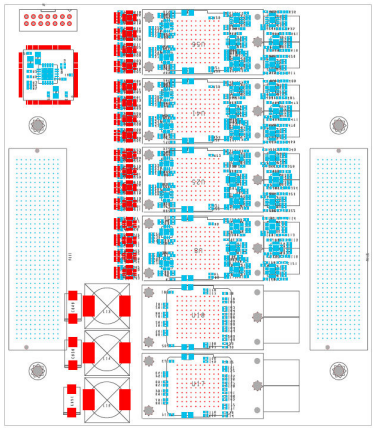
- Will serve as data input for the topological processor


A-U58
C-U60
U11
E-U65
U12
B-U59
D-U61
U97
U95
U20
F-U18
G-U19
U13
U14
H-U23
J-U24
Backplane
diff MGTX
diff MGRX
2.5V diff I/O
3.5V diff I/O
Control & monitoring


A-U58
C-U60
40.08 MHz
U11
E-U65
U12
40 MHz
B-U59
D-U61
SFP1
SFP2
U97
U95
IC1.2
100Hz
U20
F-U18
G-U19
U13
U14
H-U23
J-U24
Backplane
Diff clock lines
Clock distribution

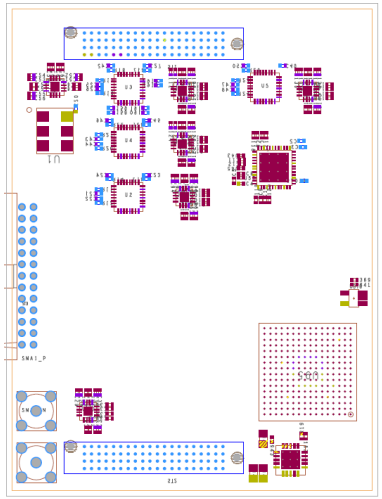
Components

Opto input mezzanine

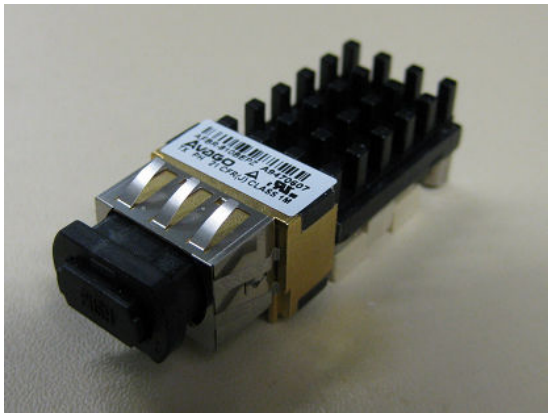


12 to 72 fibres per backplane connector (MPO/MTP)

Clock mezzanine



10Gb/s opto link



Power supply