Si detector development for ALICE ITS3 and ALICE 3

Magnus Mager (CERN) on behalf of the ALICE collaboration
FCC Week 2023
08.06.2023

R = 18, 24, 30 mm
(beam pipe: 16 mm)

L ~ 28 cm
Overview

- **Intro**
  - silicon tracking in ALICE
  - ALICE ITS2
  - monolithic Active Pixel Sensors (MAPS)

- **ITS3**
  - detector concept
  - bending of MAPS
  - 180 nm → 65 nm technology
  - development of wafer-scale sensors

- **ALICE 3**
  - bending
  - layer assembly

- **Outlook**
  - lepton colliders

- **Summary**
ALICE

Detector and main goals

- Study of QGP in heavy-ion collisions at LHC - i.e. up to $O(10k)$ particles to be tracked in a single event

- Reconstruction of charm and beauty hadrons

- Interest in low momentum ($\lesssim 1$ GeV/c) particle reconstruction
ALICE ITS1

... now an artefact

It served some 10 years and was key to many analyses and publications...

... but technology has moved on!

ALICE exhibition at LHC P2

6 layers:
2 hybrid silicon pixel
2 silicon drift
2 silicon strip

Inner-most layer:
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425 \, \mu\text{m}^2$

rate capability: 1 kHz
ALICE ITS2 + MFT
LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)

Inner Tracking System

6 layers:
2 hybrid silicon pixel
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2 silicon strip
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7 layers:
all MAPS
10 m², 24k chips, 12.5 Giga-Pixels
Inner-most layer:
radius: 23 mm
material: X/X₀ = 0.35%
pitch: 29 × 27 μm²
rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker

new detector
5 discs, double sided:
Based on same technology as ITS2
ALICE ITS2 + MFT

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Magnus Mager (CERN) | Si detector development for ALICE ITS3 and ALICE 3 | FCC week, London | 08.06.2023

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ALICE ITS2:
- 7 layers
- 10 m² MAPS
- 12.5 GPixel
- installed in Mar-May’21 (LHC LS2)
ITS2 offspring
dexample: sPHENIX

replica of ITS2 Inner Barrel (3 layers) – installed in Mar’23
### ITS2: ALPIIDE

#### Parameters and Requirements

<table>
<thead>
<tr>
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<th>Req.</th>
<th>ALPIIDE</th>
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<td>&lt; 40</td>
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<td>TID (krad)</td>
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<td>NIEL (1 MeV n_{eq} / cm²)</td>
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**ITS2: ALPIDE**

24k in continuous operation on ITS2 + several other applications

> 70k chips produced and tested

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Monolithic Active Pixel Sensors (MAPS) in a nutshell

- Single silicon chip contains both the detection volume and the readout electronics
  - as opposed to hybrid pixel sensors, which use two chips that need to be interconnected

- Advantages:
  - small pixel pitches: $O(10-30 \, \mu m)$
  - very low capacitances = low power $O(10-100 \, mW/cm^2)$
  - thin: <50 $\mu m$ (0.05% $X_0$)
  - commercial process
Future applications in ALICE

**ITS3:** wafer-scale, bent MAPS

- R = 18, 24, 30 mm (beam pipe: 16 mm)
- L ~ 28 cm

**ALICE 3:** based on a 60 m$^2$ silicon tracker

- Superconducting magnet system
- Tracker
- RICH
- TOF
- Vertex chambers
- Muon absorber

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Run 3 | LS3 | Run 4 | LS4 | Run 5
---|---|---|---|---
2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036 | 2037
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- Muon absorber
- Vertex Detector
- FCT
- ECAL

Run 3: 2023, 2024, 2025, 2026, 2027, 2028, 2029
Run 4: 2030, 2031, 2032, 2033, 2034, 2035, 2036, 2037
ITS2 Inner Barrel
first 3 layers
ALICE ITS3
LHC LS3 upgrade (installation 2027/28)

- Replacing the barrels by real half-cylinders (of bent, thin silicon)
- Rely on wafer-scale sensors (1 sensor per half-layer) in 65 nm technology
- Minimised material budget and distance to interaction point → large improvement of vertexing precision and physics yield ("ideal detector")
ALICE ITS3
Performance improvement

Improvement of pointing resolution by:
- drastic reduction of material budget
  \(0.3 \rightarrow 0.05\% X_0/\text{layer}\)
- being closer to the interaction point
  \(24 \rightarrow 18 \text{ mm}\)
- thinner and smaller beam pipe
  \(700 \rightarrow 500 \mu\text{m}; 18 \rightarrow 16 \text{ mm}\)

Directly boosts the ALICE core physics program that is largely based on:
- low momenta
- secondary vertex reconstruction

E.g. \(\Lambda_c\) S/B improves by factor 10, significance by factor 4
Beam tests

1st paper: NIM A1028, 166280

Clearly proving that bent MAPS are working!

Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale ($10^{-1}$ to $10^{-5}$) to show fully efficient rows. Each data point corresponds to at least 8k tracks.
Qualification of 65 nm CMOS
TPSCo 65 nm CMOS Imaging Technology ("MLR1")

- Concentrated effort ALICE ITS3 together with CERN EP R&D

- Key benefits
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - larger wafers (200→300 mm)

- MLR1:
  - comprehensive first submission: 55 prototype chips
  - goal: qualify the technology (achieved)

- ER1:
  - goal: first test of stitching
  - wafers just came back, tests to start within a few weeks
ITS2 R&D: process modification
full depletion as “side development”

- Addition of a **low-dose n-implant**
  - developed together with foundry
- Opens up new applications
  - higher radiation hardness
  - faster charge collection
- Now crucial for the 65 nm development (it paid off also for ALICE!)

Developed and prototyped within ALPIDE R&D

Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to $10^{14}$ 1 MeV $n_{eq}/cm^2$

Fully depleted epitaxial layer
Charge collection time < 1 ns
after further improvements (outside ALICE): operational up to $10^{15}$ 1 MeV $n_{eq}/cm^2$

Magnus Mager (CERN) | Si detector development for ALICE ITS3 and ALICE 3 | FCC week, London | 08.06.2023 | [doi:10.3390/s8095336]
ITS3: pixel prototype chips (selection)

**APTS**
- **matrix**: 6x6 pixels
- **readout**: direct analog readout of central 4x4
- **pitch**: 10, 15, 20, 25 μm
- **total**: 34 dies

**CE65**
- **matrix**: 64x32, 48x32 pixels
- **readout**: rolling shutter analog
- **pitch**: 15, 25 μm
- **total**: 4 dies

**DPTS**
- **matrix**: 32x32 pixels
- **readout**: async. digital with ToT
- **pitch**: 15 μm
- **total**: 3 dies

Comprehensive set of (small) prototypes and variants to explore the technology for particle detection
APTS – Fe-55 lab tests
comparison of pitches

- Process modification was introduced:
  - full depletion of sensors
  - electric field pointing to collection electrodes

- Pixels of pitches of 10-25 μm show similar results
  - indicates that the charge collection is very efficient

- Allows to choose optimal pitch for the final sensor

This is a remarkable result — showing that we have very efficient charge collection
Detection efficiency

Digital pixel test chip ("DPTS")

First comprehensive paper on 65 nm — summarises 1 year of measurements
Detection efficiency

Digital pixel test chip ("DPTS")

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ITS3: Wafer-scale sensors

Engineering Run 1 (ER1)

- First MAPS for HEP using stitching
  - one order of magnitude larger than previous chips

- "MOSS": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²)
  - conservative design, different pitches

- "MOST": 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²)
  - more dense design

- Plenty of small chips (like MLR1)
Wafer-scale sensors

benefits and challenges

- **Previous** chip sizes are O(1-3 by 1-3 cm²)
  - dictated by mask size
  - masks are exposed once for each chip

- Chips diced out and qualified/selected

- Interconnection on circuit boards (“modules”)

- **Wafer-scale** “chips”/sensors: stitching of exposures
  - same mask exposed in a precisely aligned fashion
  - design is made periodic (metal lines stitch together)
  - (edges and corners need attention)

- Monolithic entity: more sensitive to manufacturing defects (yield)

- All interconnection is done on the wafer: denser, but also less conductive

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**Courtesy: R. Turchetta, Rutherford Appleton Laboratory**
Stitching simplified principle

what we “design”

what we want to fabricate

wafer ($\varnothing = 300$ mm)

reticle (mask)
Stitching simplified principle

- top part

wafer ($\varnothing=300$ mm)

reticle (mask)
Stitching
simplified principle

- repeated part (1)

wafer (⌀=300 mm)

reticle (mask)
Stitching
simplified principle

- repeated part (2)

wafer (⌀=300 mm)

reticle (mask)
Stitching
simplified principle

- repeated part (3)
Stitching simplified principle

- final circuit is a concatenation of different parts of the masks
Thinning/Dicing/Picking tests

- Two pad wafers were thinned and diced (50 μm)
- Chips were picked using dedicated tooling
- Works! — processed wafers underway
wafer probe testing (MOSS)

- Dedicated needle card for MOSS ready
- Tests are starting on fully processed wafers
  - chip is alive! (powering, slow control, digital pulsing)
- Stay tuned for much more!
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LS4: 2036 - 2037
Run 5: 2038 - 2043

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ALICE 3 is centred around a 60 m² MAPS tracker
- innermost layers will be based on wafer-scale Silicon sensors “iris tracker”, similar to ITS3 (but in vacuum)
- outer tracker will be based on modules like ITS2 (but order of magnitude larger)

This is the next big and concrete step for this technology
pointing resolution

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ALICE 3
outer tracker

- 60 m² silicon pixel detector
  - large coverage: ±4η
  - high-spatial resolution: ≈ 10 μm
  - very low material budget: X/X₀ (total) ≲ 10%
  - low power: ≈ 20 mW/cm²

- module (O(10 x 10 cm²)) concept based on industry-standard processes for assembly and testing
ALICE 3
vertex detector

- Based on wafer-scale, ultra-thin, curved MAPS
  - radial distance from interaction point: \(5\) mm
    (inside beampipe, retractable configuration)
  - unprecedented spatial resolution: \(\approx 2.5\) μm
  - ... and material budget: \(\approx 0.1\% \times \)0/layer
  - at radiation levels of: \(\approx 10^{16}\) 1MeV n_{eq}/cm\(^2\) + 300 Mrad
  - and hit rates up to: 94 MHz/cm\(^2\)

- Unprecedented performance figures
  - largely leverages on the ITS3 developments
  - pushes improvements on a number of fronts
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Outlook
lepton colliders and more

- In many respects ALICE can be seen as a prototype for lepton colliders (linear or circular)
  - moderate radiation environments
  - no need for picosecond timing
  - high resolution is key
  - … and indeed, CMOS MAPS have roots in the ILC community (Strasbourg)

- Result: teams mostly interested in FCC-ee, the C3, ILC joined the ITS3 effort to develop the technology
  - large team allows to explore a large phase space — for the benefit of everyone!

- Similar: EIC, SPS Na-XX, medical (proton CT), space
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**Example for “extra” studies**

**ALICE ITS3 preliminary**
Fe-55 source measurements
Plotted on 27 Mar 2023

**APTS SF MUX**
- pitch: 20 μm
- type: modified with gap split: 4
- $V_{\text{subs}} = V_{\text{pent}} = -1.2 \text{ V}$
- $I_{\text{reset}} = 100 \text{ pA}$
- $I_{\text{bias}} = 5 \text{ μA}$
- $I_{\text{bias}} = 0.5 \text{ μA}$
- $I_{\text{bias}} = 150 \text{ μA}$
- $I_{\text{bias}} = 200 \text{ μA}$
- $V_{\text{reset}} = 500 \text{ mV}$

**IDEA Delphes simulation**

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L. Freitag and A.I @ FCC Physics Workshop
Summary

- **ALICE** is continuously developing cutting edge low-material, high-resolution vertex and tracking detectors

- **ALICE ITS2** (now): 10 m² 12.5 GPixel tracker based on the **ALPIDE** chip (180 nm)
  - significant push in terms of integration density, radiation hardness, readout speed wrt previous MAPS generations
  - **stable, >99% functional, quasi noise-free** operation

- **ALICE ITS3** (LS3) project is on track, advancing the technology further in several areas:
  - **bent MAPS** demonstrated in beam
  - **65 nm** process qualified
  - **stitched design** exercised, **testing started**
  - **assembly** procedure of minimal material budget wafer-scale sensors defined

- With **ALICE 3** (LS4), the endeavour will continue, addressing:
  - **large-scale integration** (60 m² outer tracker)
  - increased **spatial resolution, radiation hardness and rate capabilities** + **in-vacuum operation** (vertex detector)

- **ALICE R&D on MAPS** continues to explore the technology beyond its strict needs, yielding
  - current and future ALICE detectors with large operational margins
  - service to the community → **lepton colliders**?!
Thank you!