Upgrade of the CMS ECAL Barrel Off-detector Electronics and L1 Trigger for the HL-LHC

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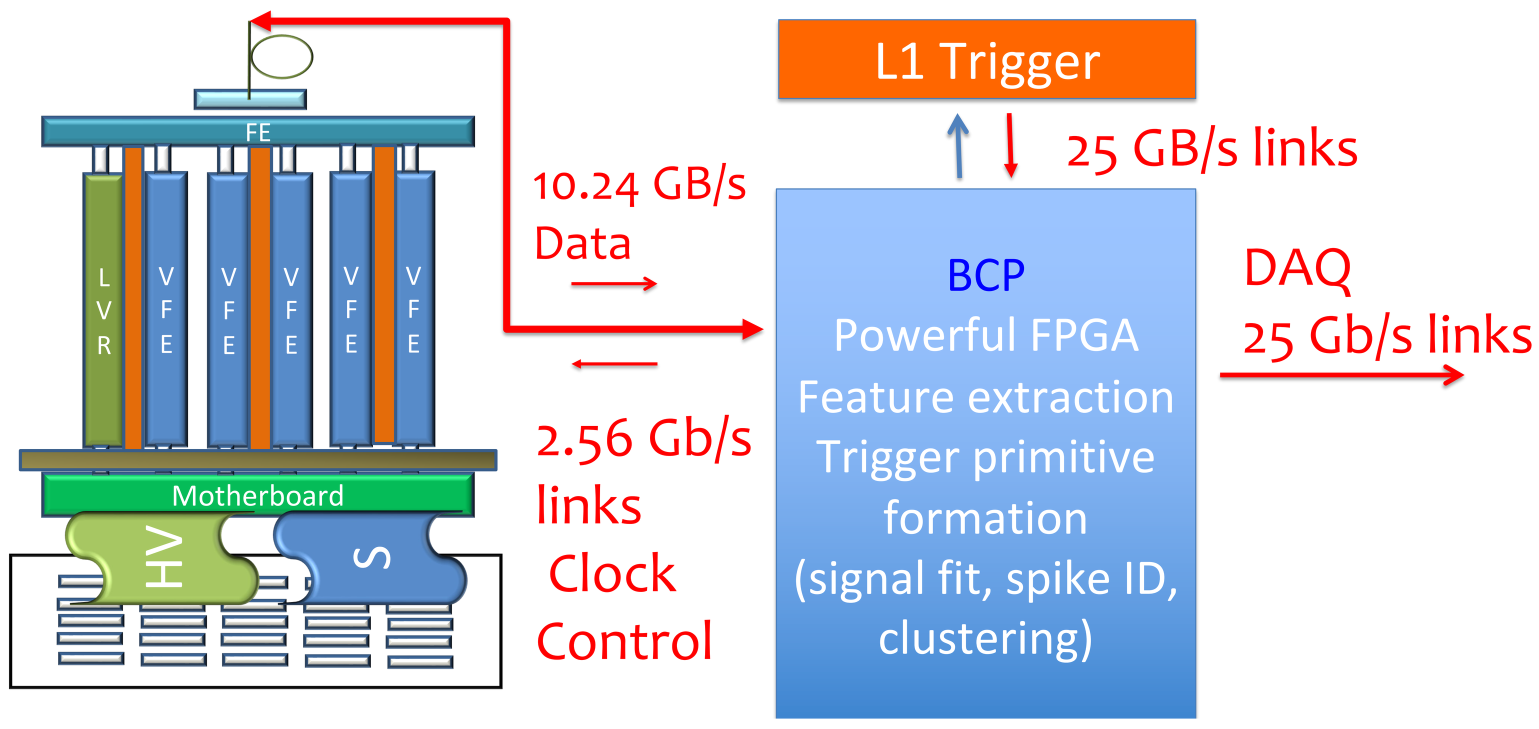
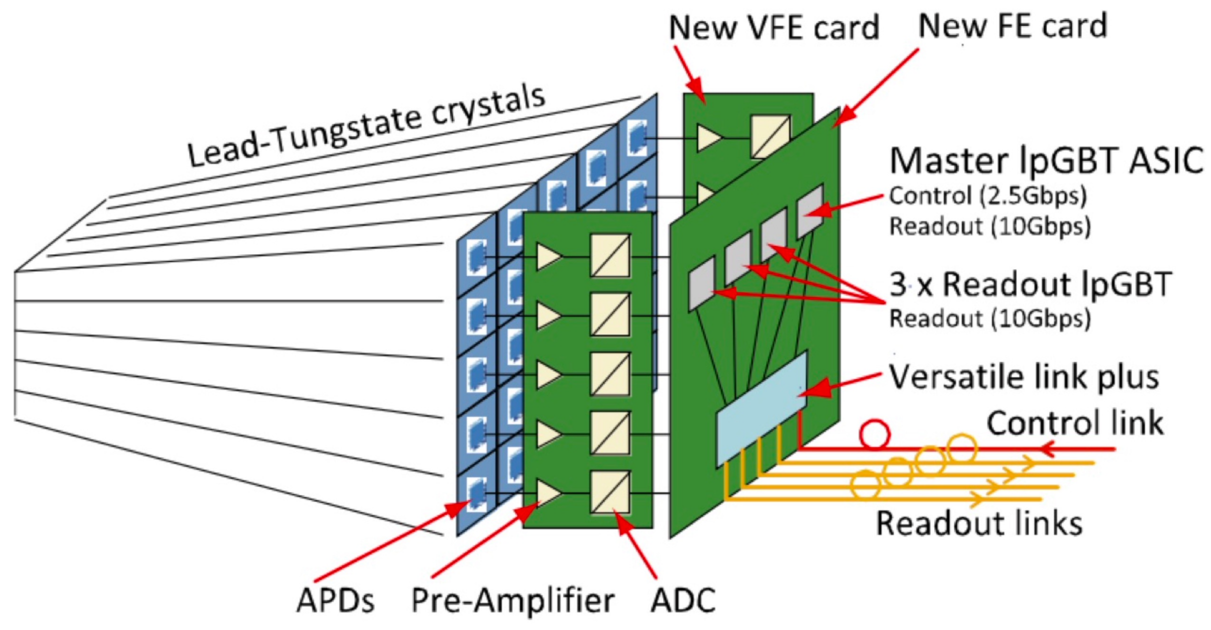


High Luminosity LHC

- **The High Luminosity upgrade of the LHC (HL-LHC) is foreseen to deliver an unprecedented peak instantaneous luminosity of 5×10^{34} cm^{-2} s^{-1}.**
- **Both the on- and off-detector electronics of the CMS electromagnetic barrel calorimeter (EB) will be replaced to mitigate the increased pileup (PU), radiation-induced ageing detector, as well as to guarantee the trigger capability and an overall performance as in Phase I.**



On-detector Electronics

- **The upgraded on-detector electronics will include the new Front-End (FE) cards, each connected to 5 new Very-Front-End (VFE) cards, monitoring 25 crystals in total.**
- **The VFEs sample, amplify and digitize signals from the photodetectors mounted at the back of the crystals every 6.25 ns, which are then transmitted to the off-detector electronics via the high speed lpGBT transceiver on the FEs and optical links.**

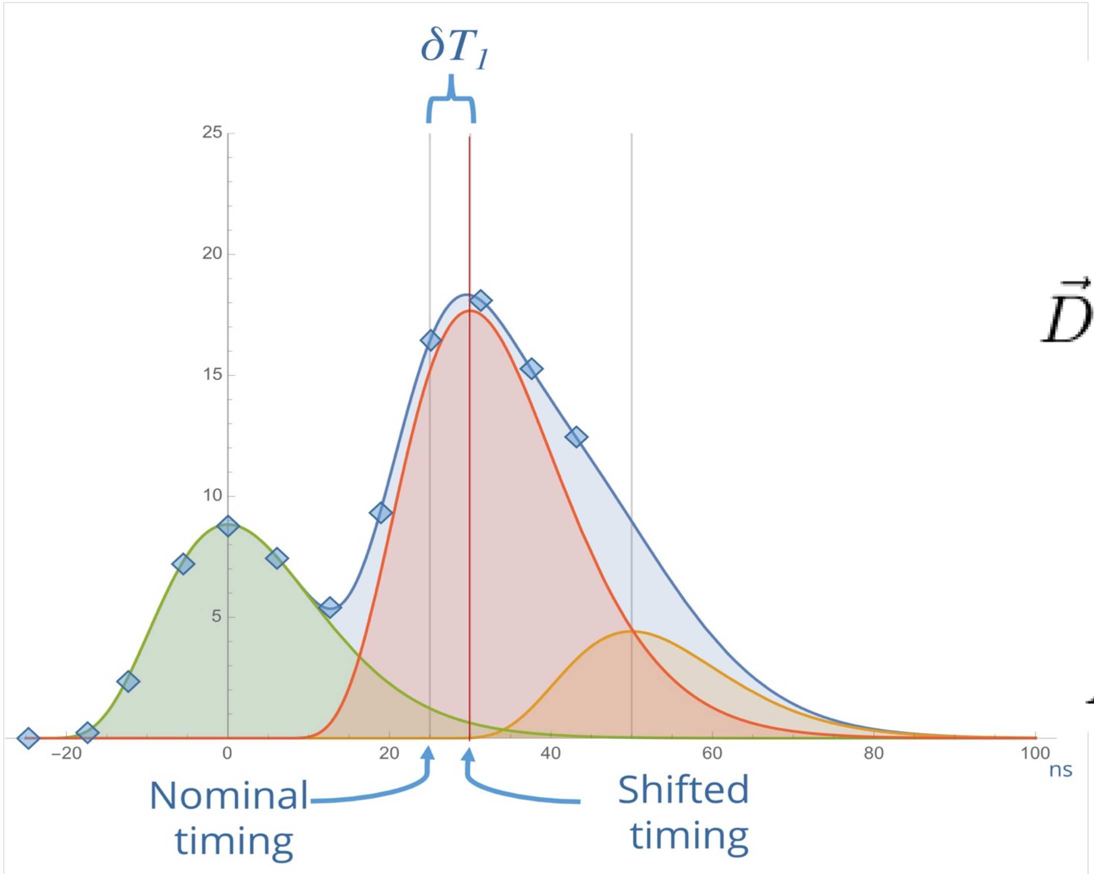
CMS electromagnetic barrel calorimeter L1 Trigger Primitive

- **The overall upgrade of the EB electronics will provide an enhanced granularity of single channel data to the central calorimeter hardware (L1) trigger.**
- **The trigger primitive generation (TPG) will be shifted off-detector to the Barrel Calorimeter Processor (BCP) board with enough pipeline to accommodate the increased CMS trigger latency.**
- **The TPG algorithms will be implemented on high-speed FPGAs housed in the BCP to provide the online linearization of digitized samples, the timing and amplitude reconstruction of signals, the tagging of anomalous signals (spikes), and the clustering of potential electron/photon candidates (e/γ) .**

Single Channel Processing

Amplitude and Timing Reconstruction

- **Signal pulses from the photo-detectors are sampled and digitized every 6.25 ns.**
- **Pedestal subtractions are applied to the digitized samples (digis), which are then calibrated and multiplied by one of the two gain windows dedicated to energy measurements of below ~200 GeV, and up to 2 TeV.**
- **The linearized digis are in general an overlap of signal pulses from multiple bunch crossings (BX), with the timing of the in BX peak shifted within ± 3.125 ns of the sampling time of the VFE.**
- **Multifit is a method to carry out a simplified least square fit of the amplitudes and the shifted timing based on the templated shapes of the pulses, designed to mitigate the out-of-time pileups.**



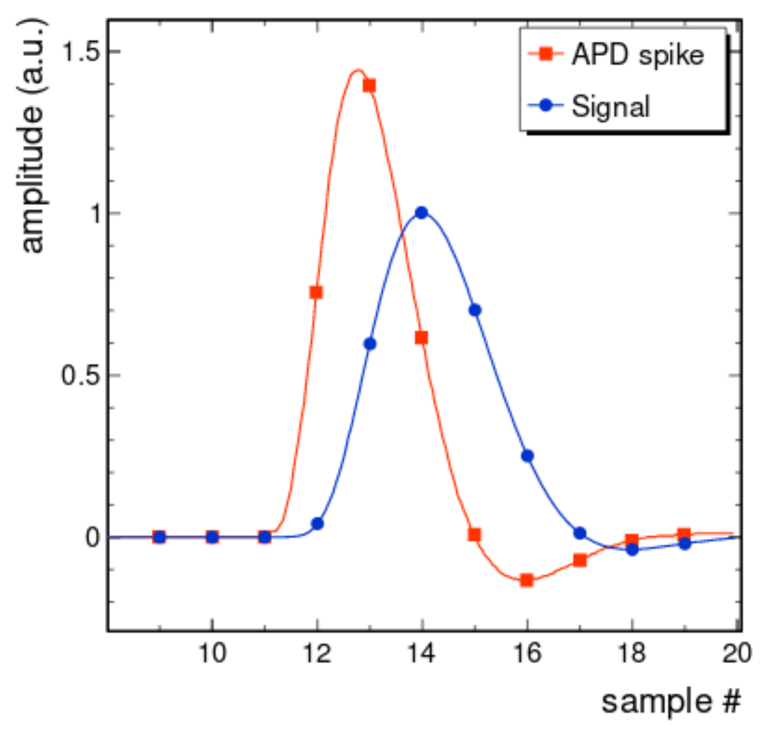
$$\vec{D} = F \begin{bmatrix} A_0 \\ \delta T_0 A_0 \\ A_1 \\ \delta T_1 A_1 \\ A_2 \\ \delta T_2 A_2 \end{bmatrix} = F\vec{A}$$

$$\hat{\vec{A}} = \left(F^T F\right)^{-1} F^T \vec{D}$$

F is the predetermined pulse shape and time derivative vector columns for the in BX peak (with subfix 0), as well as the BX before (subfix 1) and after (subfix 2), relating the amplitudes, A, the shifted timing, δT, of the peaks to the incoming vector of digis, $\vec{D}$.

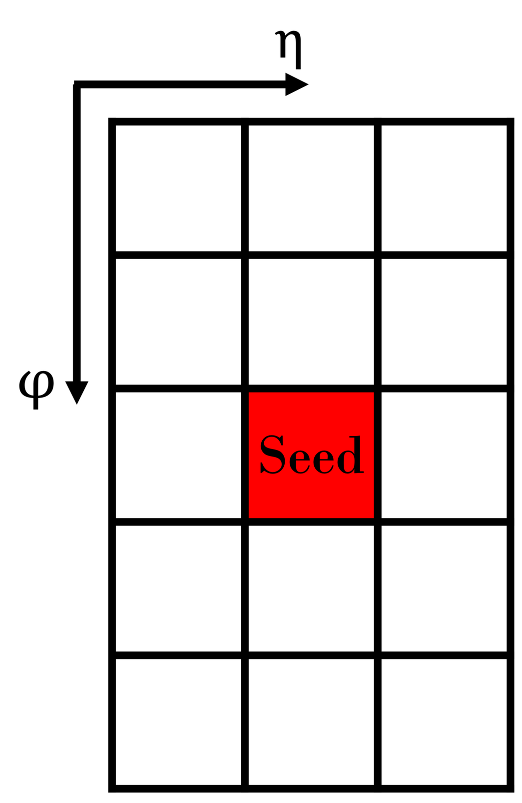
Anomalous Signal Tagging

- **Anomalous signals (spikes) come from hadrons striking the photo-detector directly, instead of actual e/γ.**
- **A simple linear discriminant value could be built from ratios of three consecutive amplitude samples to discriminate the spikes against actual signals based on their characteristic narrow shape.**



Local Clustering

- **A max-finder is built to look recursively for the "seeds" of the clusters: channels with among the highest reconstructed energies above a threshold that are not flagged as spikes.**
- **A local region of 3 x 5 crystals with energy above a threshold are clustered around the "seed".**
- **Energy thresholds for the clustering is configurable, and to be optimized according to the run conditions.**



Timing and Resource Usage on the FPGAs

- **The single channel processing and the local clustering algorithms are implemented on the FPGA to process 600 channels.**
- **The total latency of the TPG algorithms has to be well below the latency allocated to the EB L1 trigger: 1.5 μs, and the resources usage of the algorithms has to be within ~60% of the FPGA for 600 channels.**