
Introduction to Electronics for Particle Physics Experiments

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Electronics System for Experiments group
Microelectronics section



Welcome to CERN

Research &
Discovery

Technology

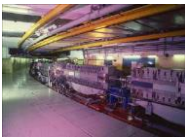
Collaboration

Education &
Training

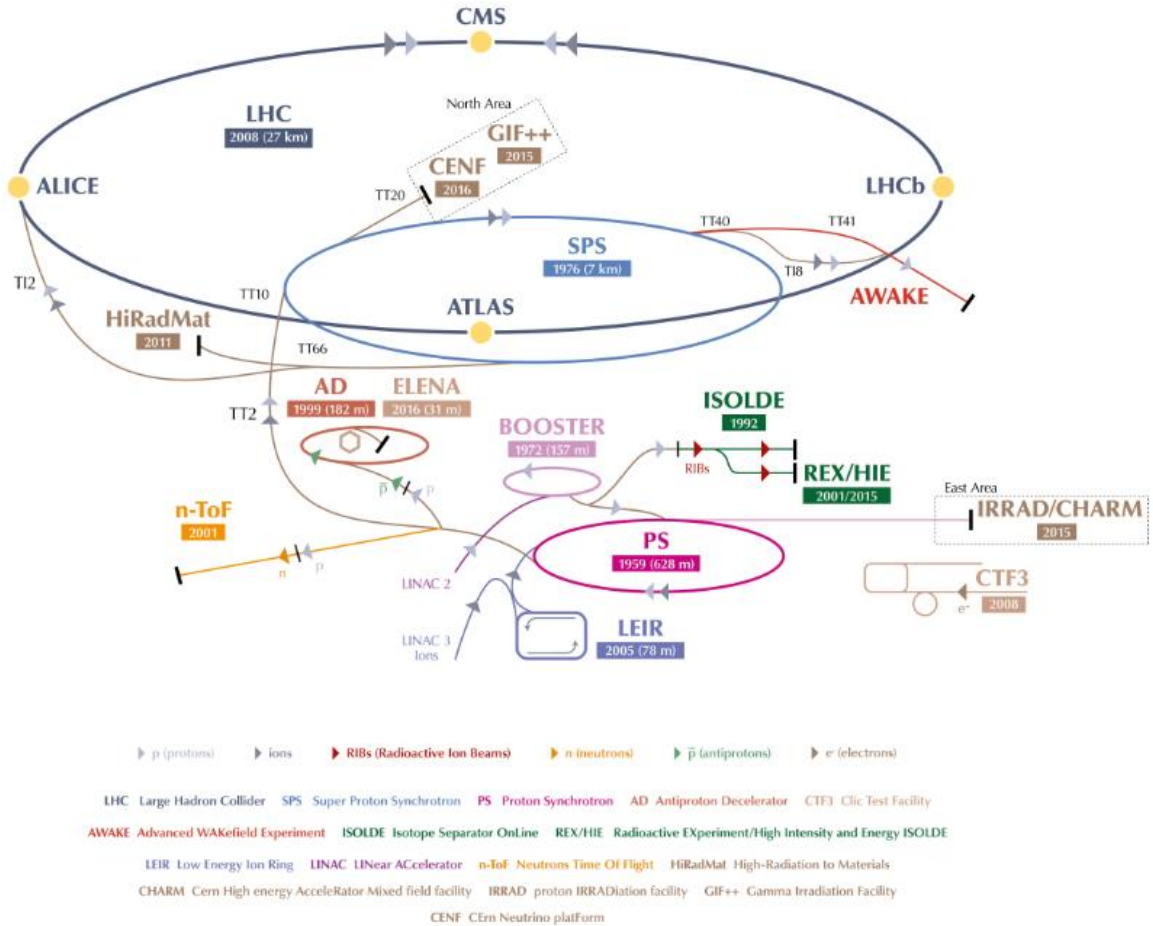




Το σύμπλεγμα επιταχυντών του CERN

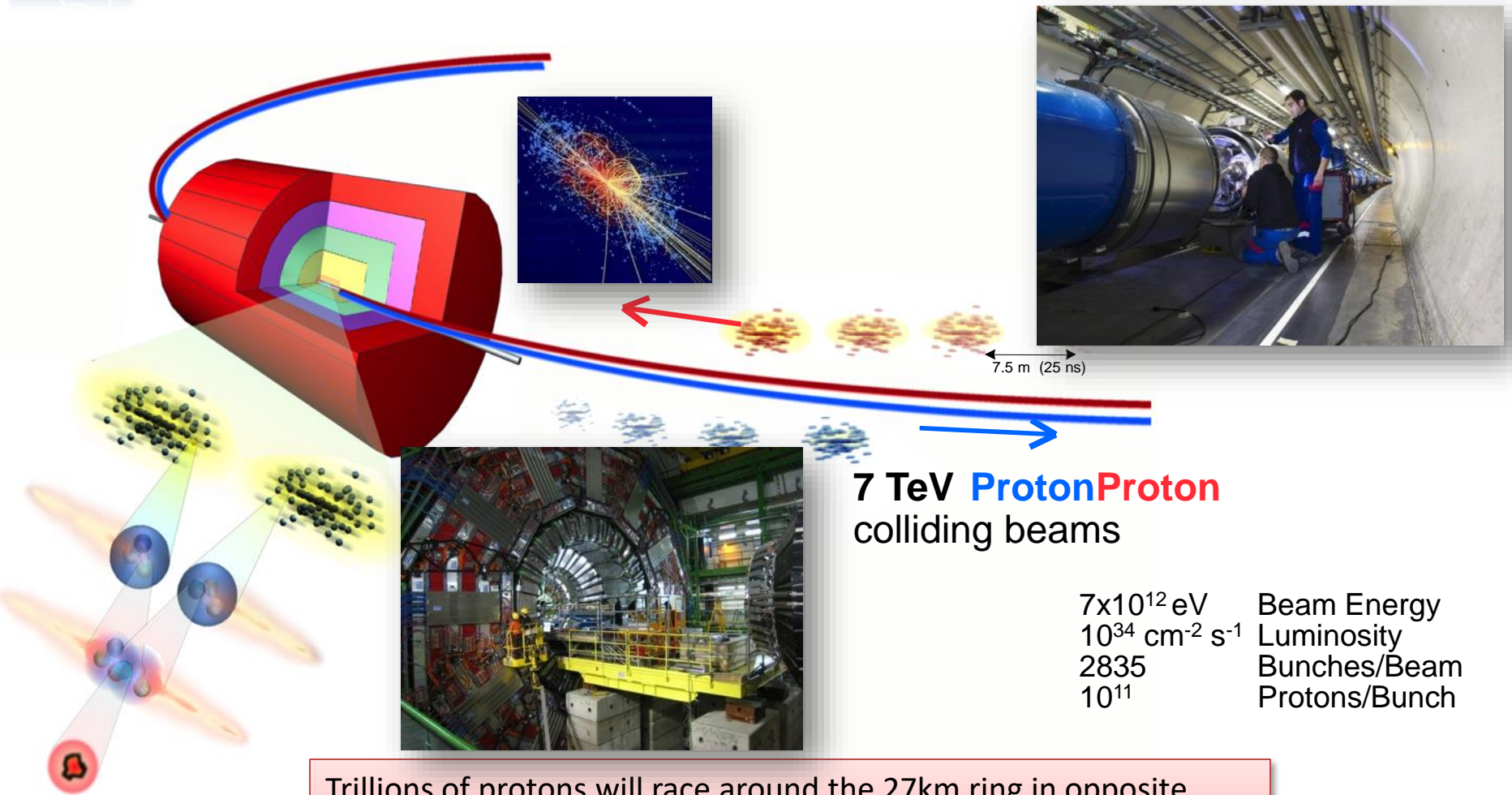


- ⑤ ↑ 7 TeV LHC
- ④ ↑ 450 GeV SPS
- ③ ↑ 26 GeV PS
- ② ↑ 1.4 GeV BOOSTER
- ① ↑ 50 MeV LINAC 2





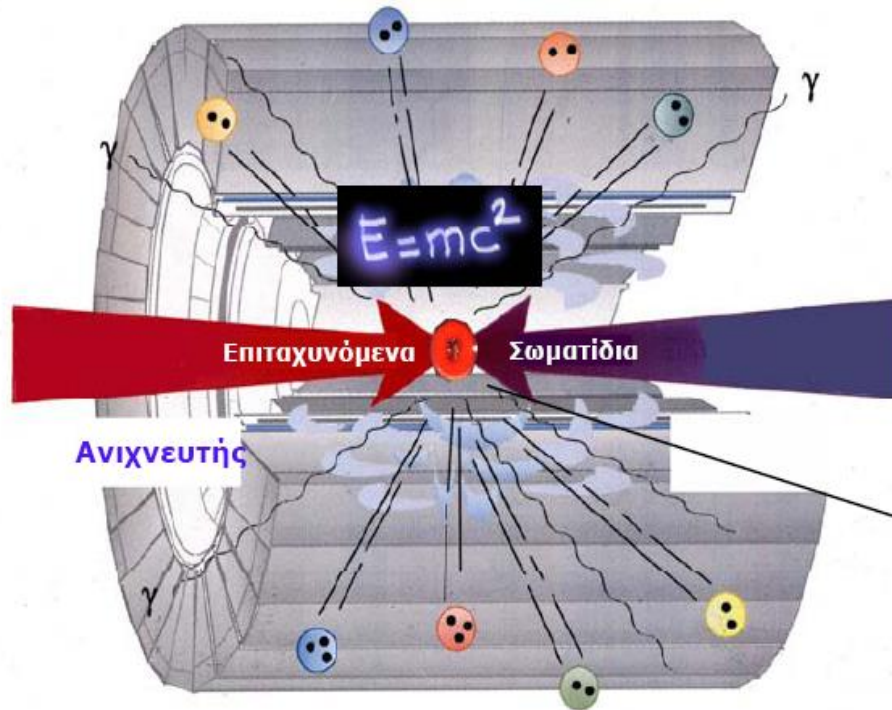
The Large Hadron Collider



7 TeV ProtonProton
colliding beams

7×10^{12} eV	Beam Energy
10^{34} cm ⁻² s ⁻¹	Luminosity
2835	Bunches/Beam
10^{11}	Protons/Bunch

Trillions of protons will race around the 27km ring in opposite directions over 11,000 times a second, travelling at 0.999999991 per cent the speed of light.



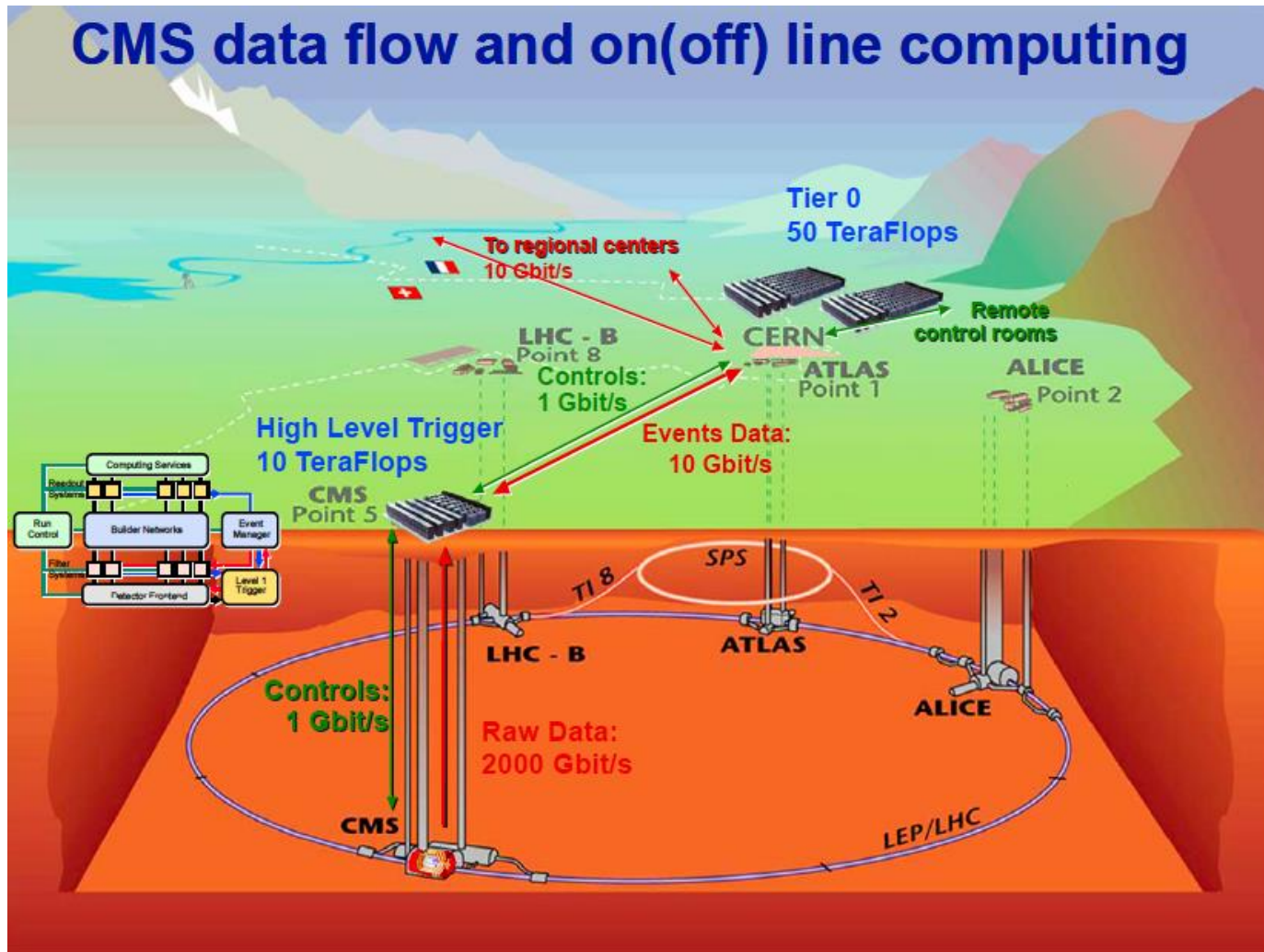
1) Συγκέντρωση ενέργειας στα σωματίδια (**επιταχυντής**)

2) **Σύγκρουση** σωματιδίων (δημιουργία συνθηκών ανάλογων του Big Bang)

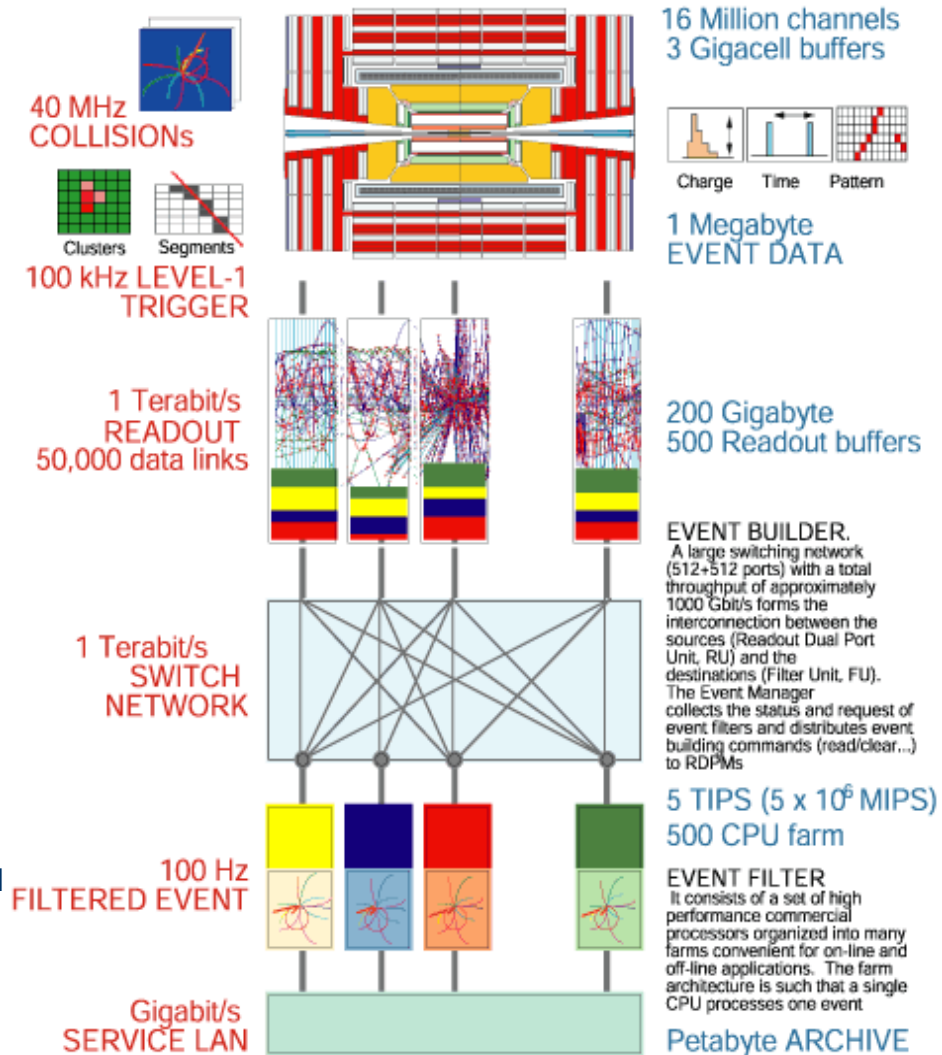
3) Αναγνώριση παραγόμενων σωματιδίων από τον **Ανιχνευτή** (έρευνα για νέα φαινόμενα)

- Τα Σωματίδια συγκρούονται με ταχύτητες παραπλήσιες με αυτή του φωτός με αποτέλεσμα την παραγωγή νέων σωματιδίων. Η διαδικασία αυτή δίνει πληροφορίες για τους μηχανισμούς αλληλεπίδρασης των σωματιδίων και και τους θεμελιώδεις φυσικούς νόμους που τα διέπουν.

The flow of Physics data at LHC



- $40 \cdot 10^6$ φωτογραφίες το δευτερόλεπτο
- 20 συγκρούσεις ανά φωτογραφία
- Το πρώτο φιλτράρισμα των μετρήσεων γίνεται στους ανιχνευτές δίνοντας $100 \cdot 10^3$ φωτογραφίες ανά δευτερόλεπτο
- Το δεύτερο φιλτράρισμα των μετρήσεων γίνεται από συστοιχίες υπολογιστών δίνοντας 1 φωτογραφία ανά δευτερόλεπτο για εγγραφή και μετέπειτα ανάλυση
- Τα πειράματα του LHC παράγουν 10-15 Petabytes δεδομένων κάθε χρόνο (20 εκατομμύρια CDs!)
- Για την ανάλυση των δεδομένων χρειάζεται η υπολογιστική ισχύς που αντιστοιχεί σε $\sim 100,000$ γρήγορους μοντέρνους επεξεργαστές.





Υπολογιστικό κέντρο CERN

- 20,000 PCs





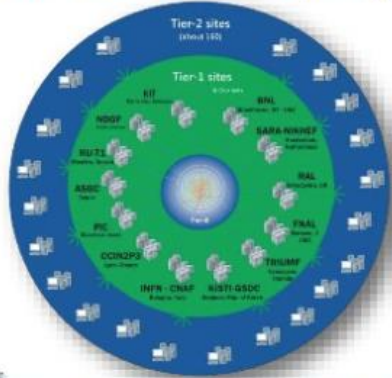
Παγκόσμιο Υπολογιστικό Δύκτιο

The Worldwide LHC Computing Grid

Tier-0
(CERN and Hungary):
data recording,
reconstruction and
distribution

Tier-1: permanent
storage, re-processing,
analysis

Tier-2: Simulation,
end-user analysis



-170 sites,
42 countries

-750k CPU cores

600 PB of storage

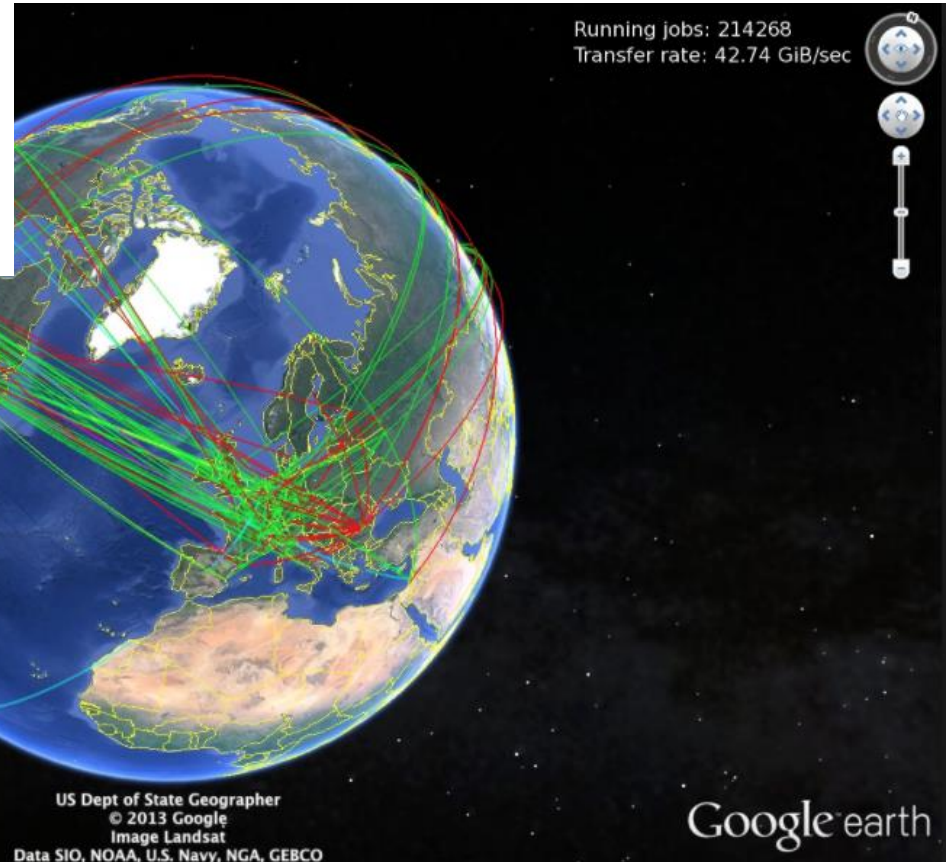
> 2 million jobs/day

10-100 Gb links

WLCG:

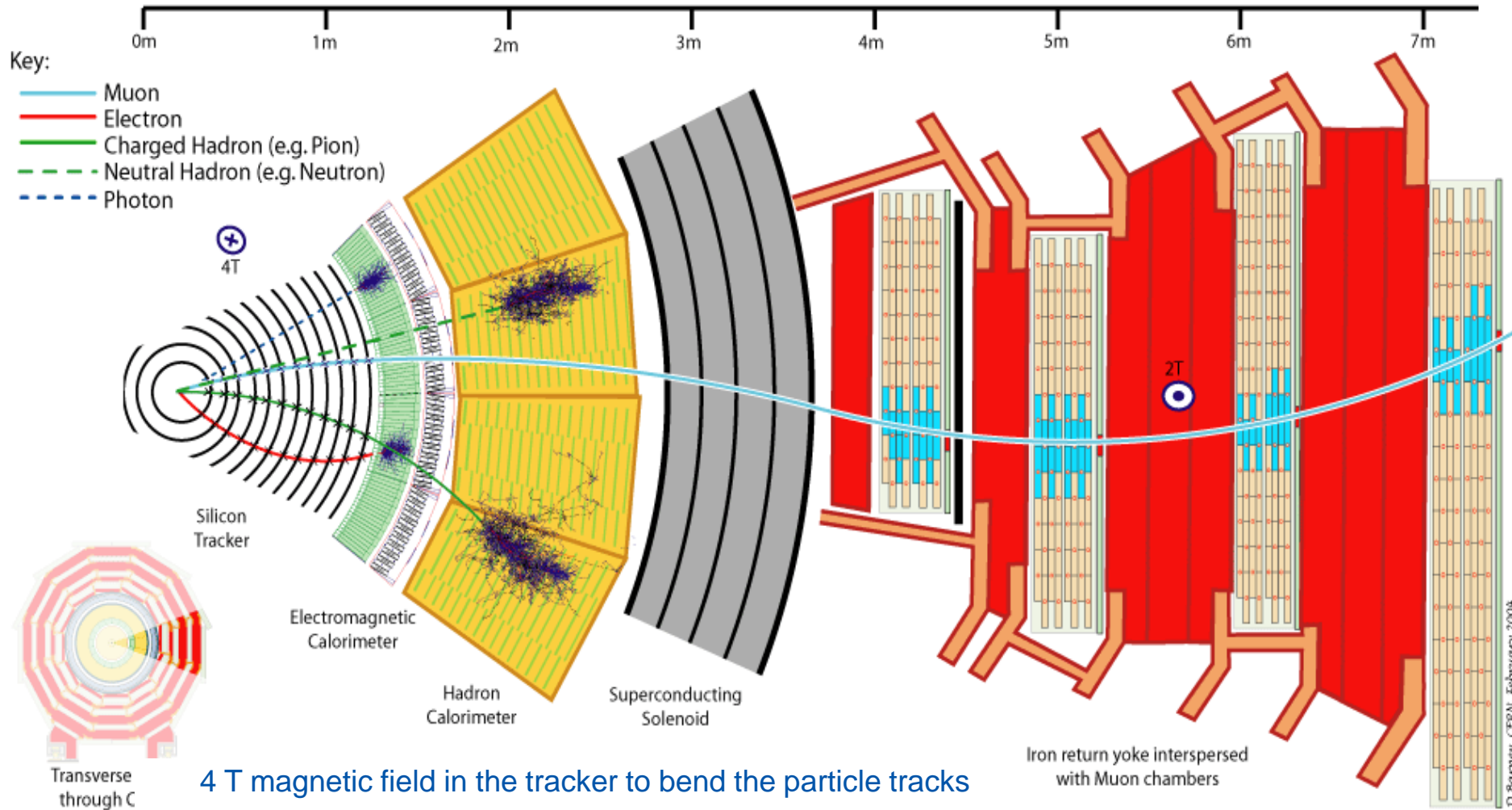
An international collaboration to distribute and analyse LHC data

Integrates computer centres worldwide that provide computing and storage resource into a single infrastructure accessible by all LHC physicists



US Dept of State Geographer
© 2013 Google
Image Landsat
Data SIO, NOAA, U.S. Navy, NGA, GEBCO

Google earth

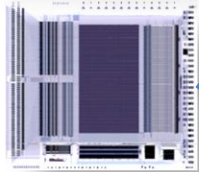




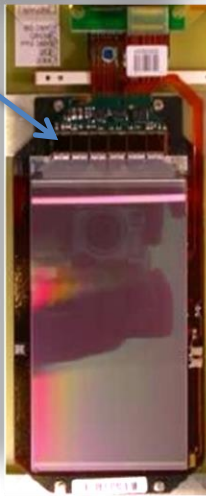
Microchips for Megastructures

On-detector ASIC

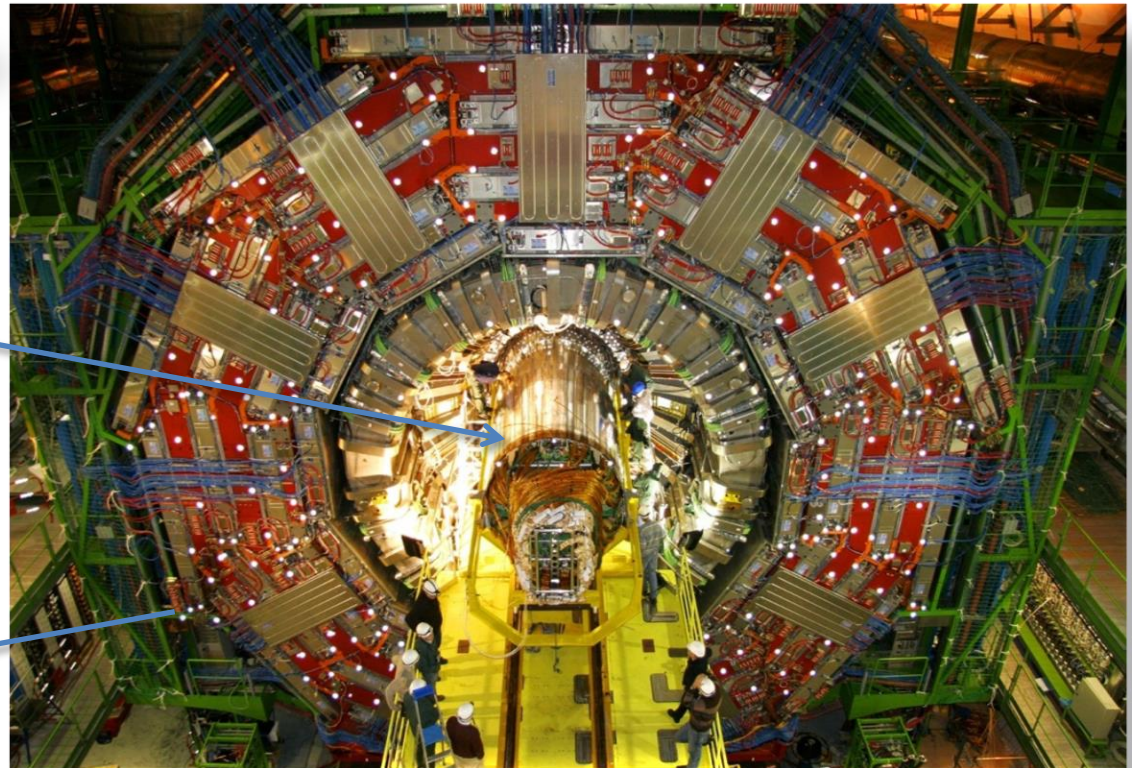
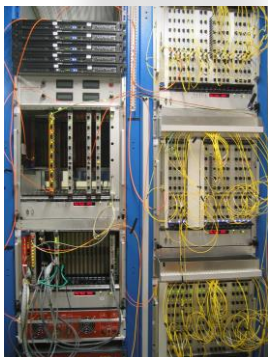
CMS experiment at the LHC accelerator at CERN



Silicon Tracker Hybrid



Off-detector electronics





ASICs for High Energy Physics

- Highly customized functionalities
 - Unique Signal Processing techniques
 - High Resolution and High Dynamic range

- Very high number of Readout Channels
 - Low power consumption

- Intense Radiation Environment
 - TID (Total Ionizing Dose) of 500 Mrads up to 1 Grad
 - Space applications requirements: up to 200 Krads
 - SEE (Single Event Effects)
 - Particle fluence $\sim 10^{15}$ cm⁻² (inner tracker layers)

Silicon Strip Detector electronics

Silicon-strip detector

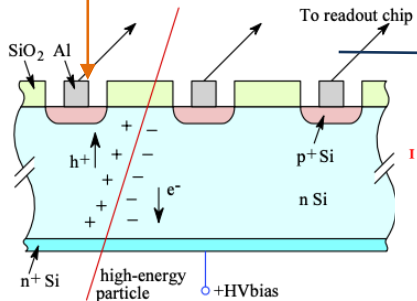
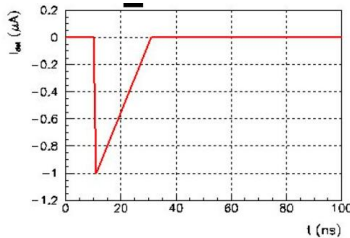
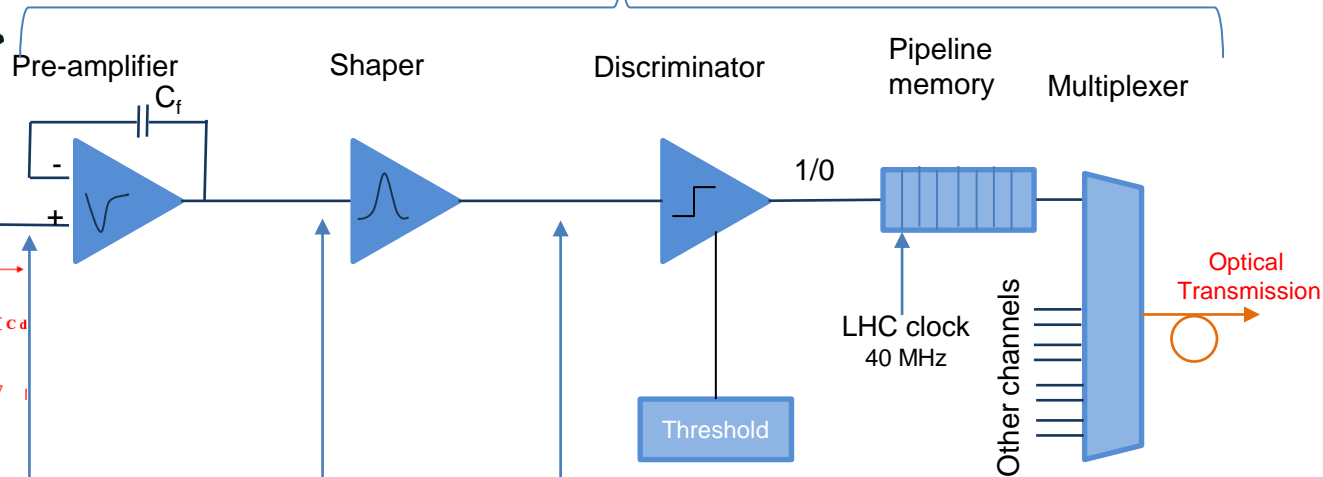
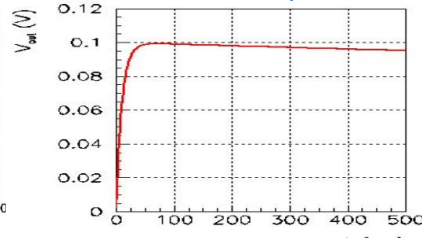


Fig.4: Schematic cross-section of a typical silicon strip detector.

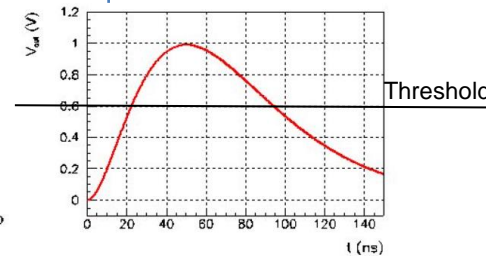
On-detector electronics ASIC (Application Specific Integrated Circuit)



Very small signal (~fC)
Needs amplification



Charge-sensitive amplifier
 $V = -Q/C_f$



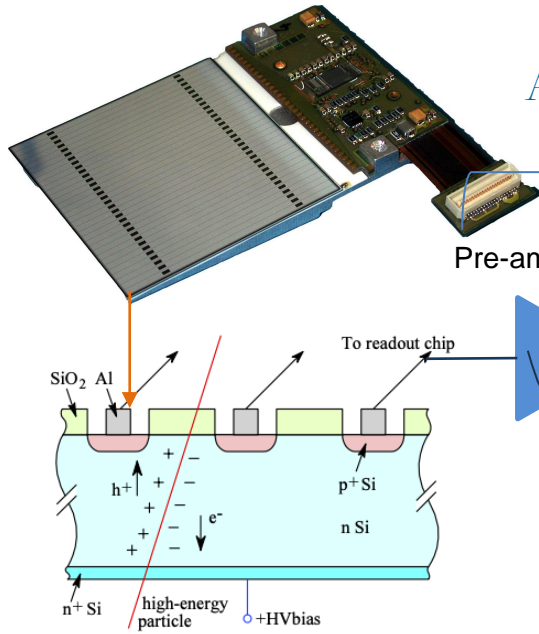
Predefined signal shape
Noise reduction by
optimizing useful bandwidth



Digitized signal (1/0)
Signal above a preset
threshold

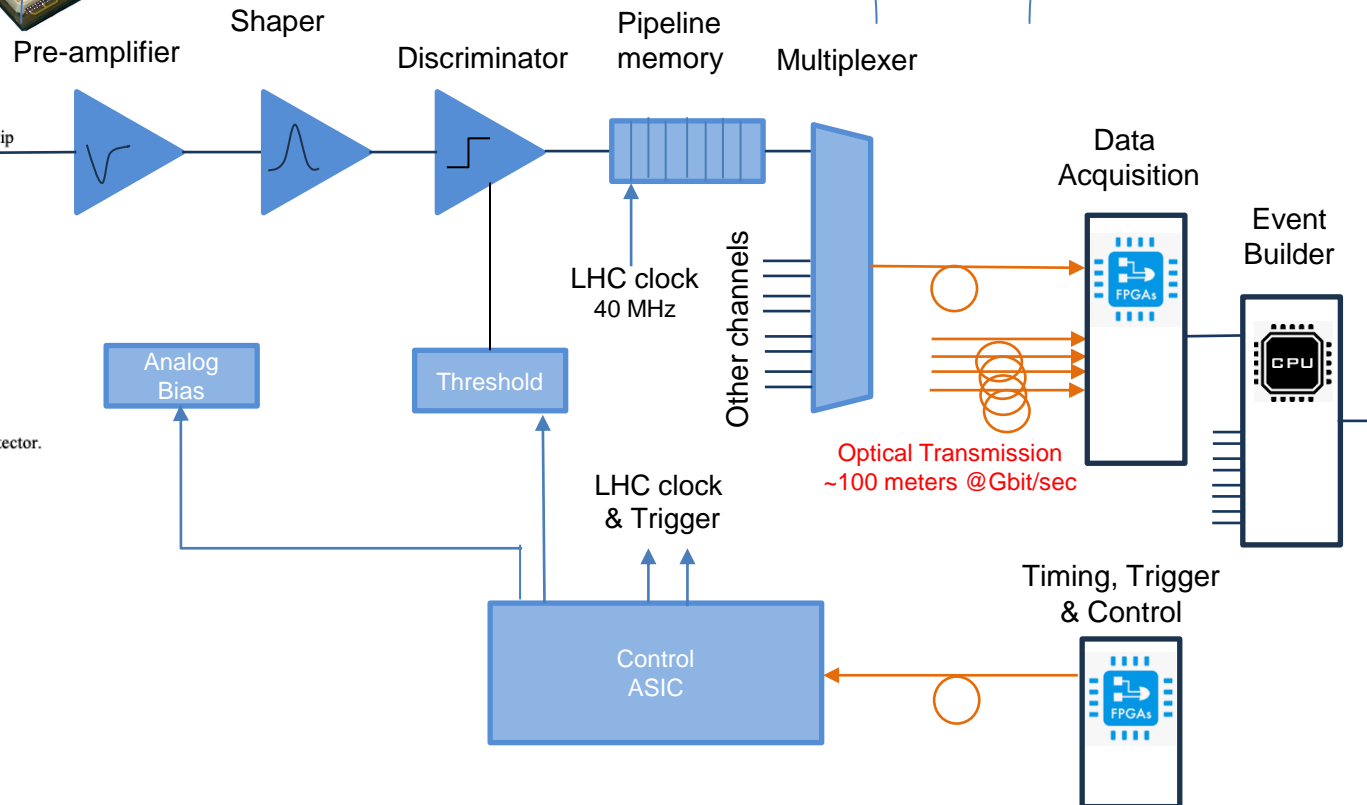
Readout of Silicon Strip Detectors

Silicon-strip detector



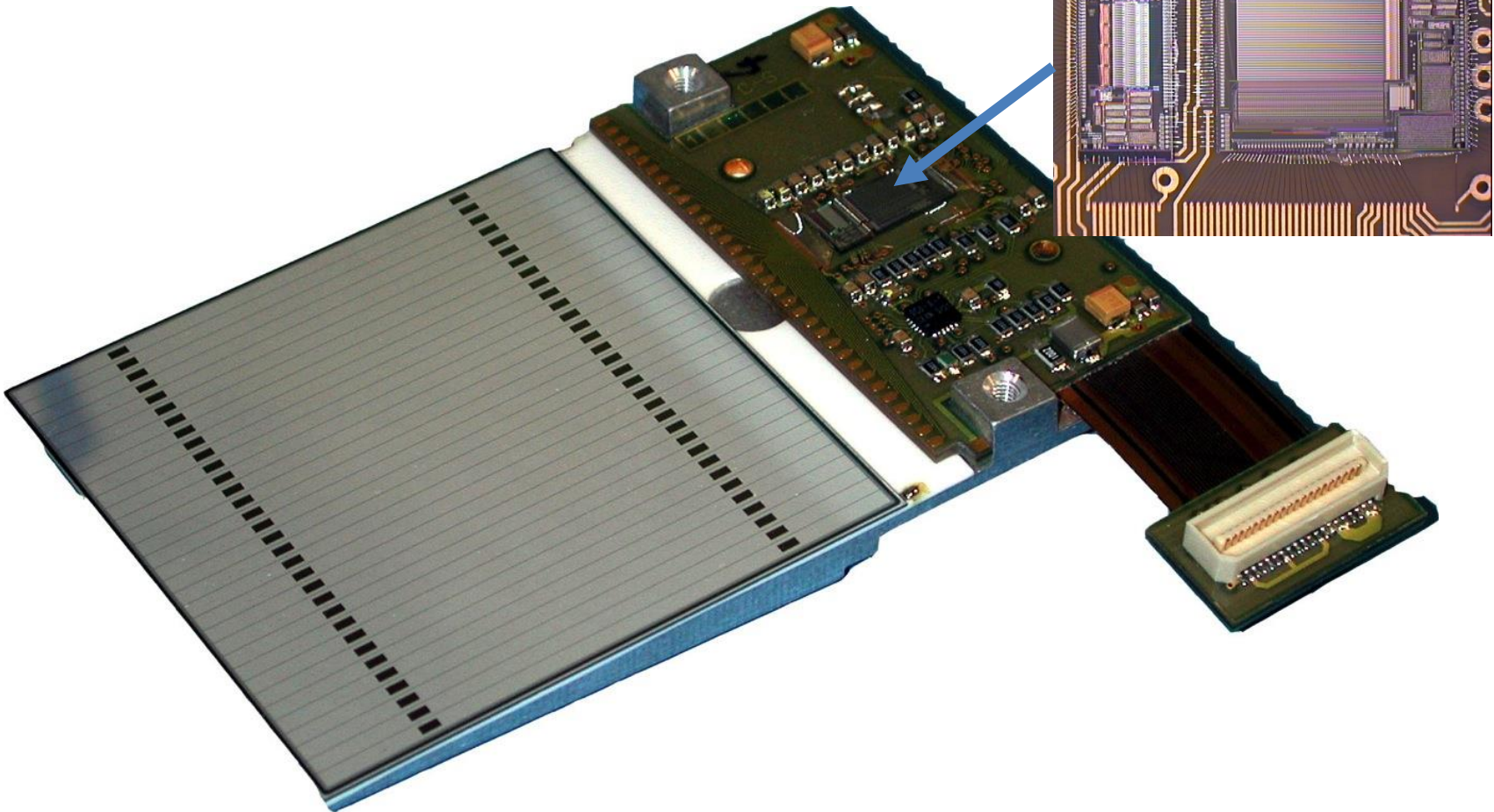
On-detector electronics ASIC (Application Specific Integrated Circuit)

Off-detector electronics

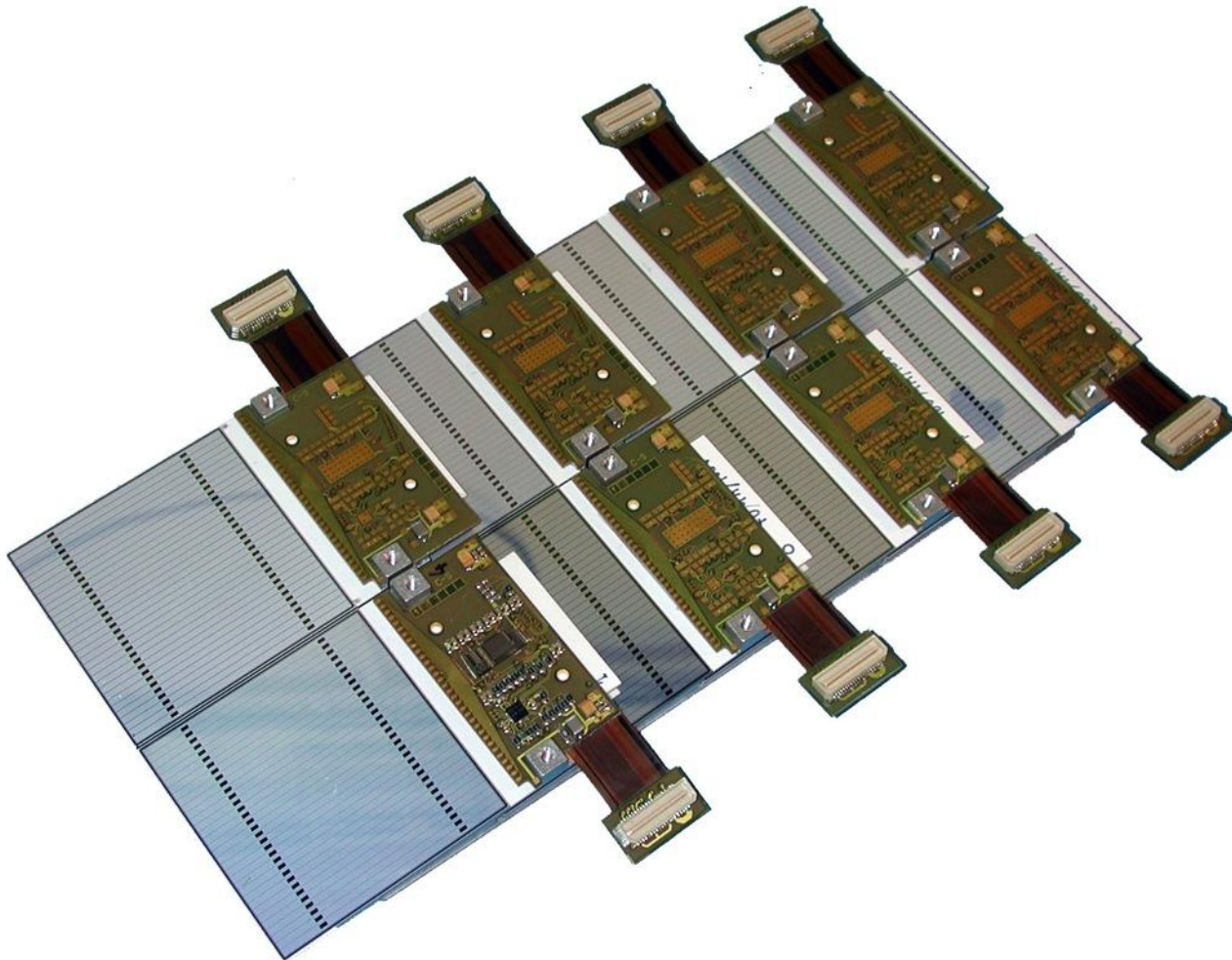


On-detector ASICs

ASIC (Application Specific Integrated Circuits)

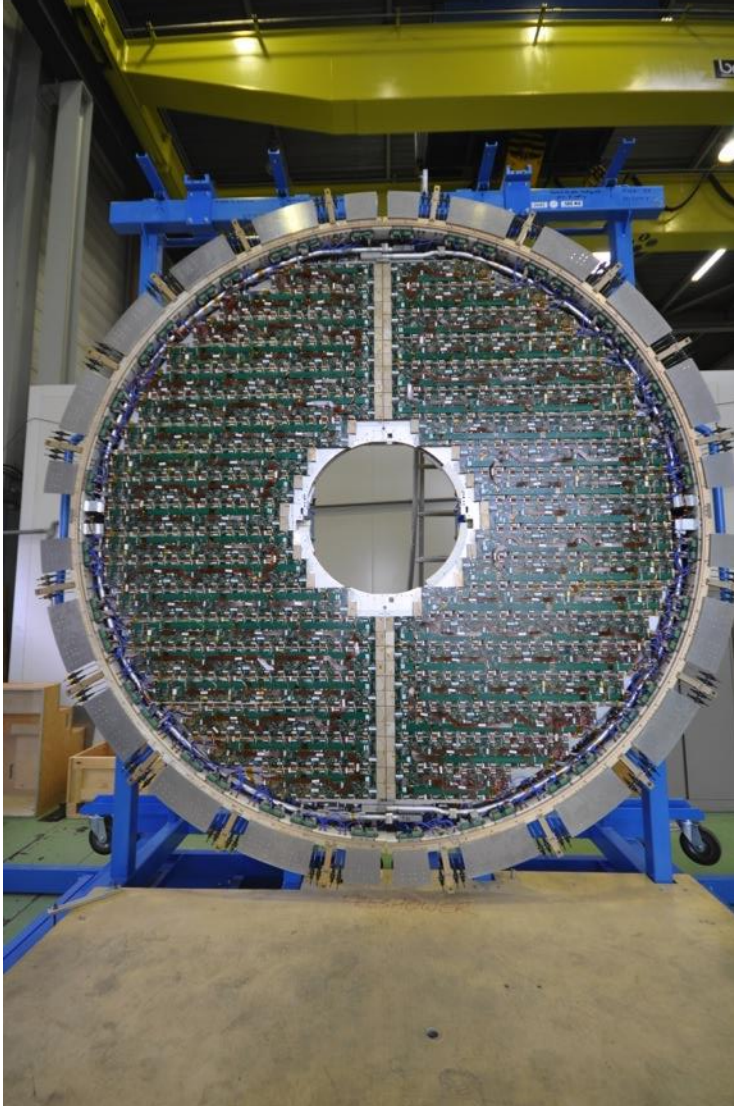


Sensor modules with ASICs

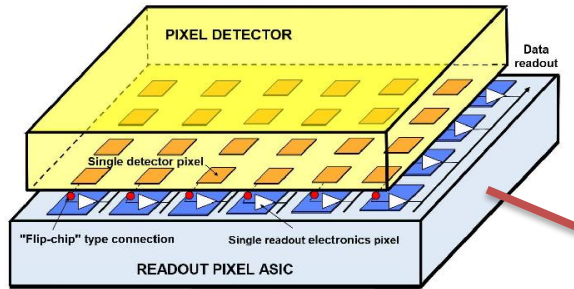




Detector Assembly

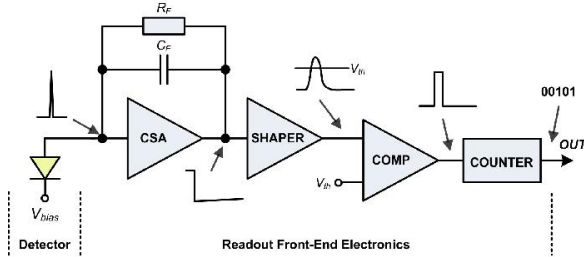


Pixel Detector electronics

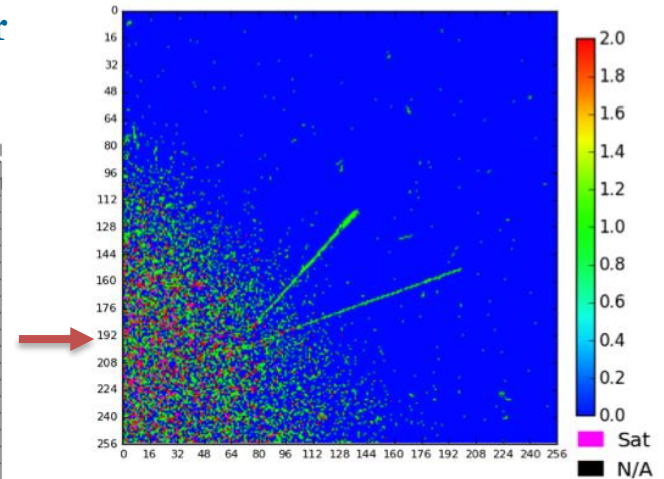
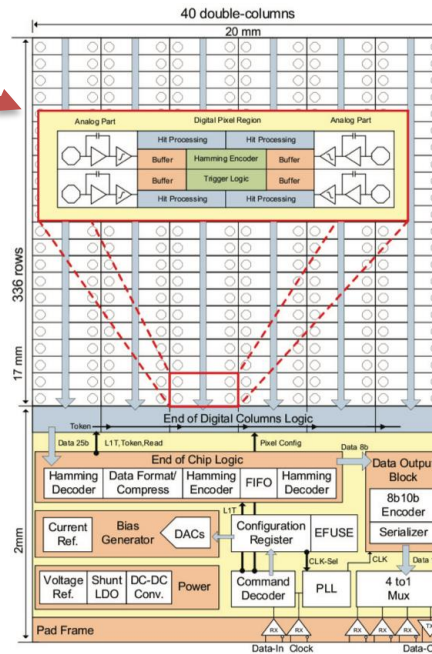


(a)

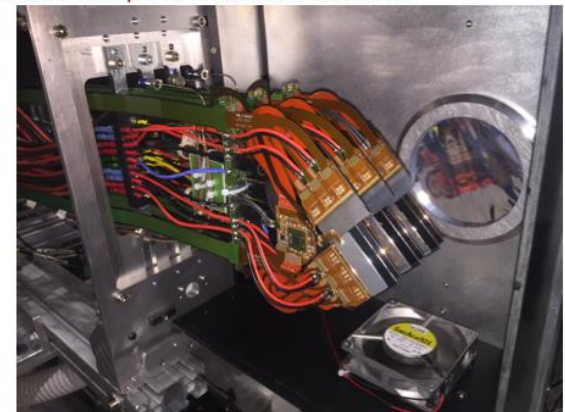
Velopix readout ASIC for the LHCb detector



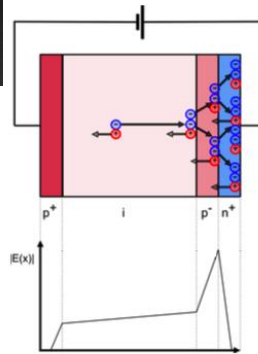
(b)



first data with proton beam over GWT link

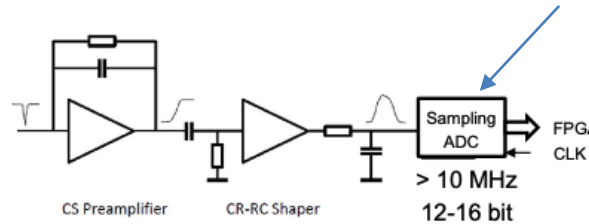


test setup with beam window



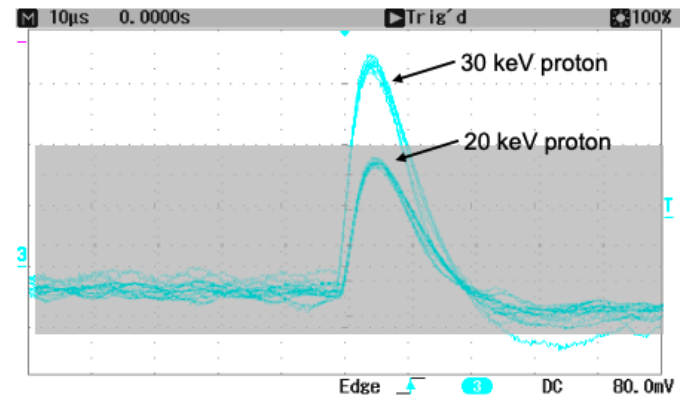
- Lead tungstate crystals
- Avalanche Photo-diodes
Reverse-biased p-n junction
- Primary photoelectrons accelerated in electric field → avalanche
- Generated charge is proportional to deposited energy

Analog to Digital Converter (ADC)

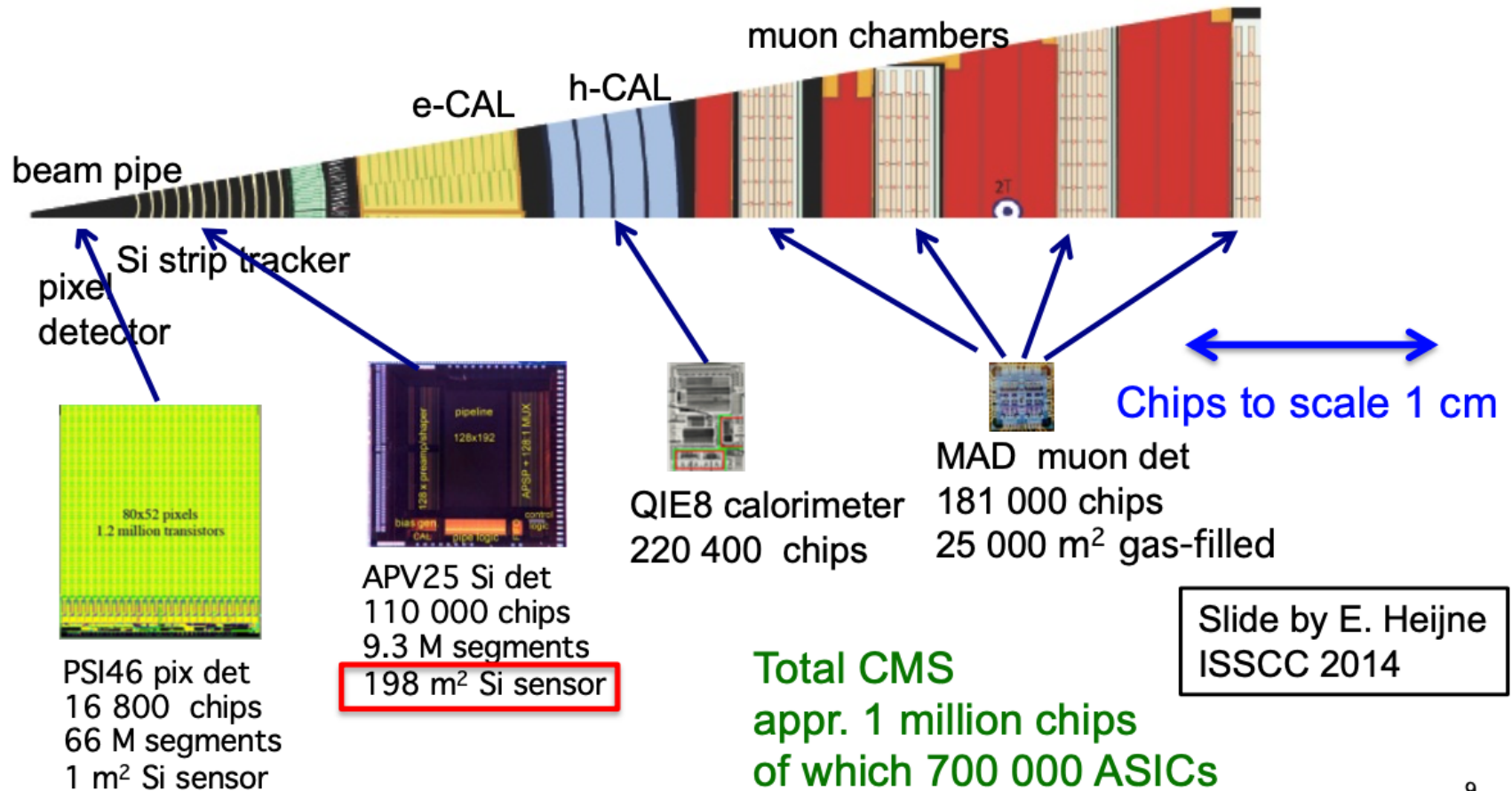


- Charge-sensitive (CS) preamplifier
- Shaping: CR differentiator and RC integrator

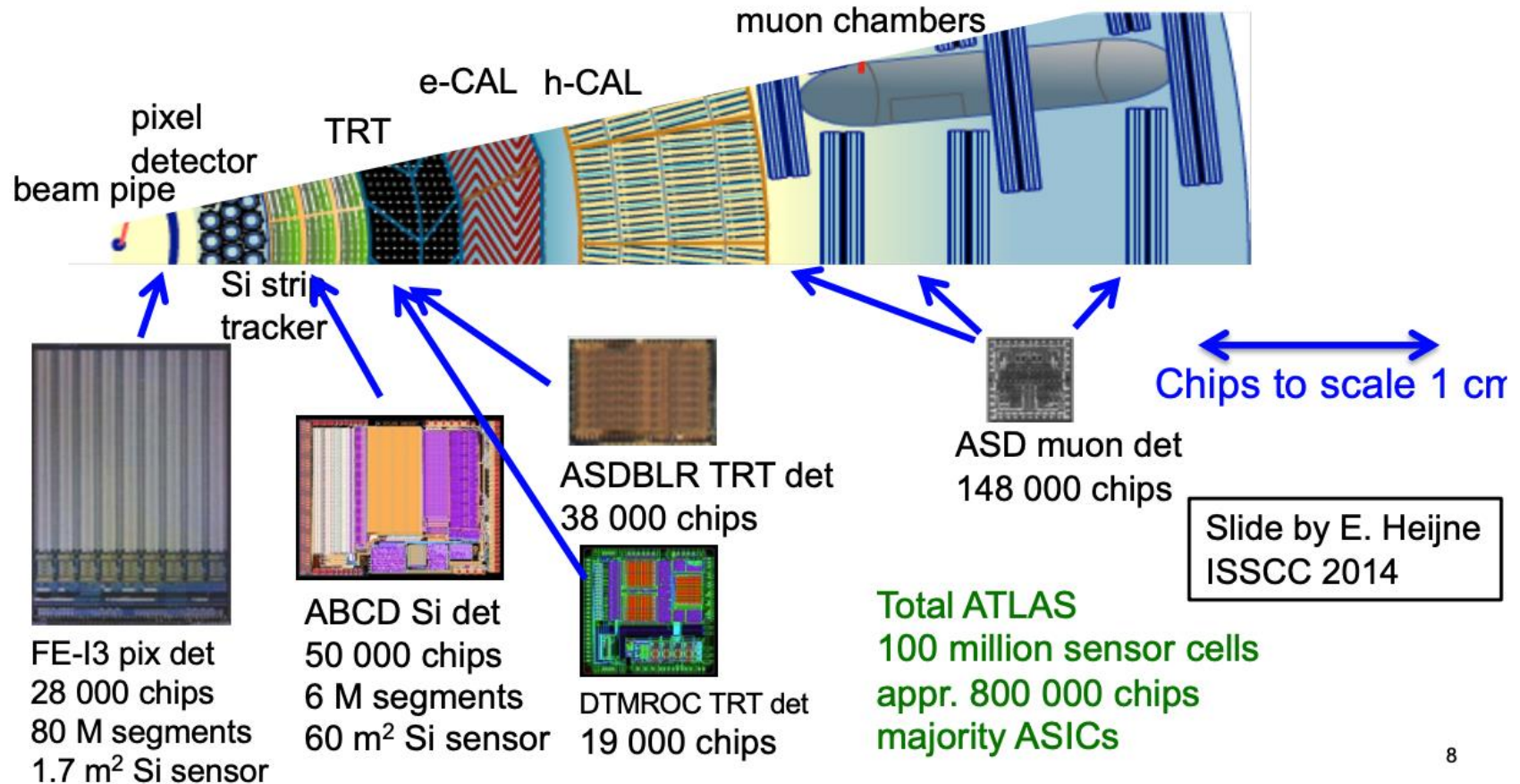
Created charge proportional to energy deposit
 ⇒ Amplitude measurement
 ⇒ Signal Time defines EVENT TIME

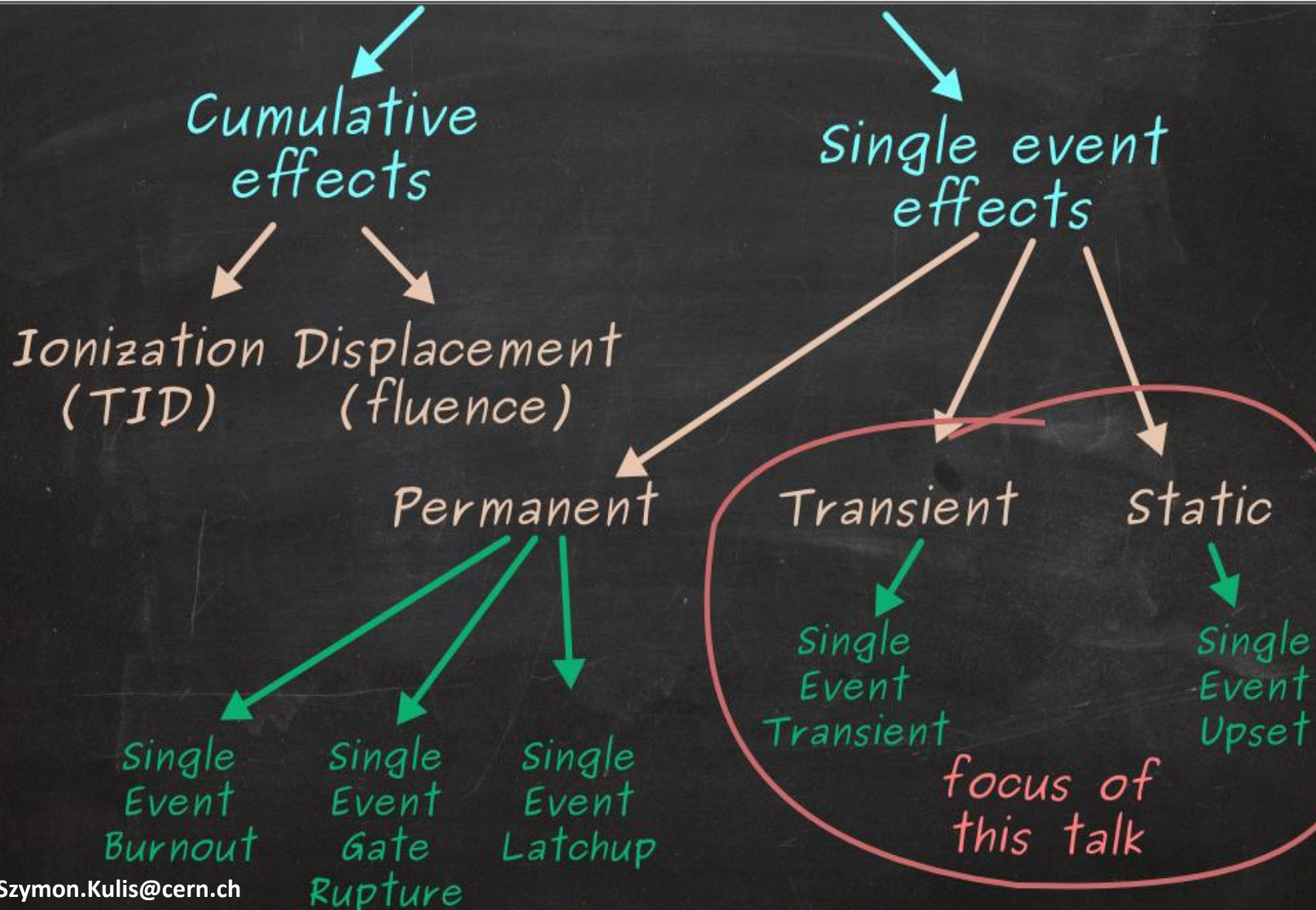


Some examples of ASICs in CMS

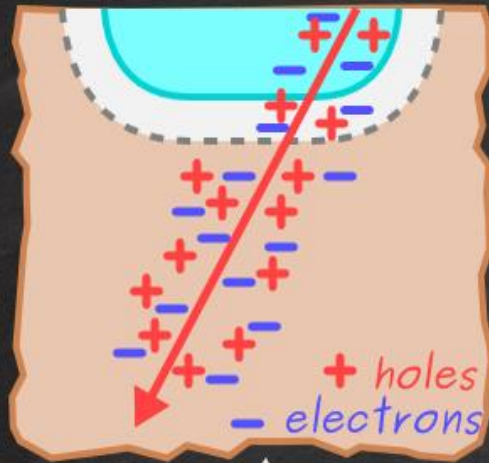


Some examples of ASICs in ATLAS

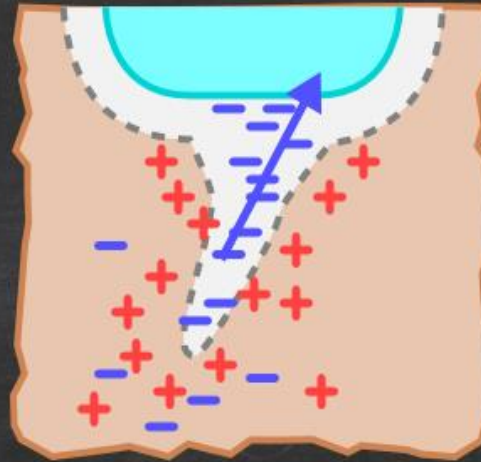




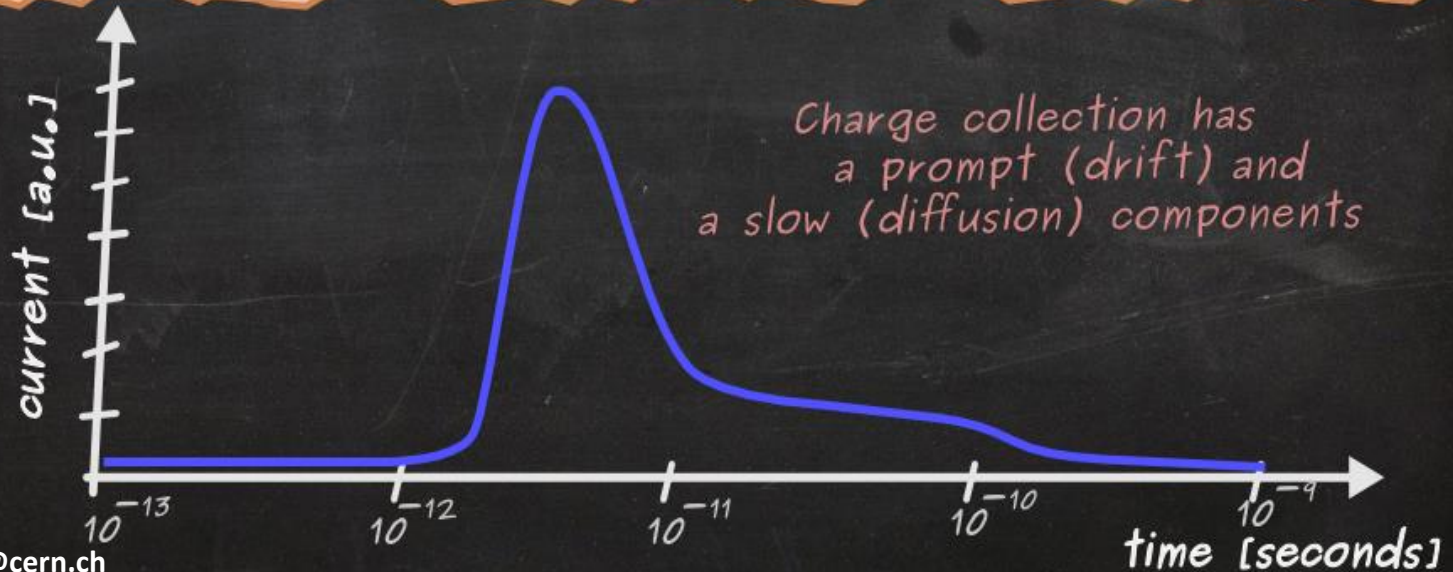
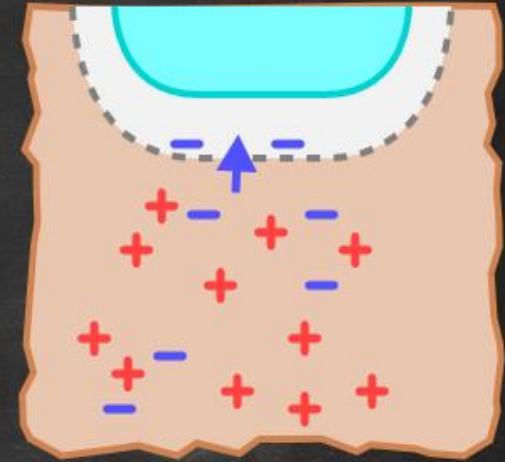
ionization ($t=0$)

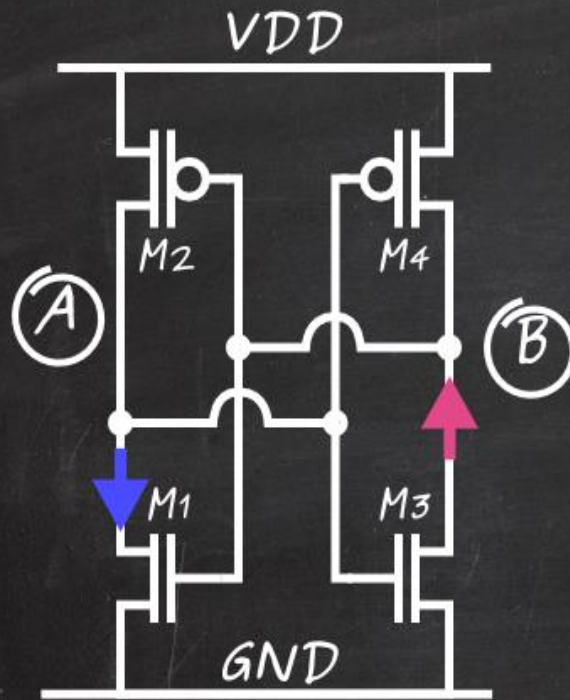


drift ($t=10ps$)



diffusion ($t=100ps$)



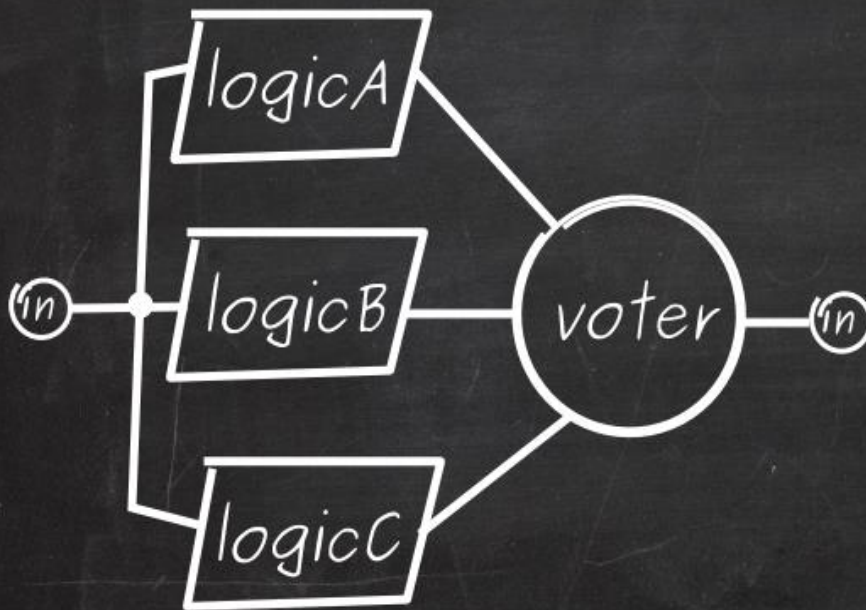


SRAM cell
(pass gates missing)

- 1) initial state : $A = VDD, B = GND$
- 2) charge deposited at drain of $M1$
- 3) transient current changes temporary the state of node A ($VDD \rightarrow GND$)
- 4) before the desposited charge is evacuated, the second inverter ($M3-M4$) switches (node B $GND \rightarrow VDD$)
- 5) The change of node B enforces the wrong state at node A \rightarrow the error is latched into the memory cell

How much charge is needed to flip the value?

Normally, the three blocks give the same output



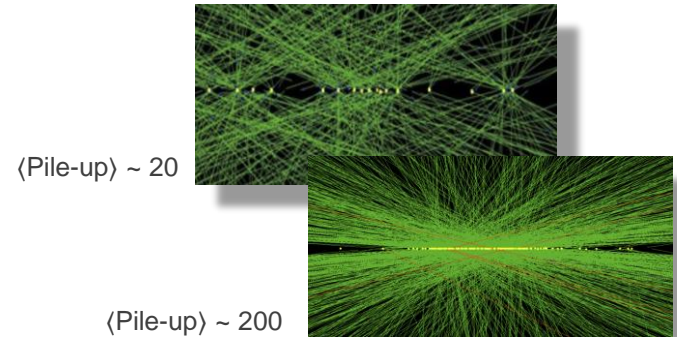
A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	1

voter truth table

CMS Phase-2 upgrade challenges

- **LHC → HL-LHC:** sustained luminosity of $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$

- From 20 → 200 pileup events per BX
- μ , e and jets at exceedingly high rates
 - Increasing thresholds would affect physics performance
 - Performance of algorithms degrades with increasing pile-up

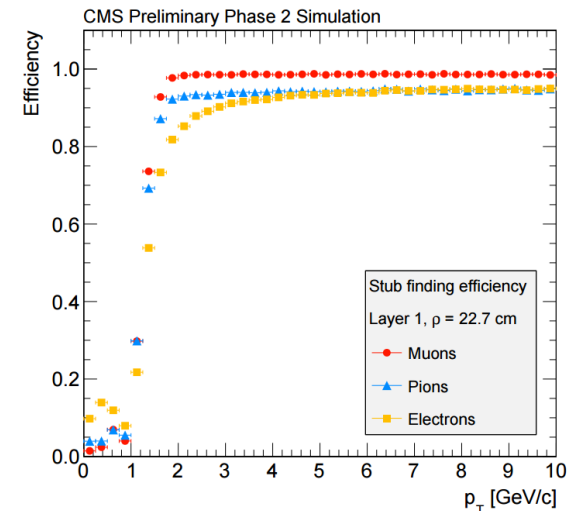


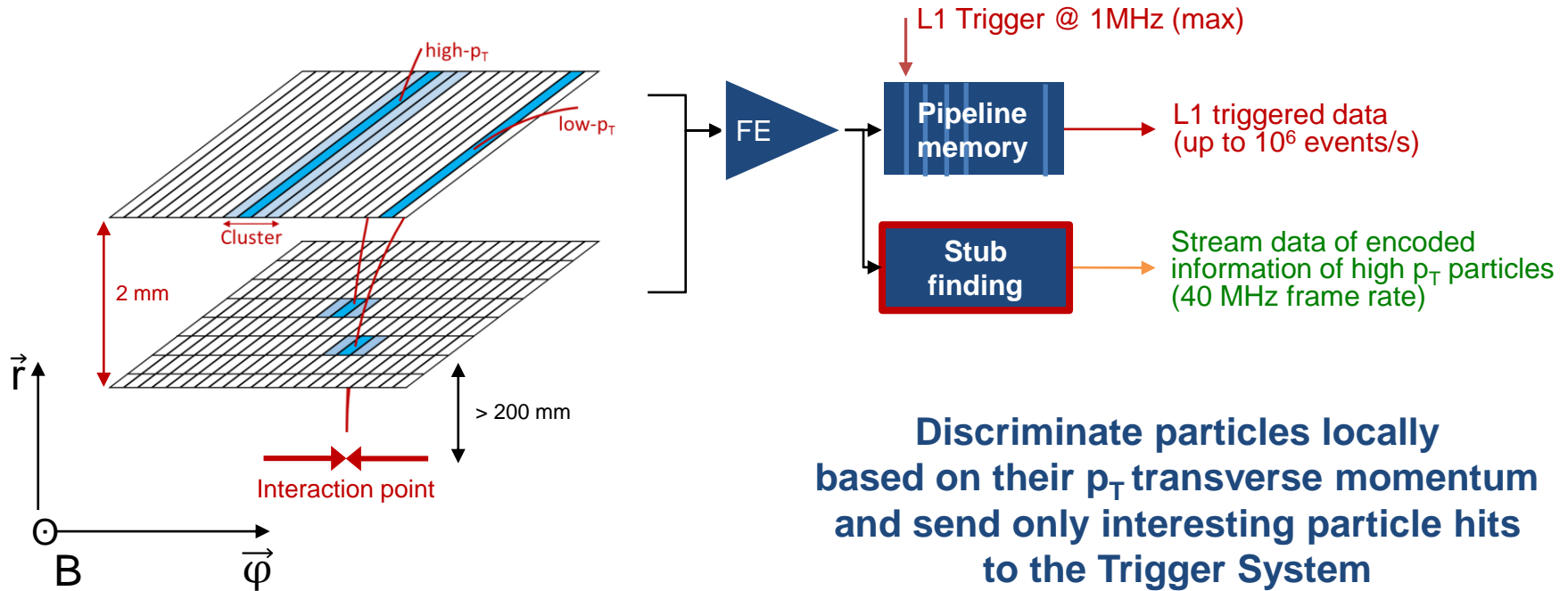
- **Track Triggering**

- Add tracking information to the Level-1 trigger decision to keep trigger rate at an acceptable level
 - Trigger Rate 100 kHz → 750kHz
 - Trigger Latency $3.2 \mu\text{s}$ → $12.5 \mu\text{s}$

- **Outer Tracker modules with p_T discrimination**

- Reject locally signals from low- p_T particles ($< 2\text{GeV}$)
- Reduce data volume by one order of magnitude making transmission feasible for the available power budget
- Simplify track finding algorithms





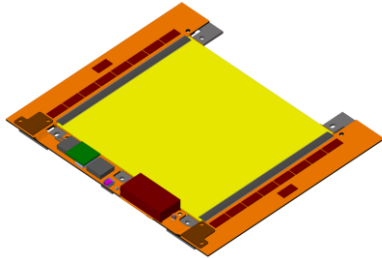
3.8T provided by the superconducting solenoid

- The CMS OT detector working principle of p_T discrimination
 - Exploit the strong magnetic field of CMS
 - Correlate signals between two closely spaced sensors to identify “stubs”
 - Stubs defined as a track coordinate + angle based on tracking window on parallel sensor
 - Transmit stub coordinates and momentum instead of a multiplicity of hits

Phase 2 CMS Outer Tracker

2S or Strip-Strip module

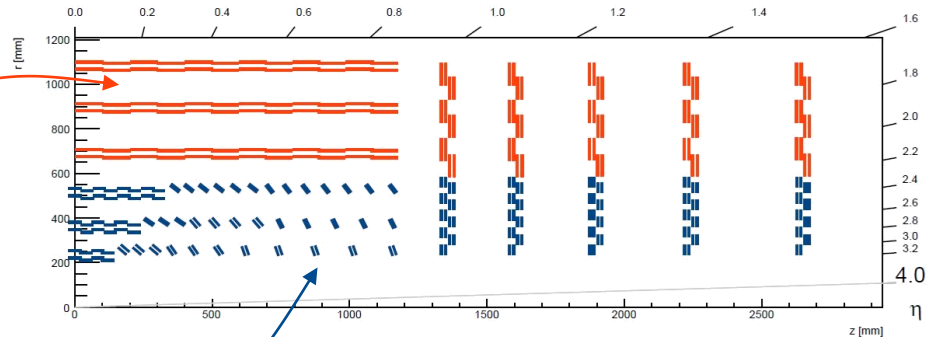
Outer Barrel



2 Strip sensors

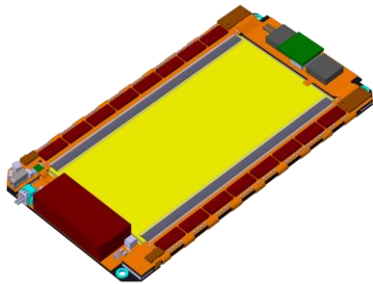
No strips: 2x 2 048 per side
 Strip size: 5 cm x 90 μ m
 Spacing: 1.8 mm and 4.0 mm
 Active area: 2 x 90 cm²
 Total 2S modules:.... 8 424

Phase 2 Outer Tracker Layout



PS or Pixel-Strip module

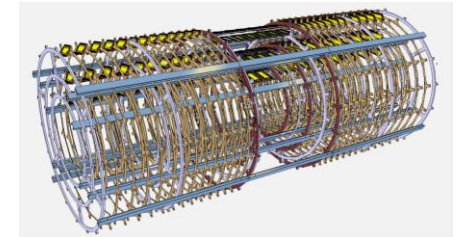
Inner Barrel



Pixel + Strip sensor

No strips: 2 x 960 = 1 920 strips
 Strip size: 2400 mm x 100 μ m
 No pixels: 32 x 960 = 30 720 pixels
 Pixel size: 1.5 mm x 100 μ m
 Spacing: 1.6 mm, 2.6 mm and 4.0 mm
 Active area: 2 x 45 cm²
 Total PS modules:.... 5 708

13 296 Modules
 44 Mstrips + 174 Mpixels
 200m² of silicon area

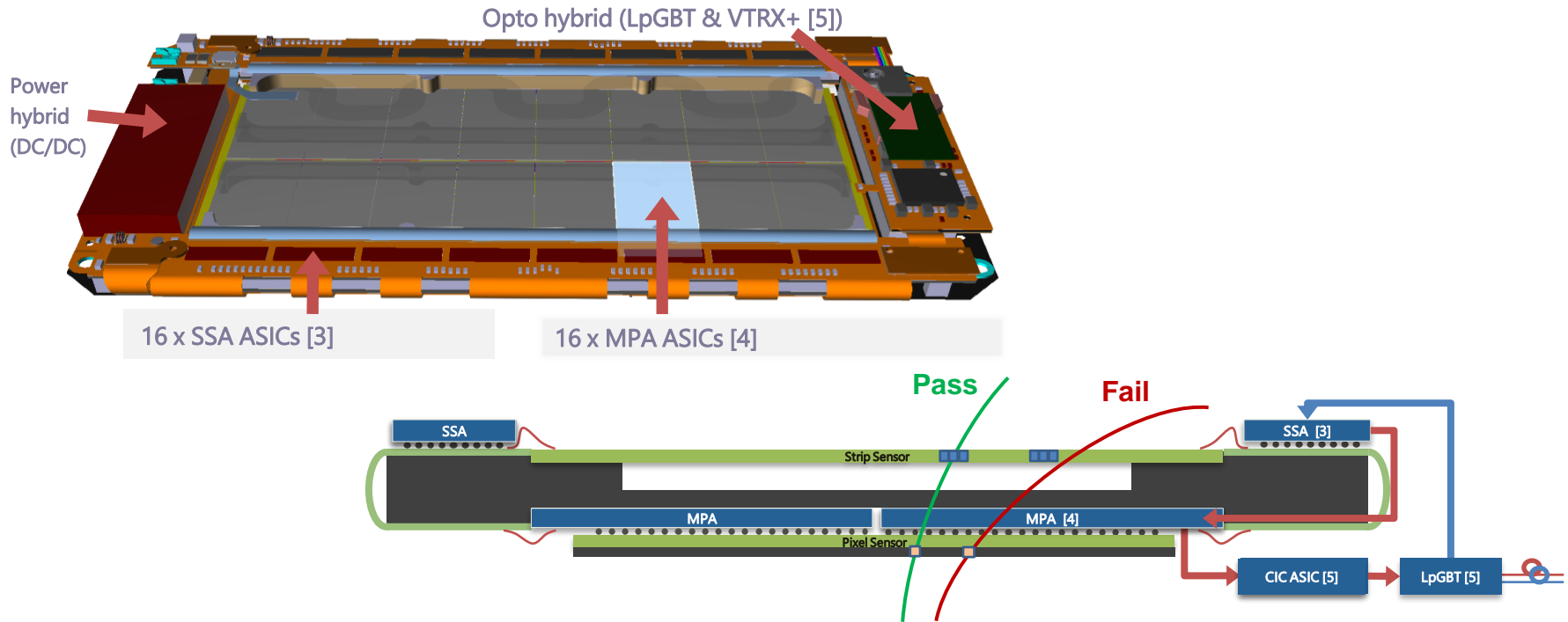


Power density: < 100 mW/cm²

[1] CMS collaboration. "The phase-2 upgrade of the CMS tracker." CMS-TDR-014 (2017).

[2] Abbaneo, Duccio. "Upgrade of the CMS Tracker with tracking trigger." Journal of Instrumentation 6.12 (2011): C12065.

The Pixel-Strip (PS) module



- **Readout ASIC chipset**

- **MPA:** Macro Pixel ASIC for Pixel sensor Readout
- **SSA:** Short Strip ASIC for Strip sensor Readout
- **CIC:** Concentrator ASIC for data aggregation and transmission through optical gigabit link

[3] Caratelli, Alessandro, et al. Characterization of the first prototype of the Silicon-Strip readout ASIC (SSA). No. CMS-CR-2018-286. 2018.

[4] Ceresa, Davide, et al. Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities. No. CMS-CR-2018-279. 2018.

[5] Moreira, Paulo. "The LpGBT project status and overview." ACES. 2016.

[6] Nodari, Benedetta, et al. A 65 nm data concentration ASIC for the CMS outer tracker detector upgrade at HL-LHC. No. CMS-CR-2018-278. 2018.

■ Design Teams

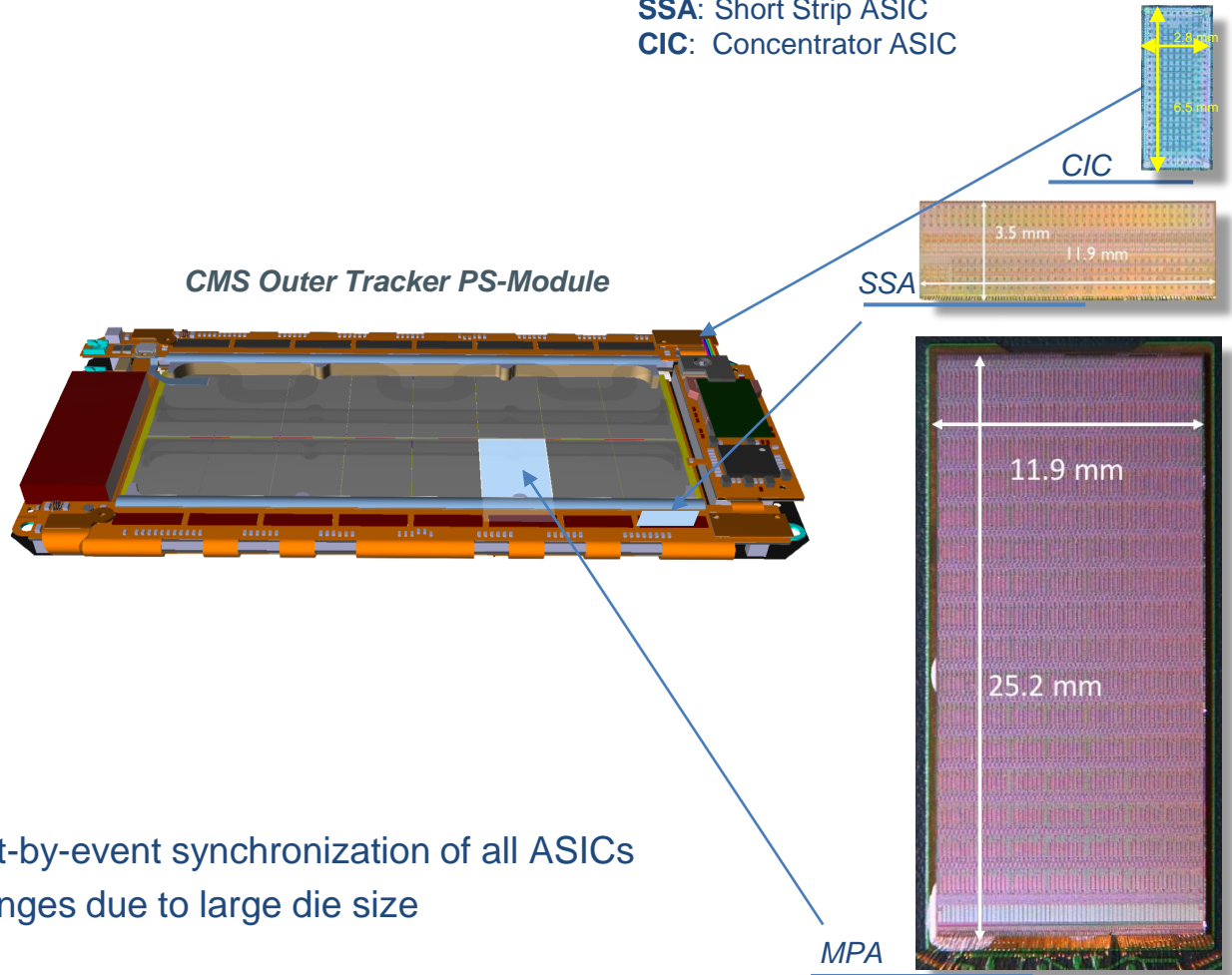
- **CERN (MPA, SSA, CIC)**
 - Alessandro Caratelli
 - Davide Ceresa
 - Jan Kaplon
 - Gianmario Bergamin
 - Kostas Kloukinas
 - Simone Scarfi

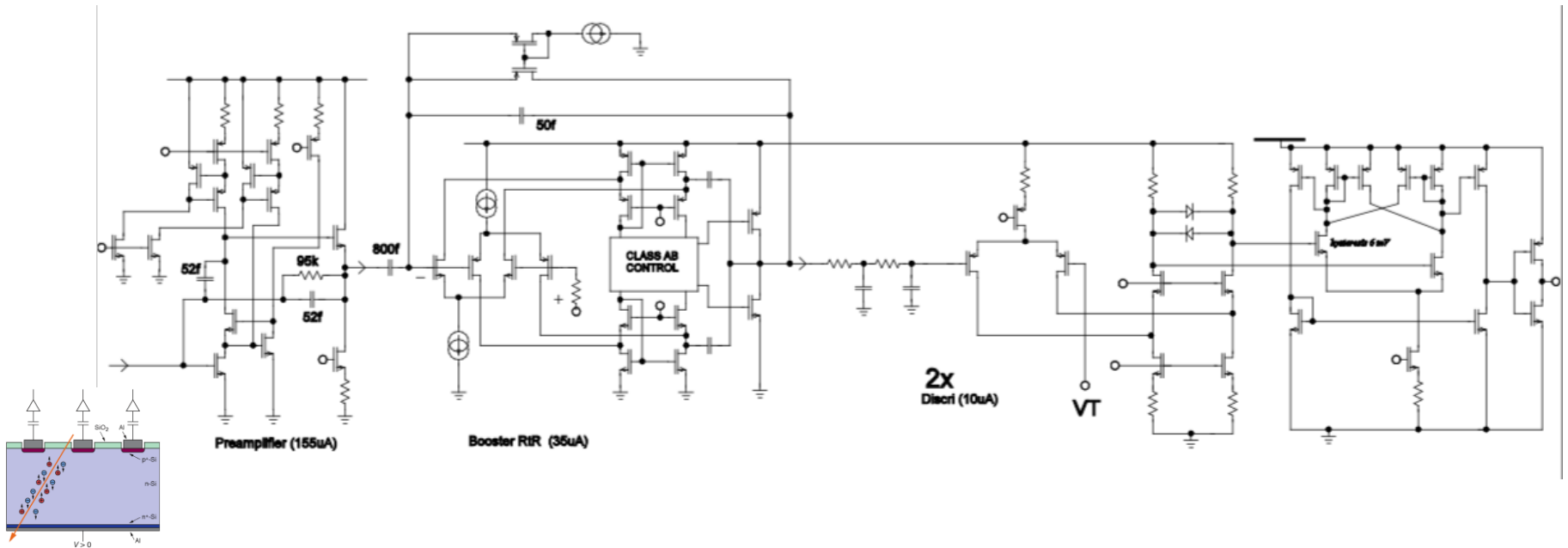
- **Lyon IPNL/IN2P3 (CIC)**
 - Luigi Caponetto
 - Geoffrey Galbit
 - Benedetta Nodari
 - Sebastian Viret

■ Challenging project

- Interoperability and event-by-event synchronization of all ASICs
- MPA ASIC design challenges due to large die size
- Low Power consumption

MPA: Macro Pixel ASIC
SSA: Short Strip ASIC
CIC: Concentrator ASIC





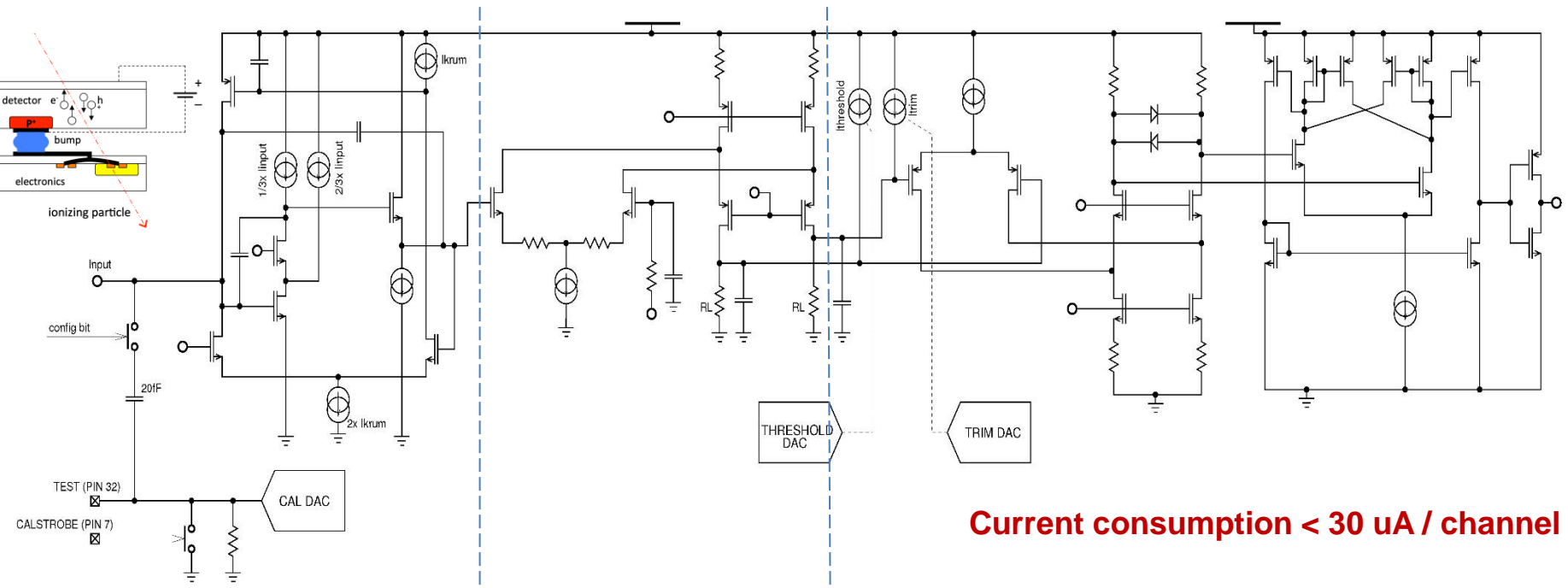
- Schematic design of the analog channel

- ❑ **Preamp:** regulated cascode transimpedance amplifier
- ❑ **Booster:** class AB buffer with active feedback for overshoot attenuation
- ❑ **3 stage discriminator**, folded cascode with resistive feedback (Discriminator for HIPs not shown)

Design parameters

Peaking time:	17 ns
Gain:	60 mV/fC
GBP:	2.7 GHz
ENC (5 pF input):	< 800 e ⁻
Max consumption:	250 μA

Designer: Jan Kaplon



Current consumption < 30 uA / channel

Pre-amplifier

Transimpedance Preamplifier with Krummenacher feedback leakage current compensation for n⁺ on p⁻ detectors

Shaper

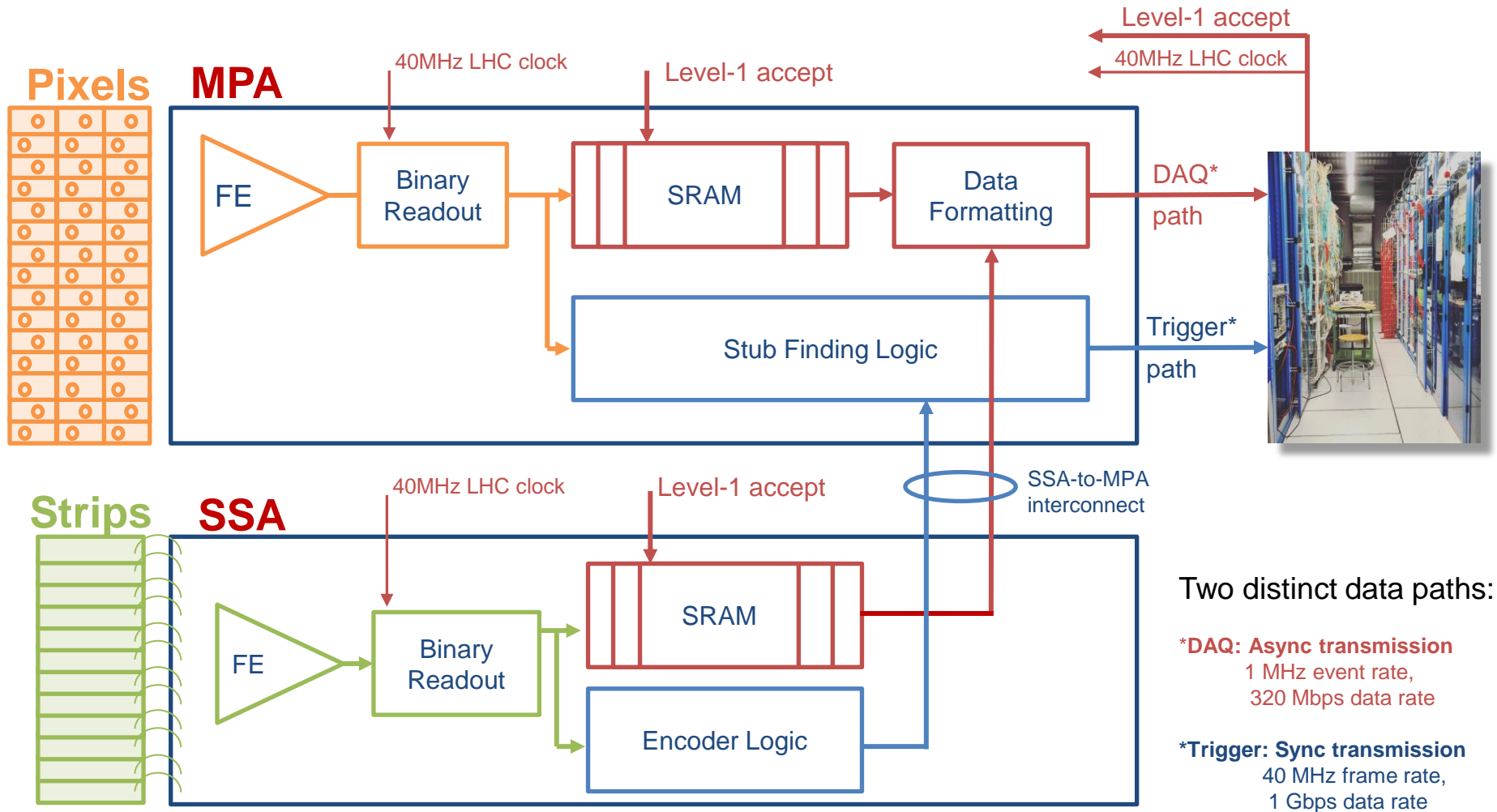
Single-ended to differential folded cascode stage with resistive load

Discriminator

- PMOS folded cascode input
- Swing limiter based on PMOS working in diode configuration
- Second stage with hysteresis (6mV)

Designer: Jan Kaplon

MPA-SSA Readout Concept



- Two full mask-set Engineering Runs on a 9-metal 65nm bulk CMOS process
- Prototype designs were tested
 - at die-on-board assemblies using custom made (FPGA based) test benches
 - at wafer level using a probe station at CERN
- Test routines include:
 - Scan-chain test for production defects
 - Functional test of digital circuits
 - Analog bias parameter characterization
 - Front-end characterization
 - Noise analysis
 - Serial ID and trimming in e-fuses



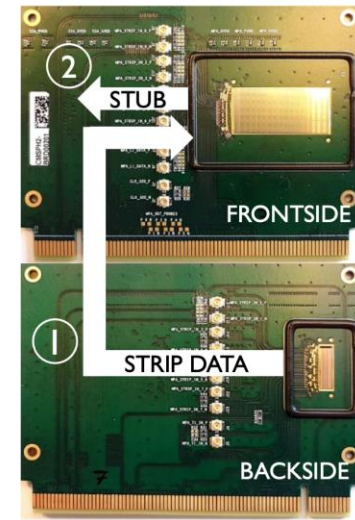
MPA prototype characterization

MPA and SSA first prototypes were proved functional and within specs...

FE results

- ENC < 200 e⁻
- Peaking time ~ 25 ns
- SNR >> 20
- Time walk < 15 ns
- Threshold 0.5 fC ~ 3120 e⁻

STUB GENERATION



POWER CONSUMPTION

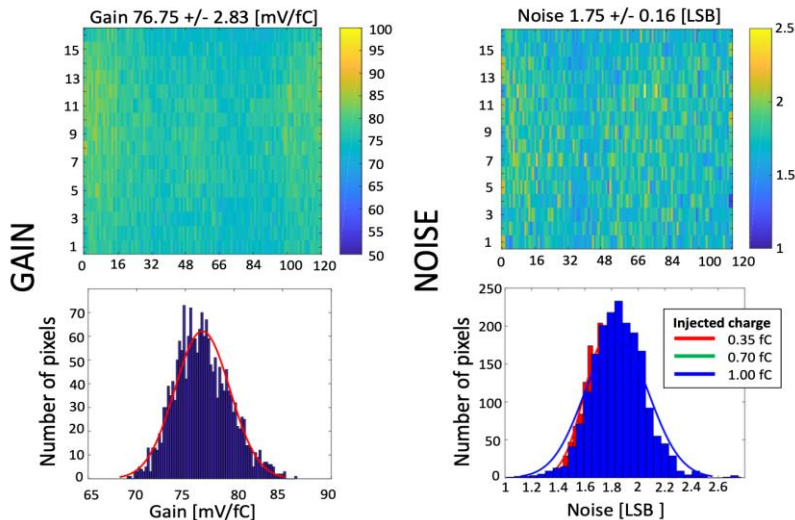
Configured w/o activity:

MPA: 184 mW
SSA: 67 mW

Increase w/ activity:

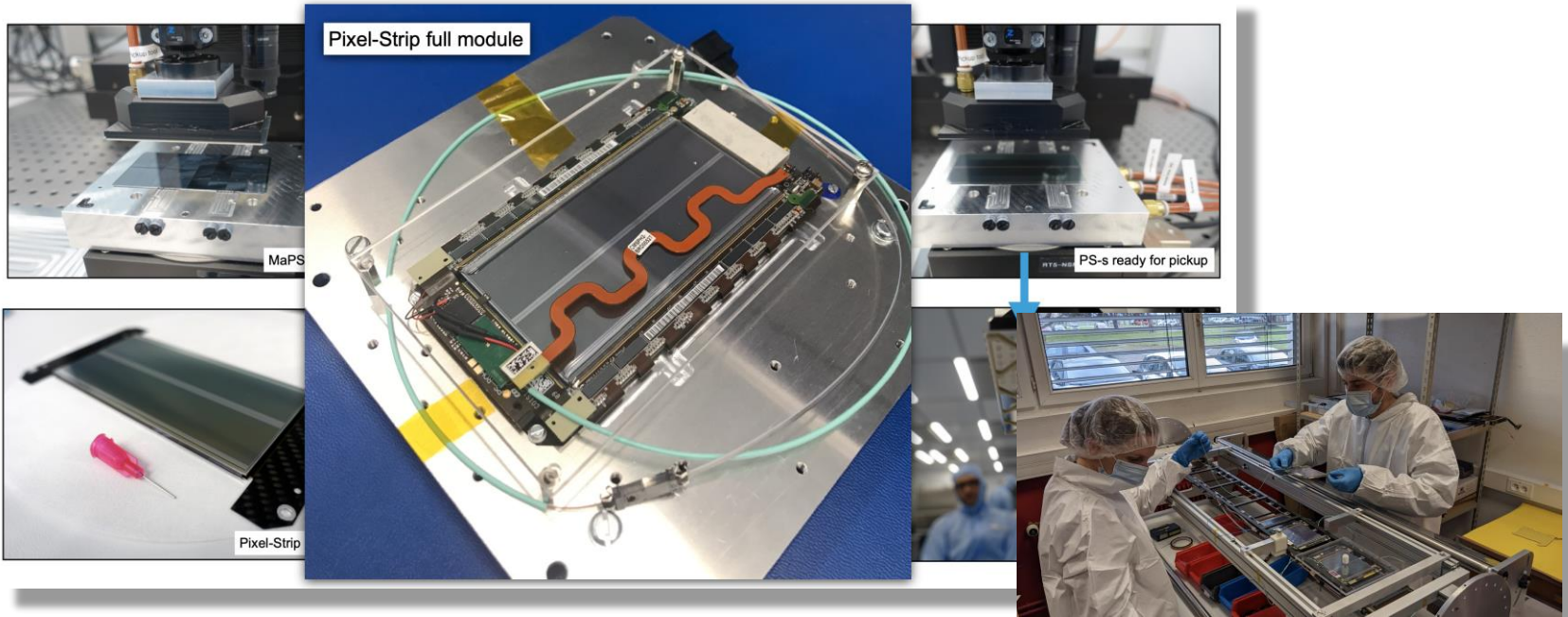
MPA: < +10 mW
SSA: < +2 mW

MAX power < 275 mW



Proved the feasibility of quick and on-chip particle discrimination

PS Module assembled

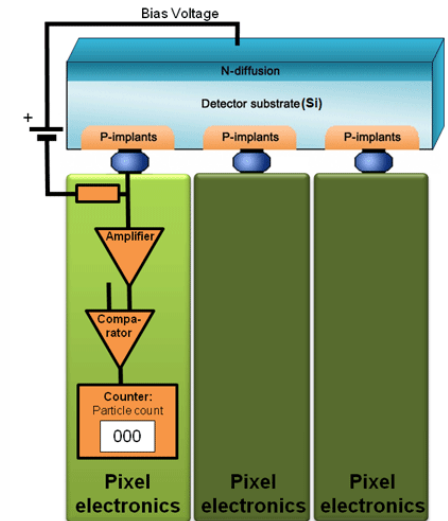
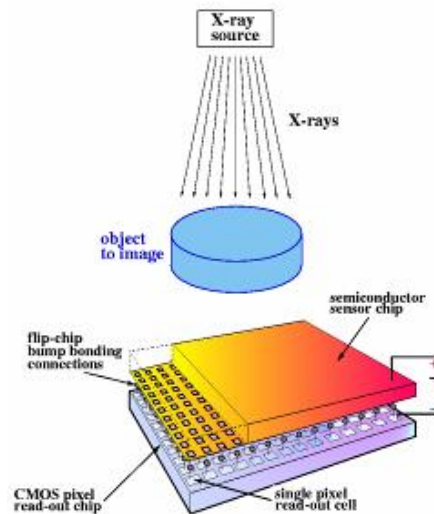
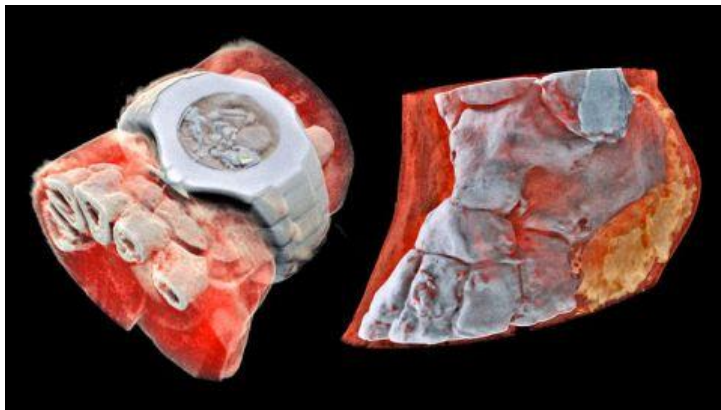
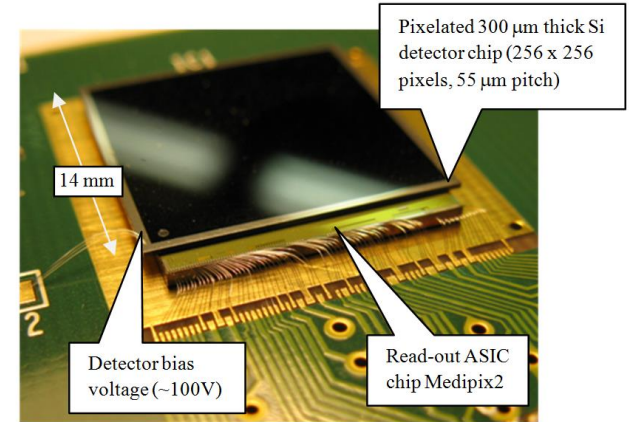


Pixel Sensors in Medical Imaging

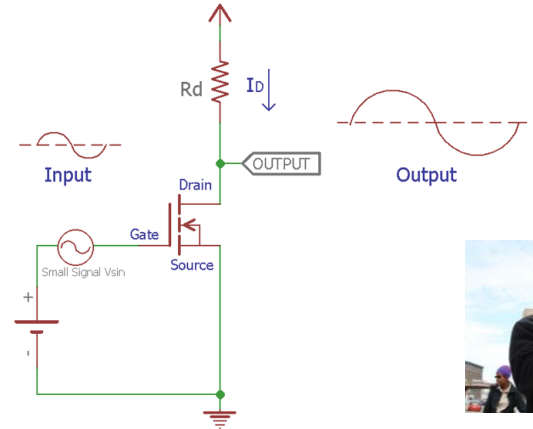
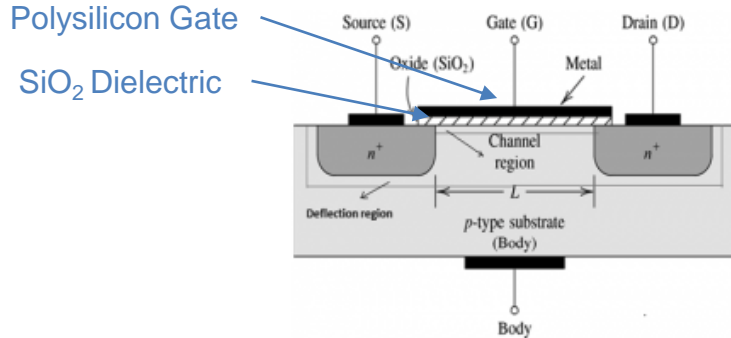
New X-ray technology produces striking 3D images in full colour

A new medical imaging device uses technology developed by particle physicists to produce full colour, 3D images of the human body.

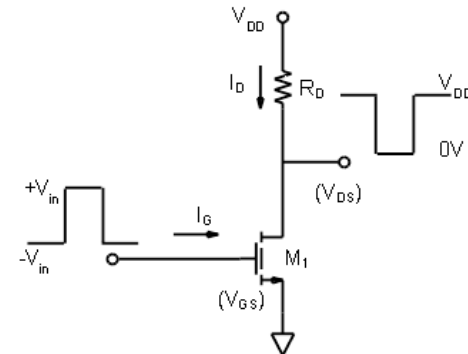
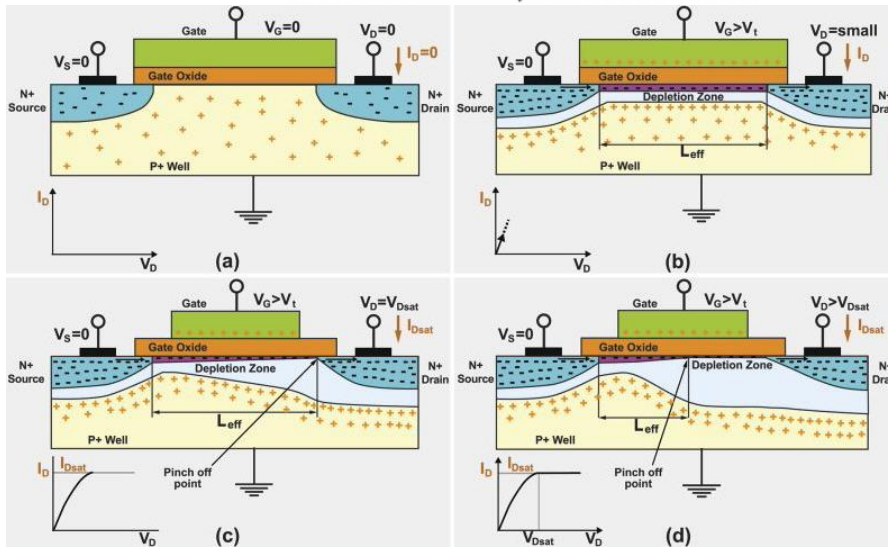
A hybrid detector capable of counting each individual particle hitting the pixels and measure its energy.



MOSFET : Metal Oxide Field Effect Transistor



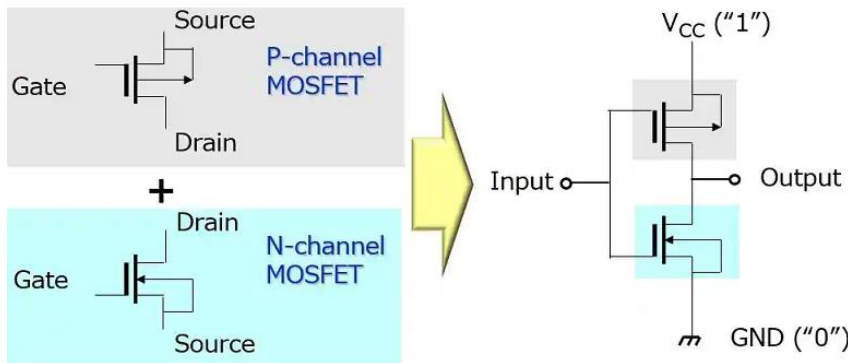
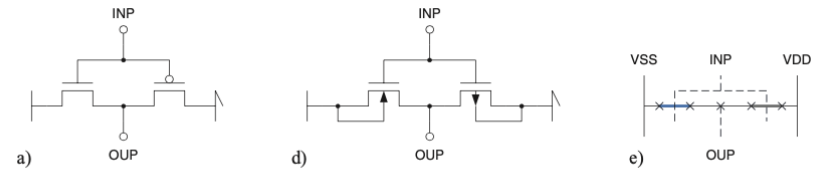
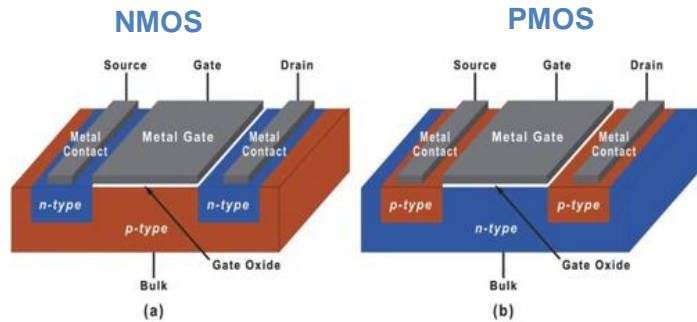
NMOS FET as an amplifier in Analog circuits



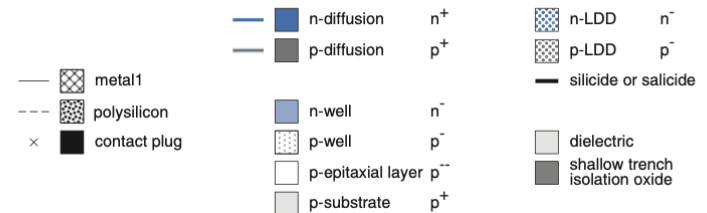
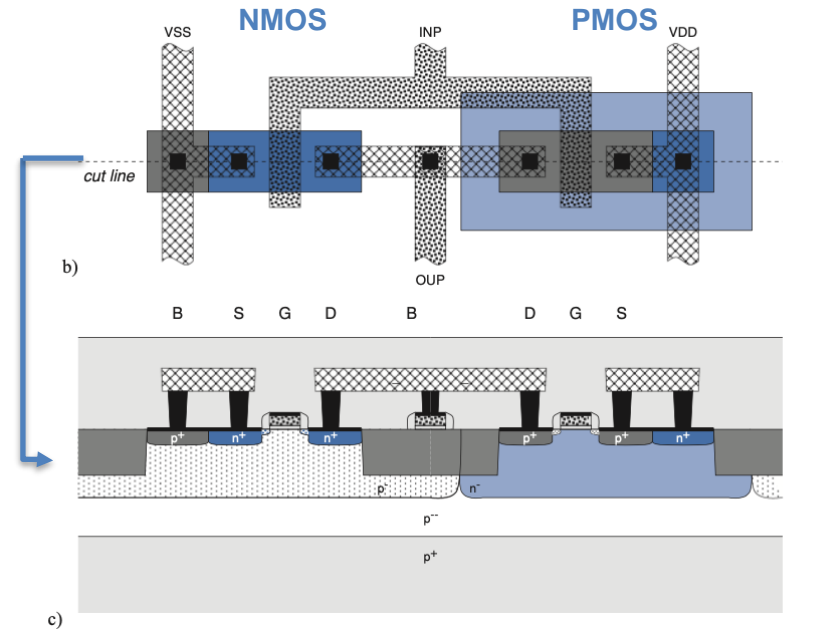
NMOS FET as a switch in Digital circuits

CMOS Transistors

CMOS : Complementary Metal Oxide Field Effect Transistor



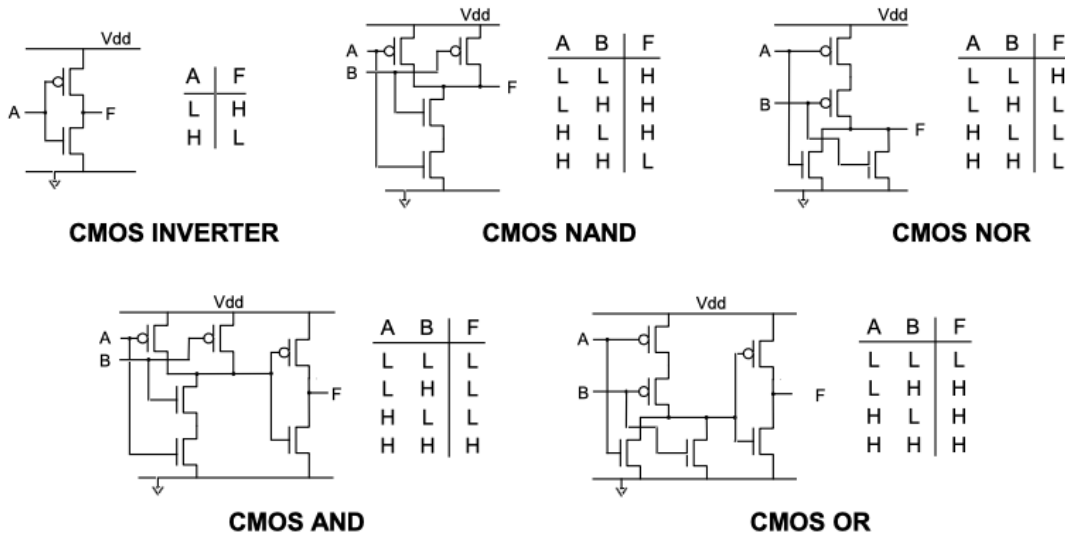
Input	Output
0	1
1	0



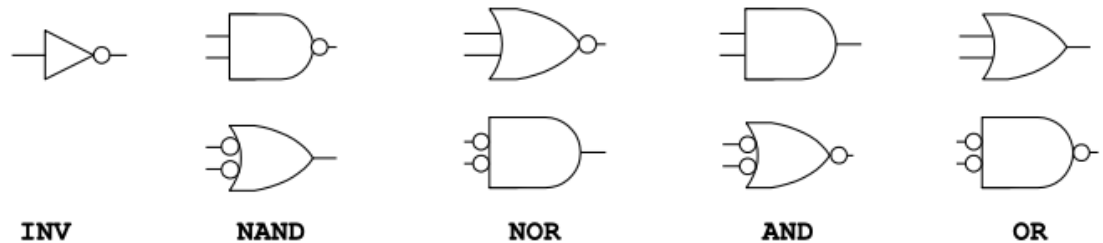
CMOS Inverter for Digital circuits

(solves the static current problem of NMOS circuits when the Output value is "0")

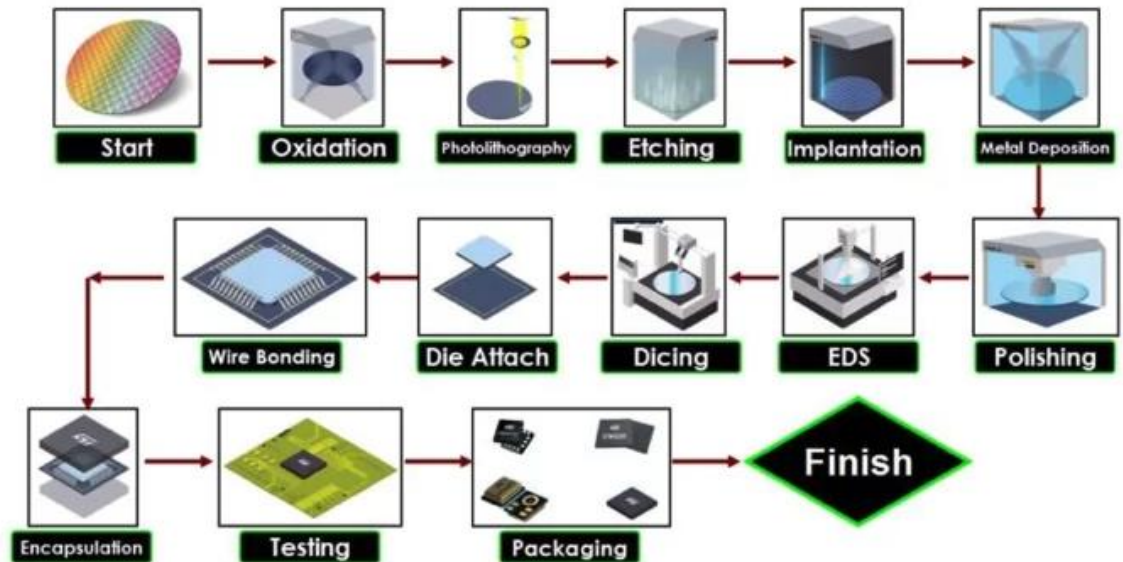
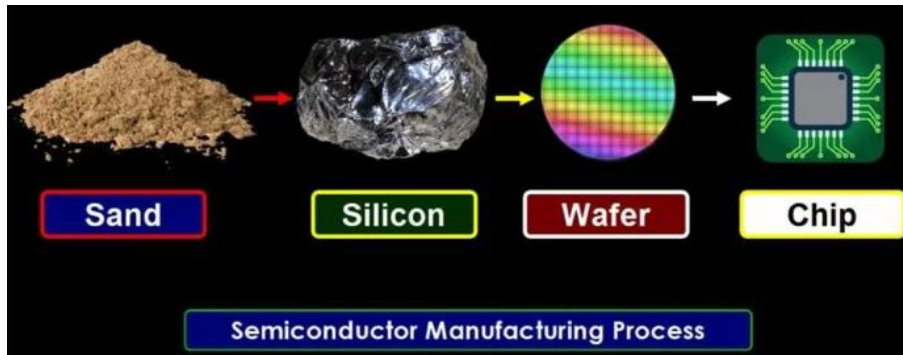
Basic CMOS Logic Gates and their truth table

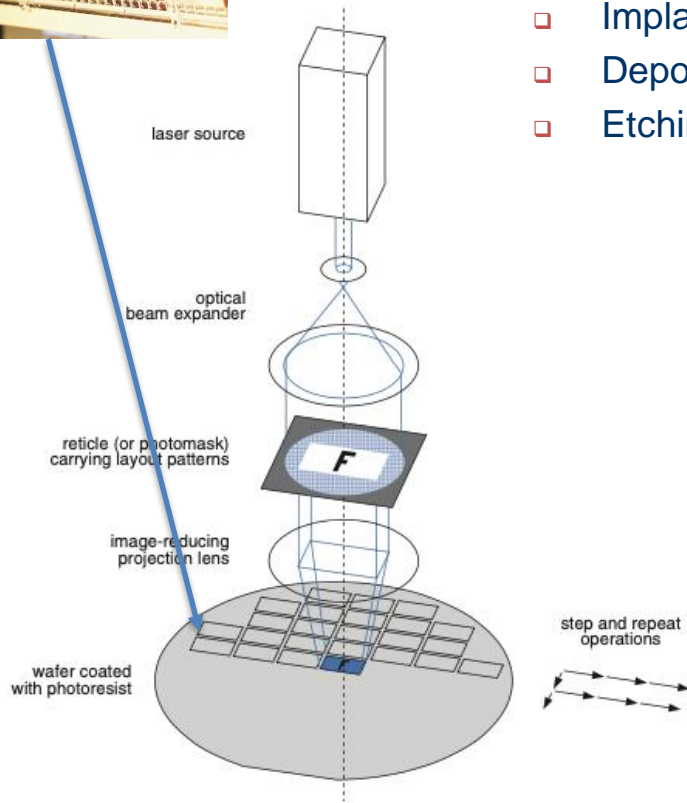
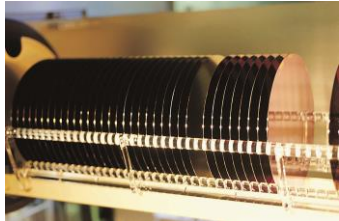


Basic CMOS Logic Gate Symbols



Semiconductor Manufacturing Process Flow Chart





■ Fabrication Steps

- Illumination
- Implantation
- Deposition
- Etching

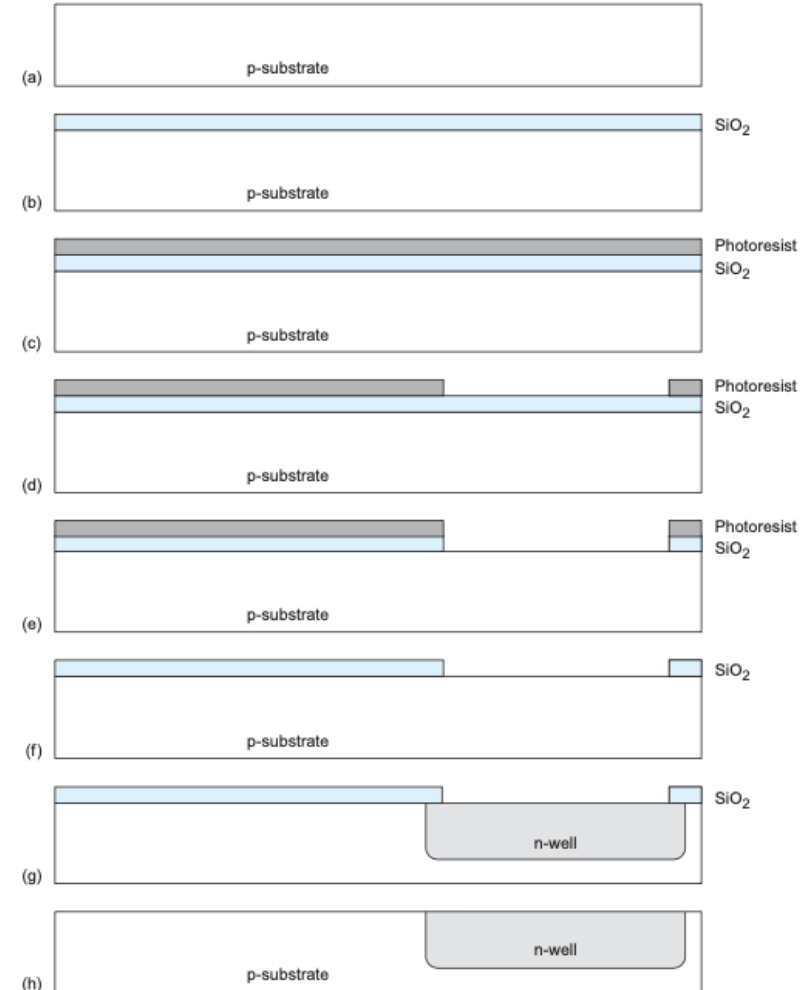


FIGURE 1.36 Cross-sections while manufacturing the n-well

Apparatus for optical lithography (greatly simplified).

Complementary Metal Oxide Semiconductor

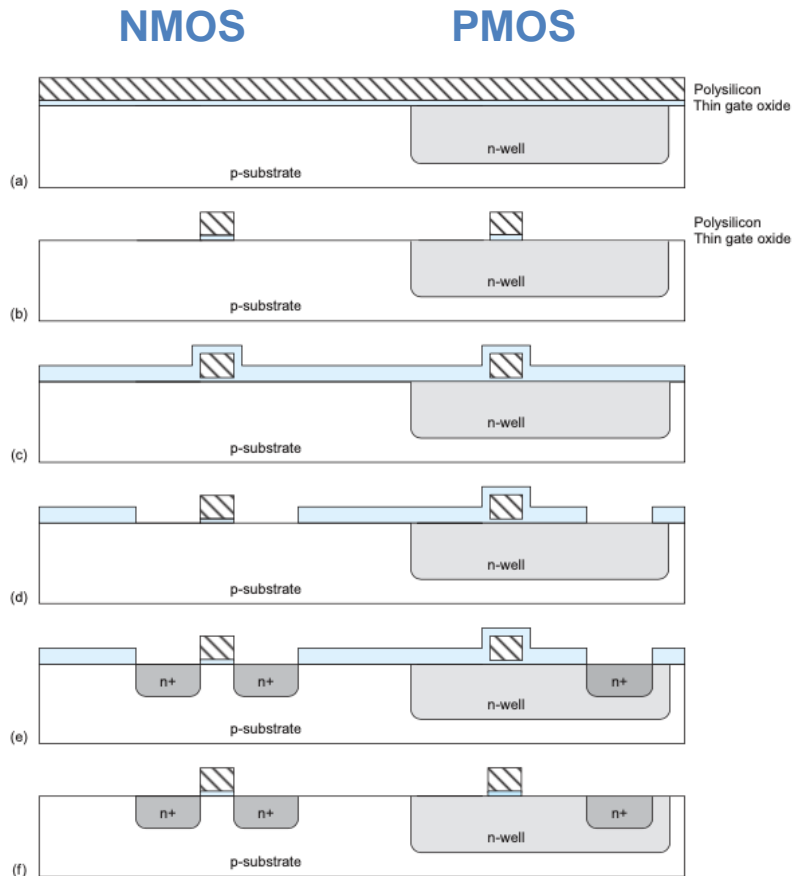


FIGURE 1.37 Cross-sections while manufacturing polysilicon and n-diffusion

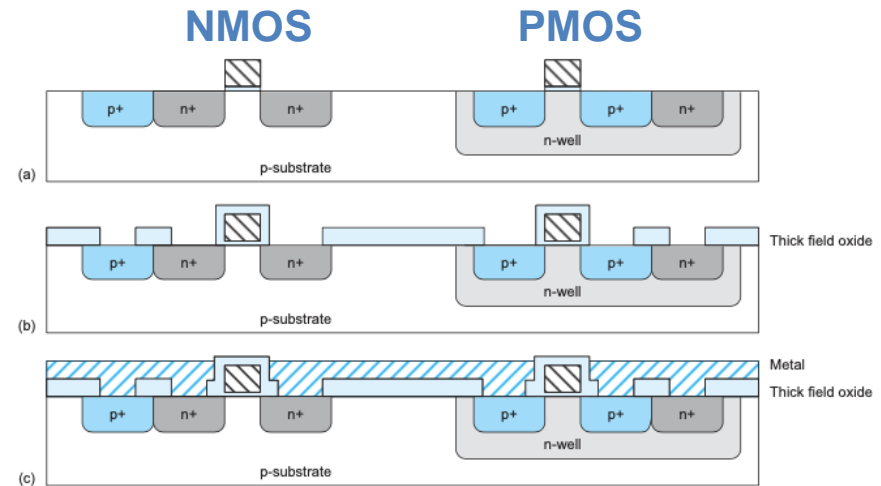
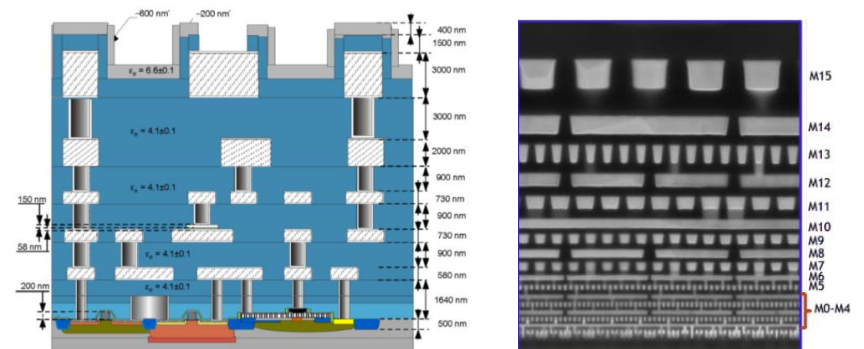


FIGURE 1.38 Cross-sections while manufacturing p-diffusion, contacts, and metal



CMOS Fabrication

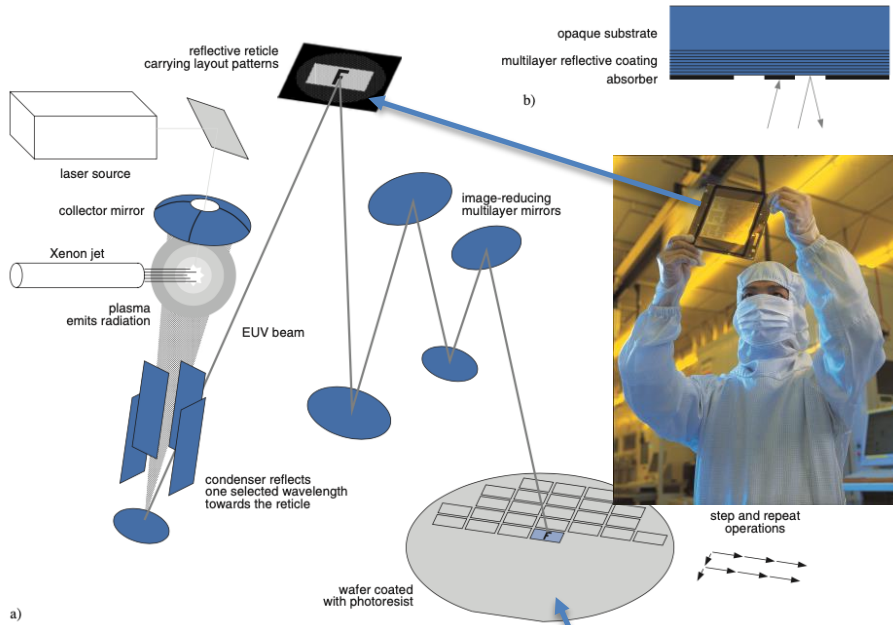


Fig. 14.25 Apparatus for EUV lithography (a) and cross section through a reflective mask (b), mirrors are the same with no absorbing coating (greatly simplified).

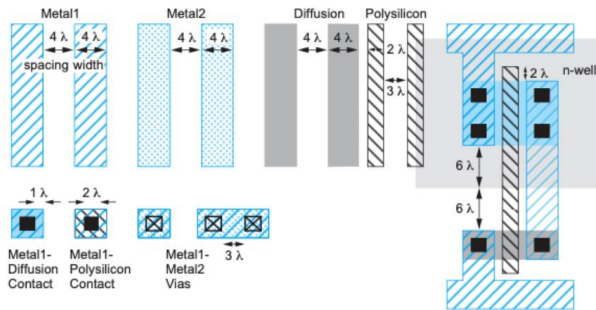


FIGURE 1.39 Simplified λ -based design rules

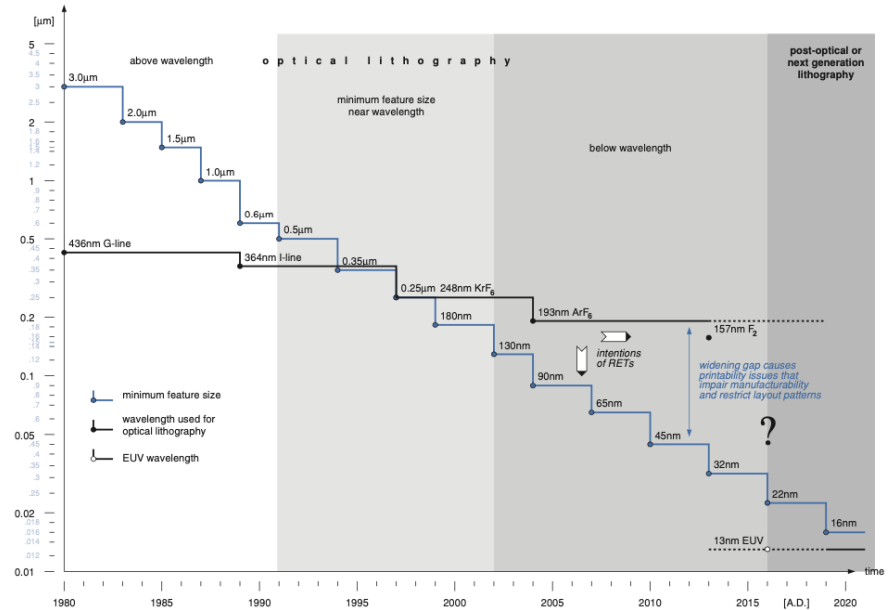
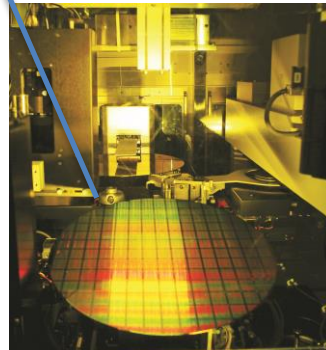


Fig. 14.22 Evolution of VLSI lithography.

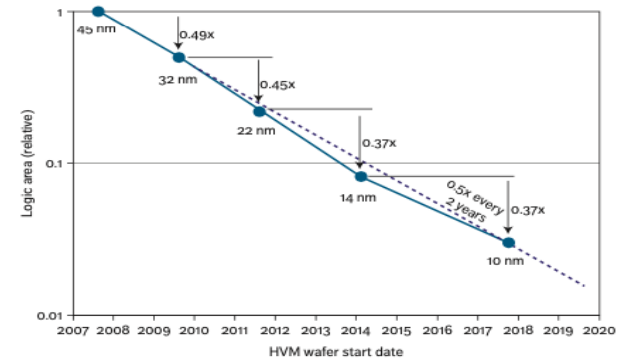


Figure 8. Intel's trend for scaling logic circuit area over the past five generations.



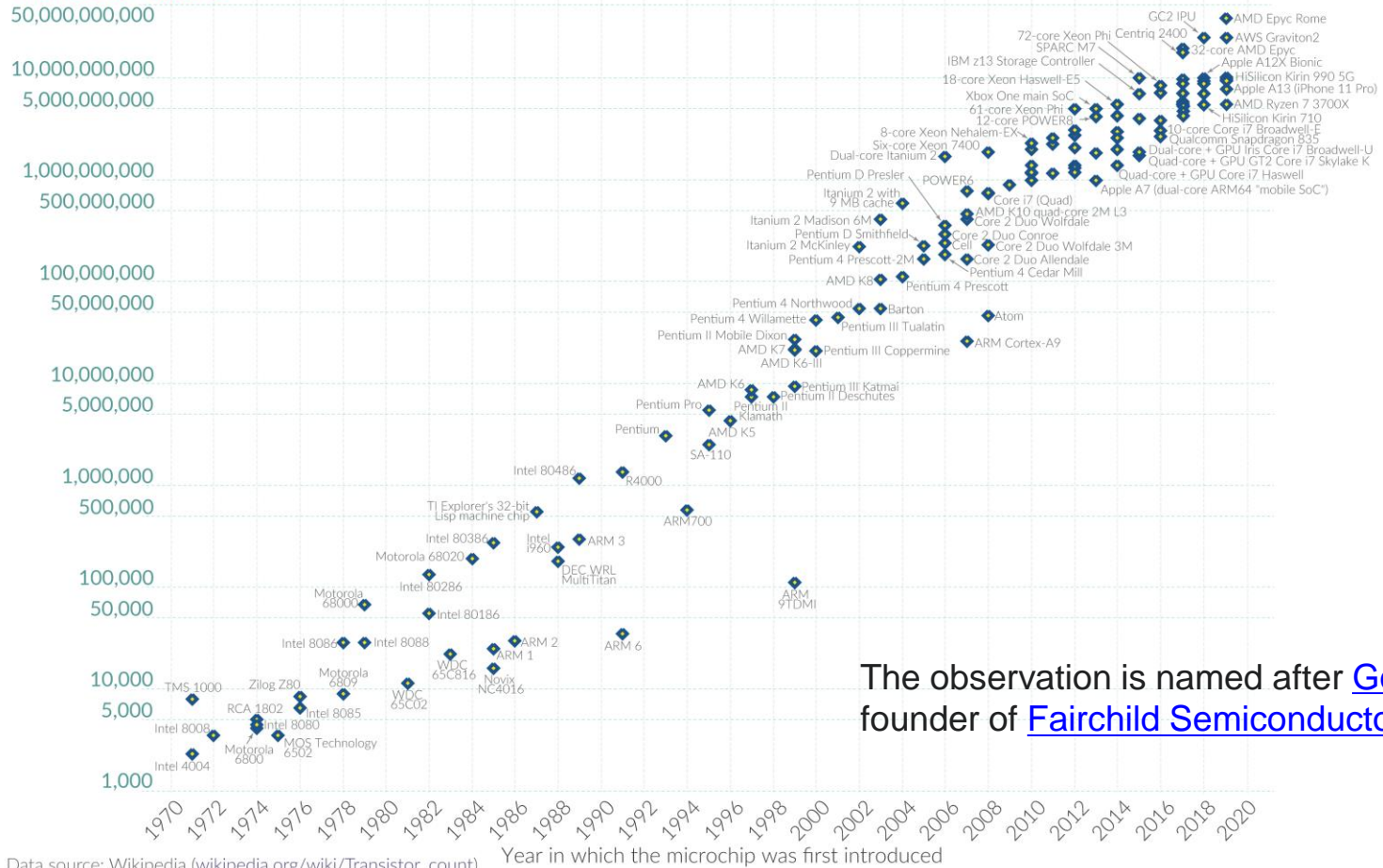
Moore's Law

Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.



Transistor count



The observation is named after [Gordon Moore](#), founder of [Fairchild Semiconductor](#) and [Intel](#)

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldinData.org – Research and data to make progress against the world's largest problems.

Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

Evolution of Intel Processors

The Revolution Begins

Throughout history, new and improved technologies have transformed the human experience. In the 20th century, the pace of change sped up radically as we entered the computing age. For nearly 40 years Intel innovations have continuously created new possibilities in the lives of people around the world.



1969



1972



1976

1983

Moore's Law

In 1965, Intel's founder Gordon Moore predicted that the number of transistors on a chip would double about every two years. Over time, Moore's Law has fueled a technological revolution as Intel has exponentially increased the number of transistors integrated onto its processors for greater performance and energy efficiency.



1992



2002

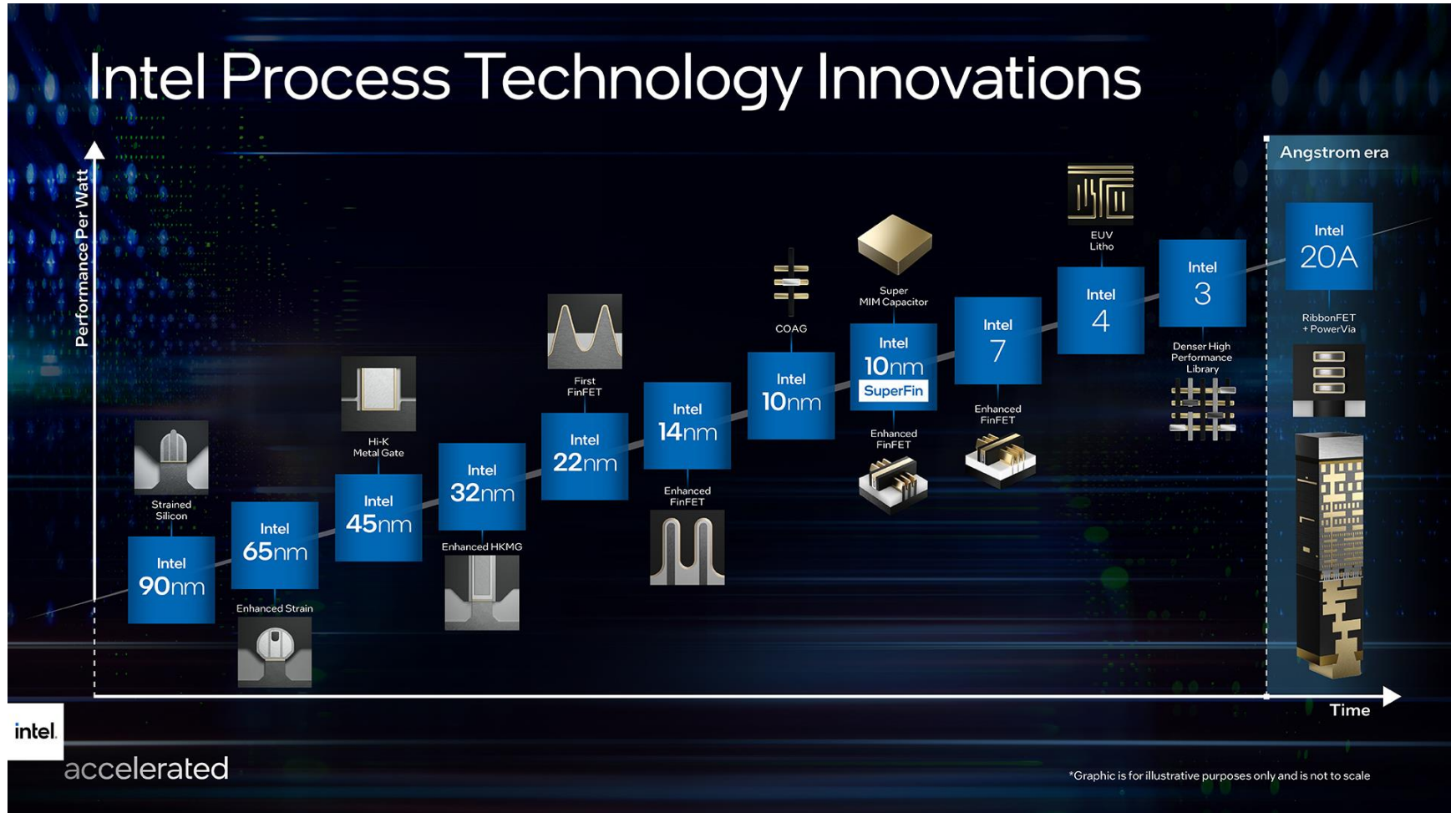


2006

The Revolution Continues
Intel continues to deliver on the promise of Moore's Law with the introduction of powerful multi-core technologies, transforming the way we live, work, and play once again.



Evolution of Intel Processors





Semiconductor Foundry (Fab)



Construction cost of a modern Fab ~\$20 billion



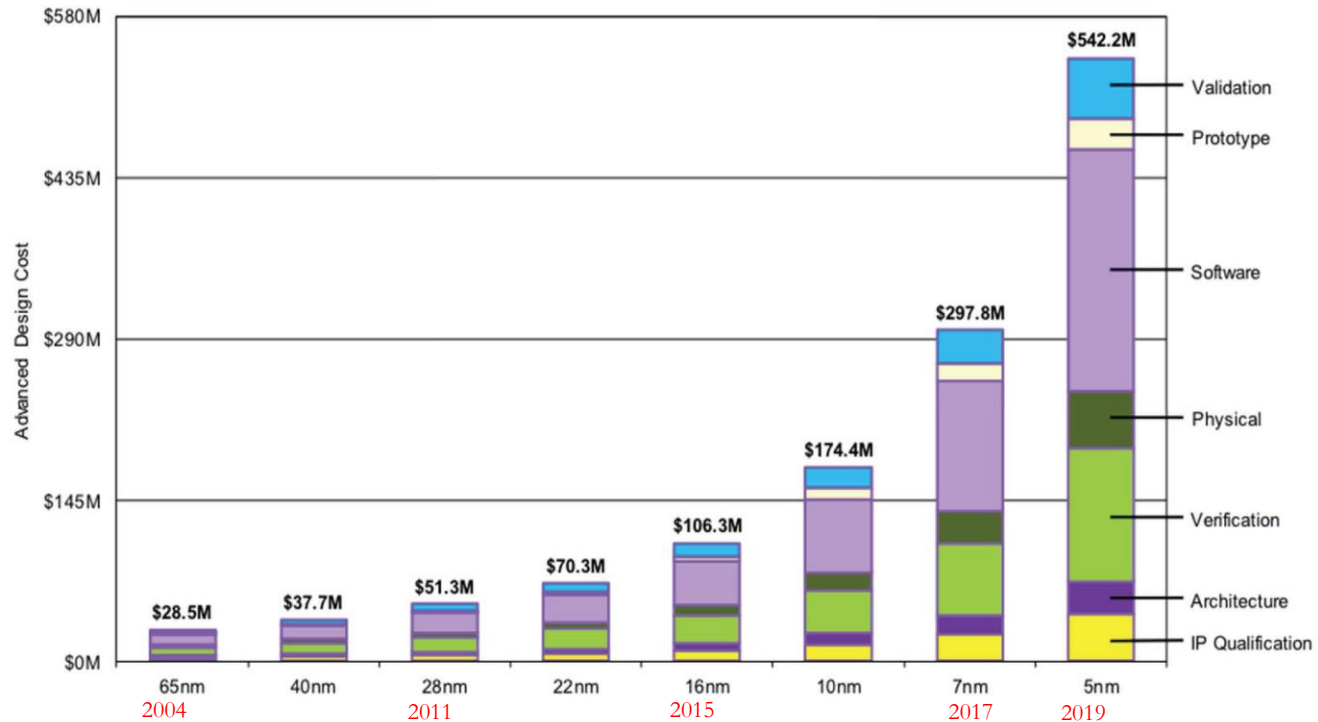
A Major Fab

Location	
AP1 Hsinchu, Taiwan	
AP2B AP2C (<i>Under construction</i>) Tainan, Taiwan	 
AP3 Longtan, Taiwan	
AP5 Taichung, Taiwan	
AP6 (<i>Under construction</i>) Chunan, Taiwan	





ASIC development costs



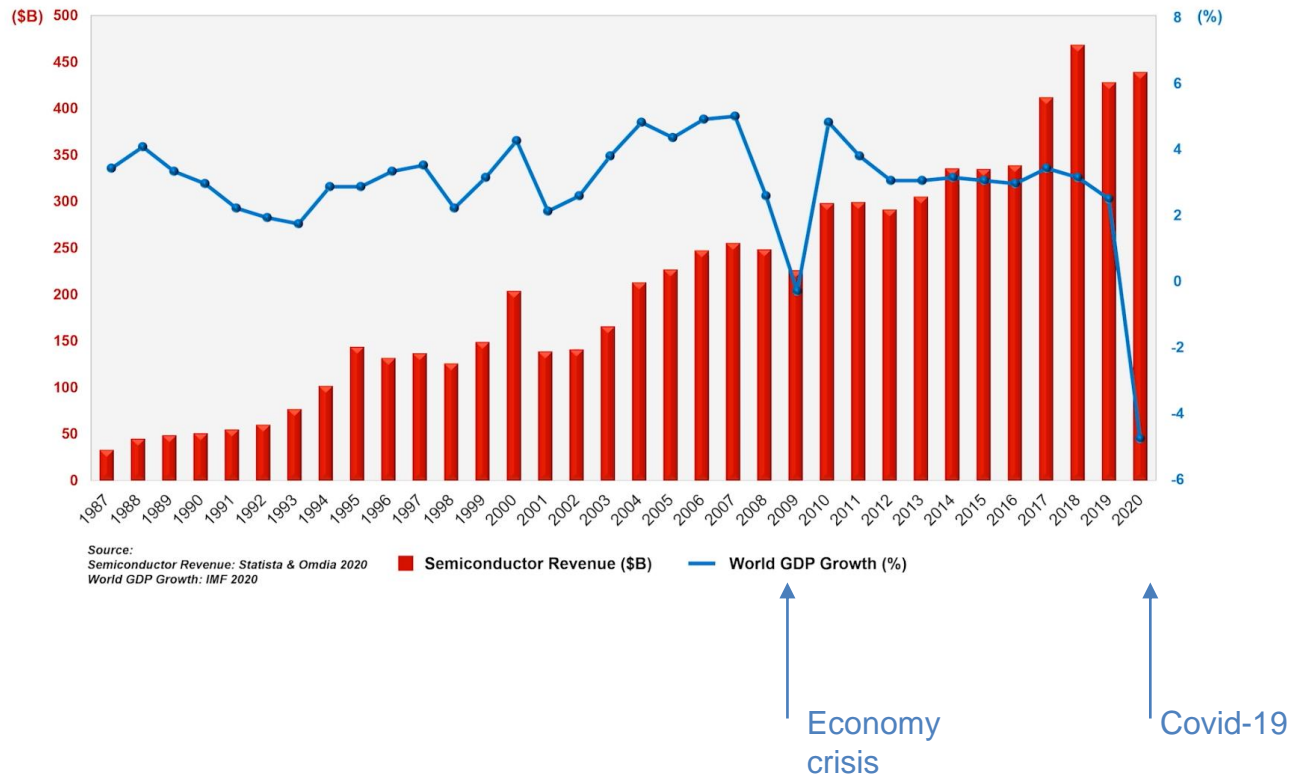
Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

* According to the survey from the *International Business Strategy Corporation (IBS)*, the increase of design cost for each generation technology has exceeded 50% after 22 nm process, including EDA, design verification, IP core, tape-out, and so forth.



Semiconductor industry

Semiconductor Revenue and World GDP Growth





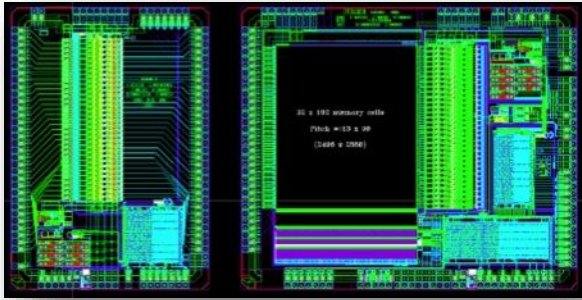
Summary

- Application-specific integrated circuits (ASICs) are the enabling technology for many complex detector systems
 - Customised electronic circuits for a well-defined application
 - Typically manufactured in CMOS processes
- Pros of ASICs
 - **Optimised** for demanding requirements: size, power, functions, performance,...
 - **Miniaturised**, ideal for high density HEP (large number of channels)
 - High **quality with low unit cost** on large scale
 - **Radiation hardness** using commercial processes
- Cons of ASICs
 - **Big development investment** required in both time and cost increasing as functionality (= complexity) increases
 - **Unchangeable** once complete, unless a lot of flexibility is built-in(adds complexity)
 - **Substantial design and evaluation** requiring specialist skills (industry pays well!)

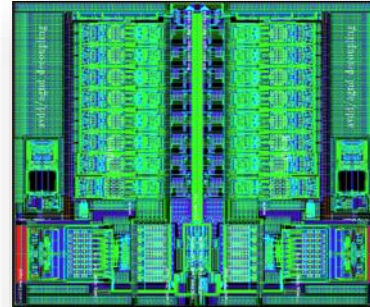
A nighttime photograph of the ATLAS detector dome at CERN, illuminated from within, set against a dark blue sky with stars and a meteor streak.

Thank You

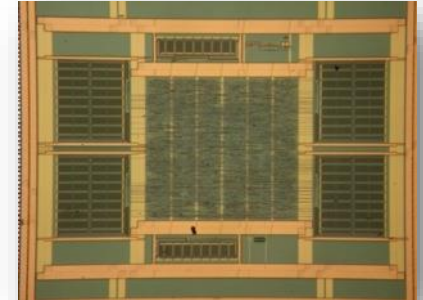
Typical ASIC designs at CERN



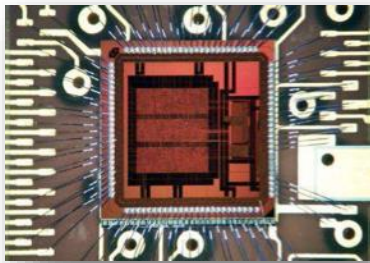
128ch pre-amp, analog memory chipset



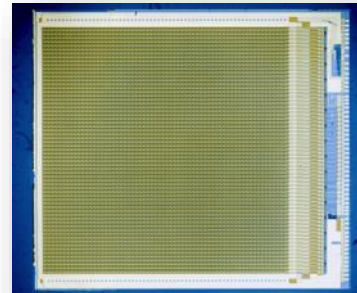
4ch 40Msps 12-bit ADC



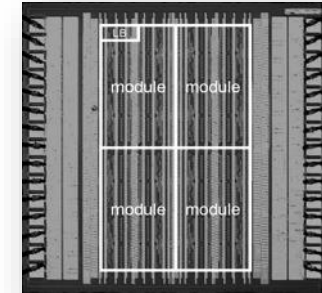
4ch data readout chip



Gigabit Optical Link



MEDIPIX1 Pixel chip



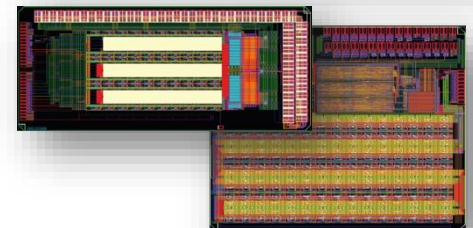
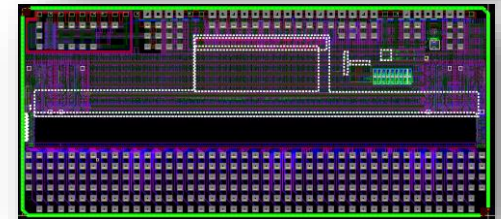
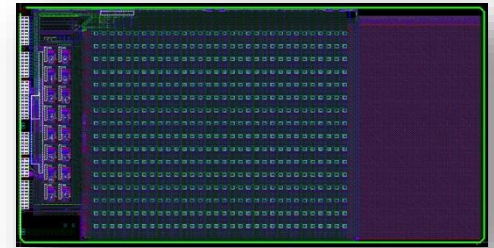
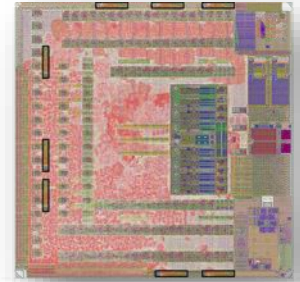
Rad-Tol FPGA

■ Typical ASIC designs:

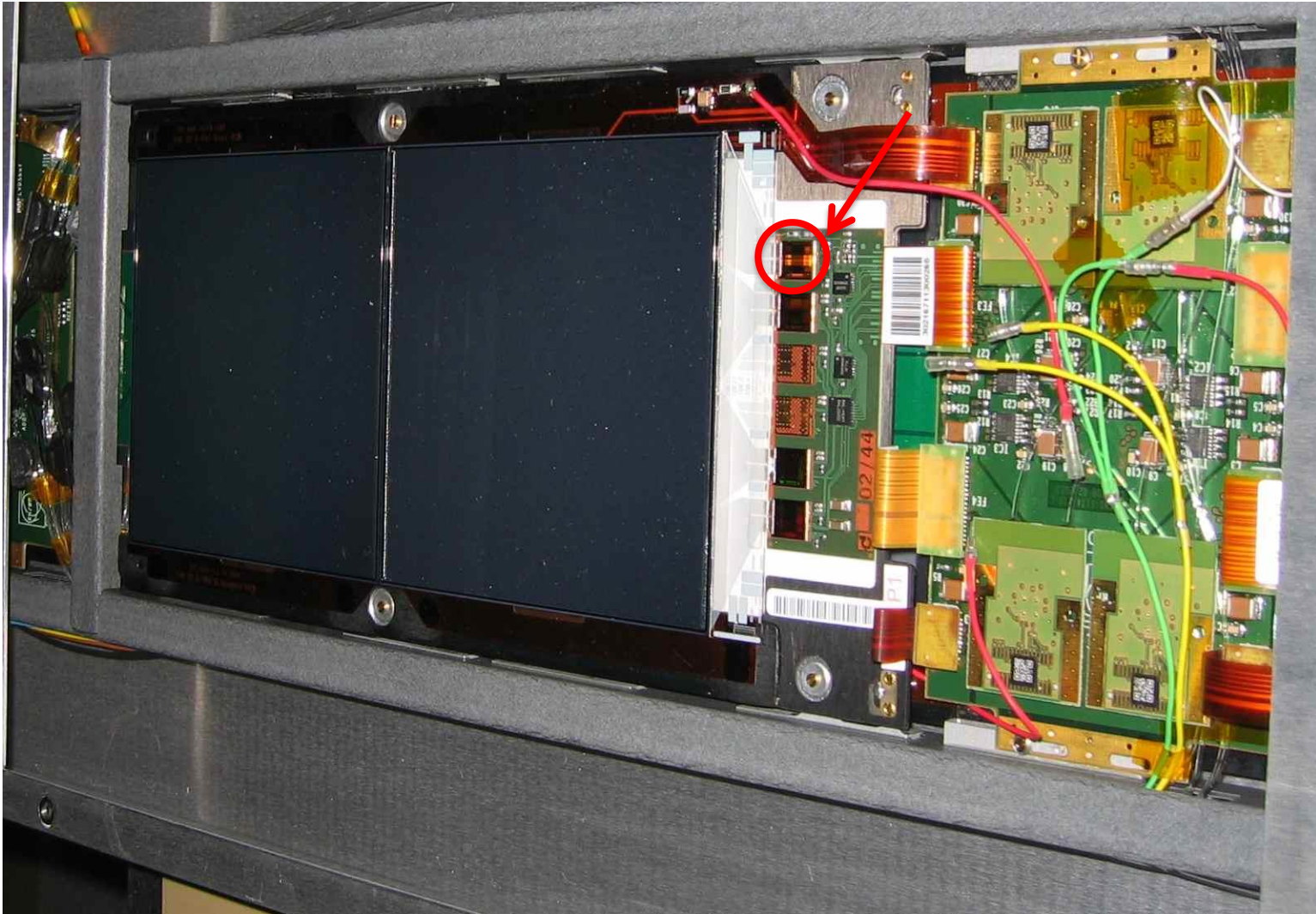
- ❑ Analog circuits with complex full custom designs
- ❑ Mixed Signal with large high performance analog and digital circuits
- ❑ Digital circuits ~500K gates.

250nm ASICs

- **Gigabit Transceiver Project (GBT)**
 - “GBLD” Gigabit Laser Driver chip final version in 2012.
 - “GBT-TIA” Transimpedance Amplifier chip in 2010.
 - “GBTX”, Transceiver chip, first prototype in 2009, second prototype in 2012.
 - “GBT-SCA”, Slow Control Adapter, first prototype in 2013.
- **Design Projects for the XFEL Synchrotron facility**
 - XFEL & DSSC ASIC designs
 - Prototype chips submitted in 2010, 2011, 2012.
 - DSSC full prototype submission scheduled for early 2014.
- **CBC: CMS Tracker Front-End ASIC**
 - First prototype submitted in 2010 MPW.
 - Second prototype submitted in 2012 MPW.
- **S-Altro: ALICE TPC Readout ASIC**
 - Submitted in 2010 on an MPW (24 wafers).
- **NA62 Pixel Gigatracker detector**
 - Test chips prototyped in 2010.
 - First prototype submitted in 2013.

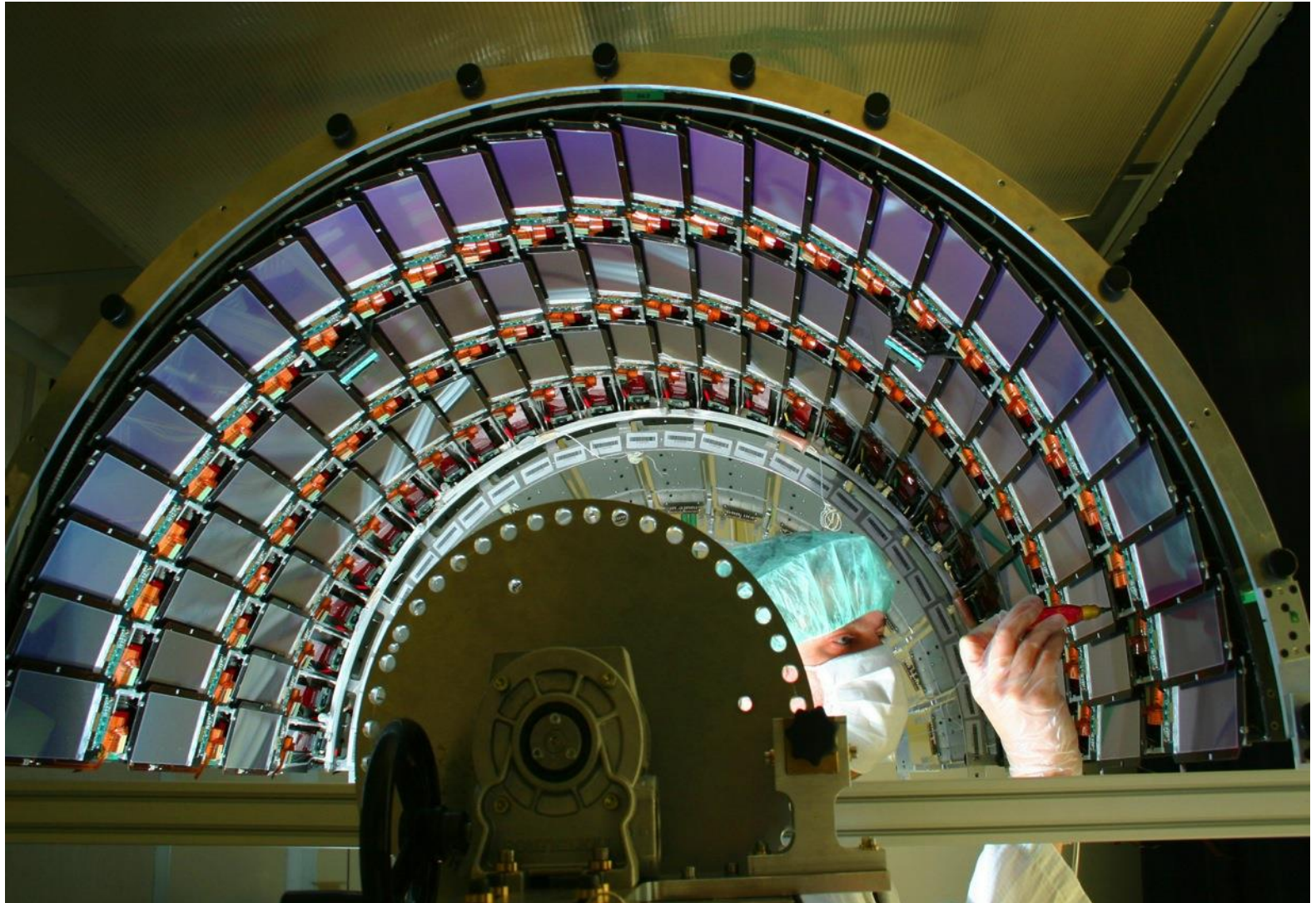


Tracker sensor with electronics



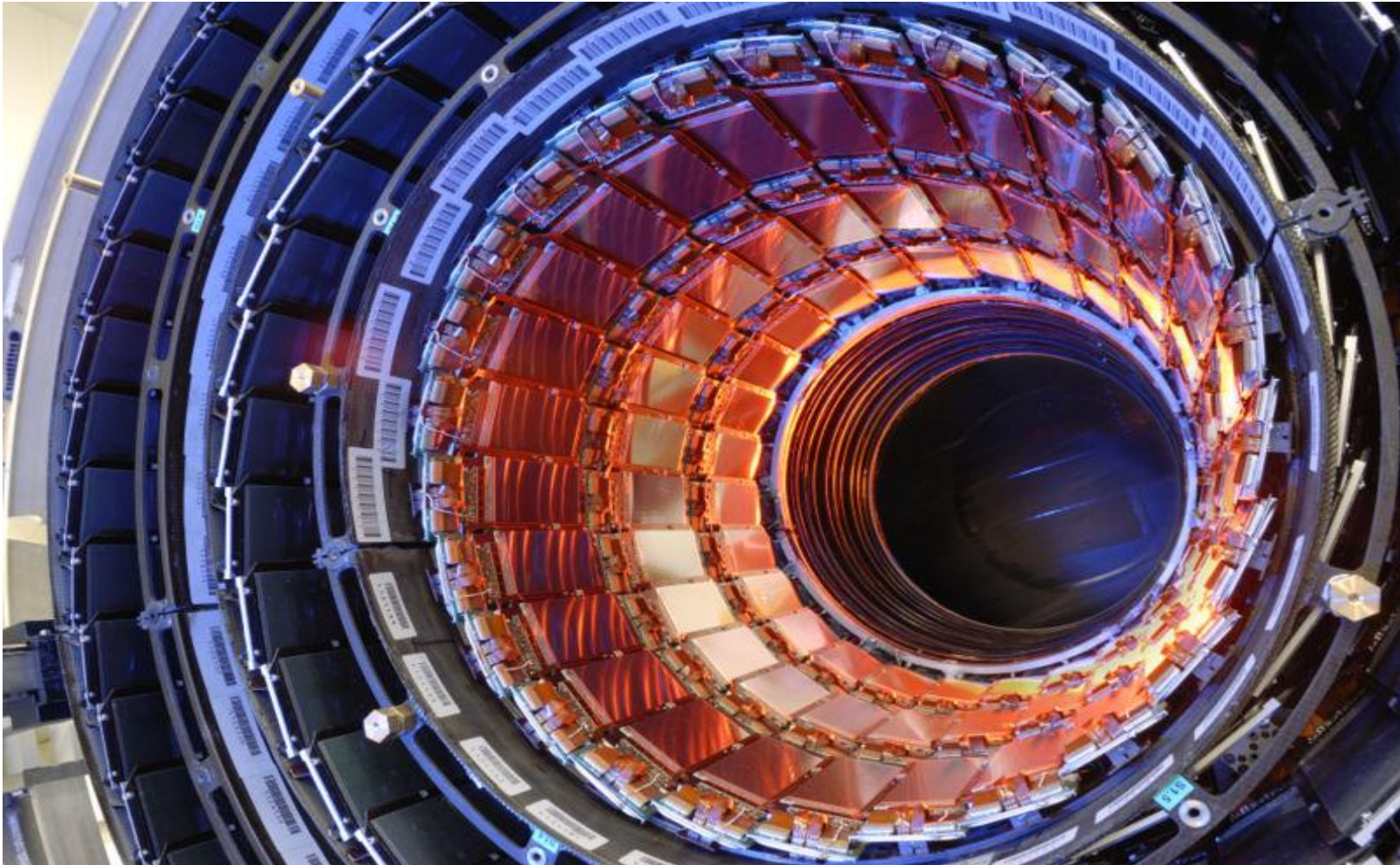


Detector assembly

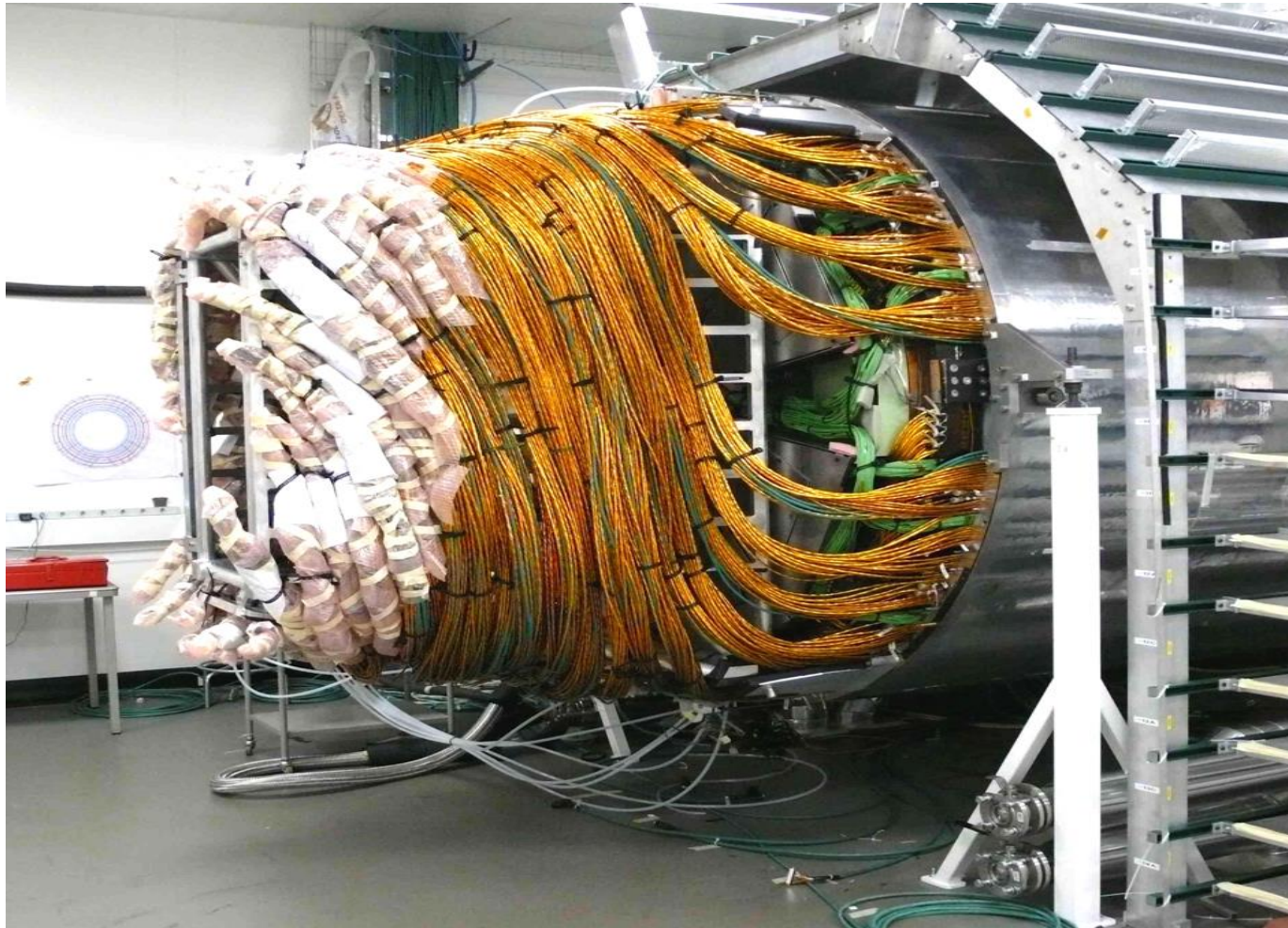




Detector assembly



Assembled Detector





The Tracker in the CMS experiment

