ARCADIA

Depleted monolithic CMOS sensors and very low power readout architectures

INFN
Istituto Nazionale di Fisica Nucleare

ARCADIA

Manuel Rolo (INFN)

on behalf of the **ARCADIA Collaboration**

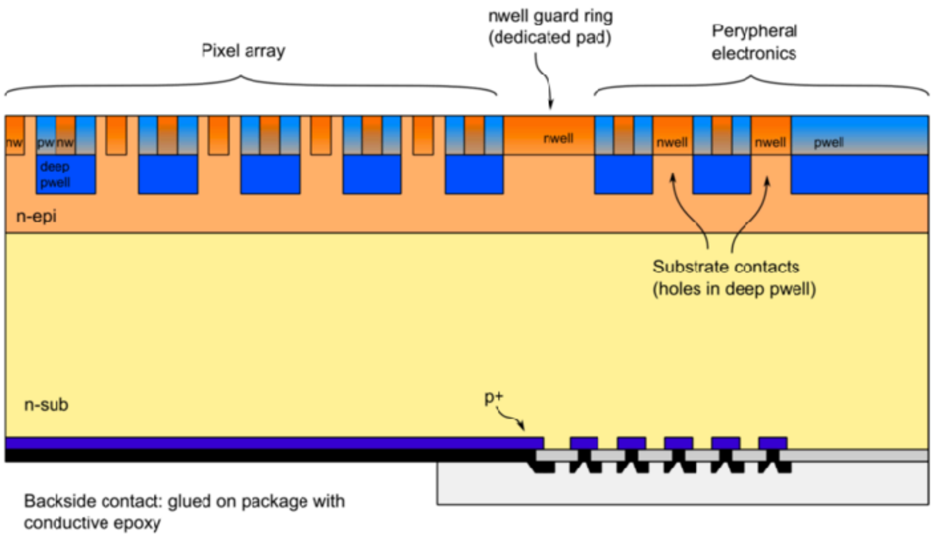
ASAPP 2023 Advances in Space AstroParticle Physics
Frontier technologies for particle measurements in space
June 19-23, 2023
Perugia (IT)

ARCADIA DMAPS R&D at INFN

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

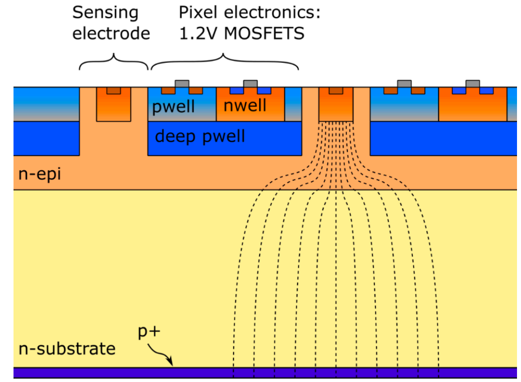
Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

- Active sensor thickness in the range 50 µm to 500 µm;
- Operation in full depletion with fast charge collection by drift, small collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(**10 mW/cm²**));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: LF11is 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry



Sensor Concepts and post-processing

- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top



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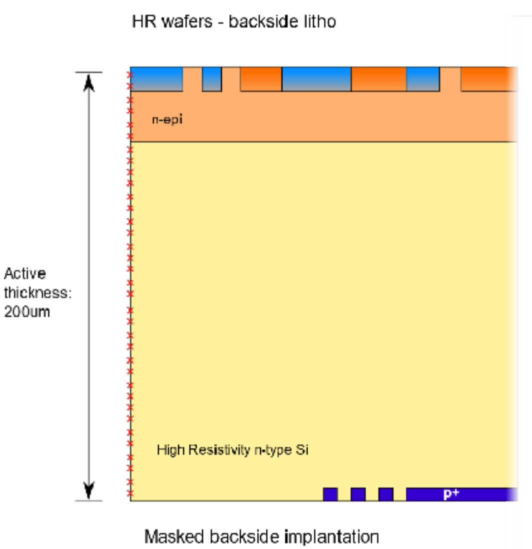
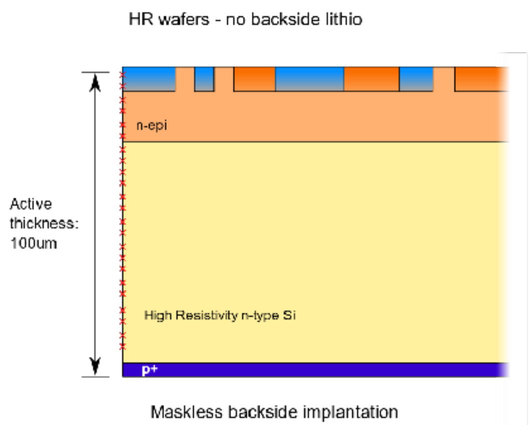
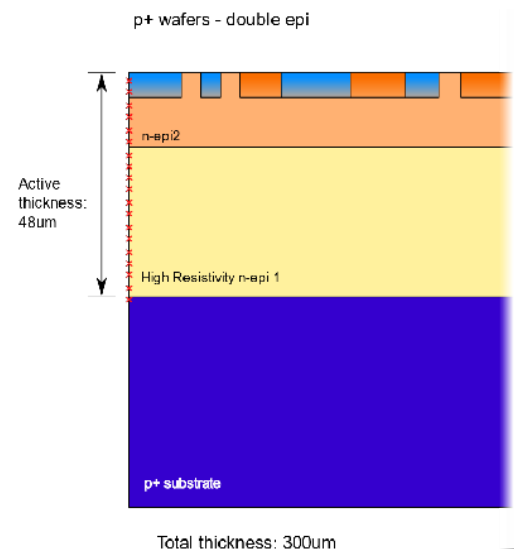
"Fully Depleted MAPS in 110-nm CMOS Process With 100–300-μm Active Substrate," in IEEE Transactions on Electron Devices, June 2020, doi: 10.1109/TED.2020.2985639.



- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition



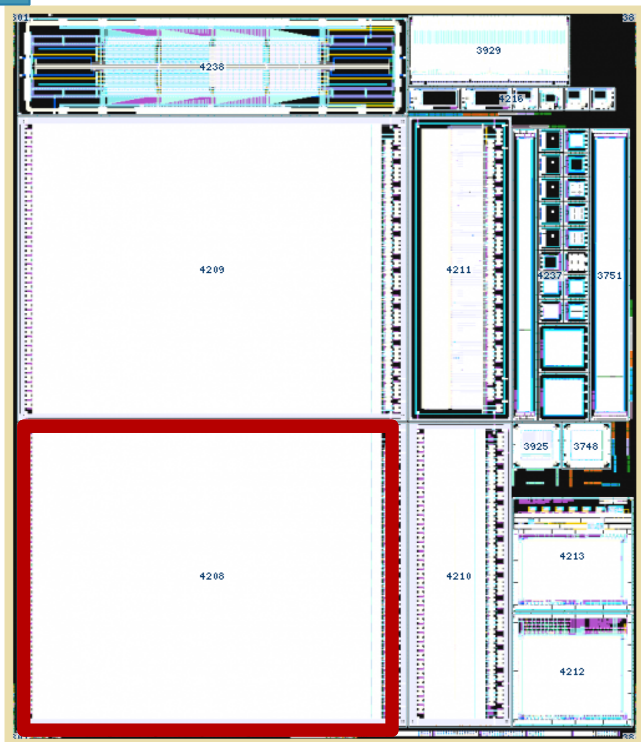
- thinning, backside p+ implantation and laser annealing

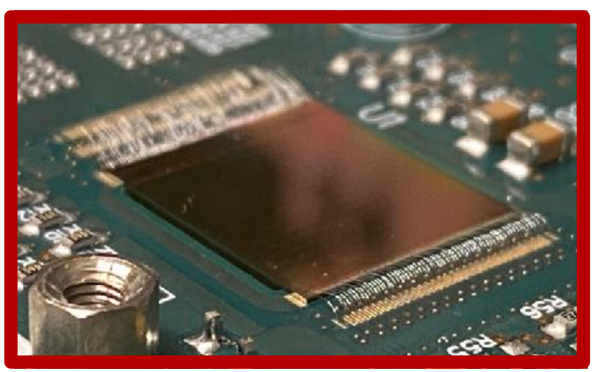


- thinning down to 100 or 300μm total thickness

L. Pancheri

ARCADIA Technology demonstrators





- ARCADIA-MD3 Main Demonstrator
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10µm pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and fully-functional readout electronics
- (ER2) HERMES: small-scale demonstrator for fast timing
- (ER3) Small-scale demonstrator of a X-ray multi-photon counter
- (ER3) Wafer splits with timing layer, new R&D towards <<50 ps timing performance: test structures and
- (ER3) MADPIX: multi-pixel active demonstrator chip for fast timing

ARCADIA-MD3: Chip Floorplan

Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

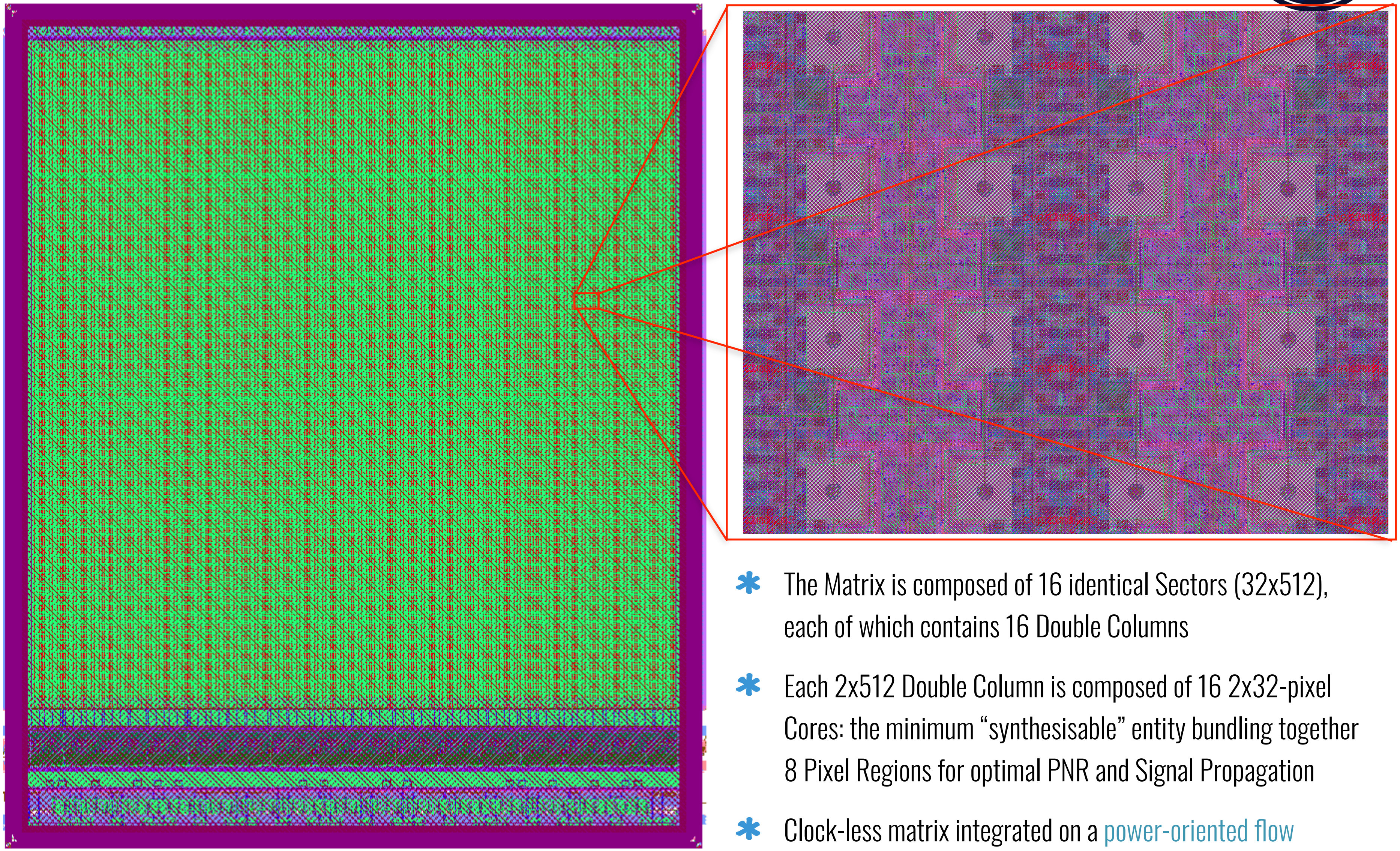
Periphery

SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe

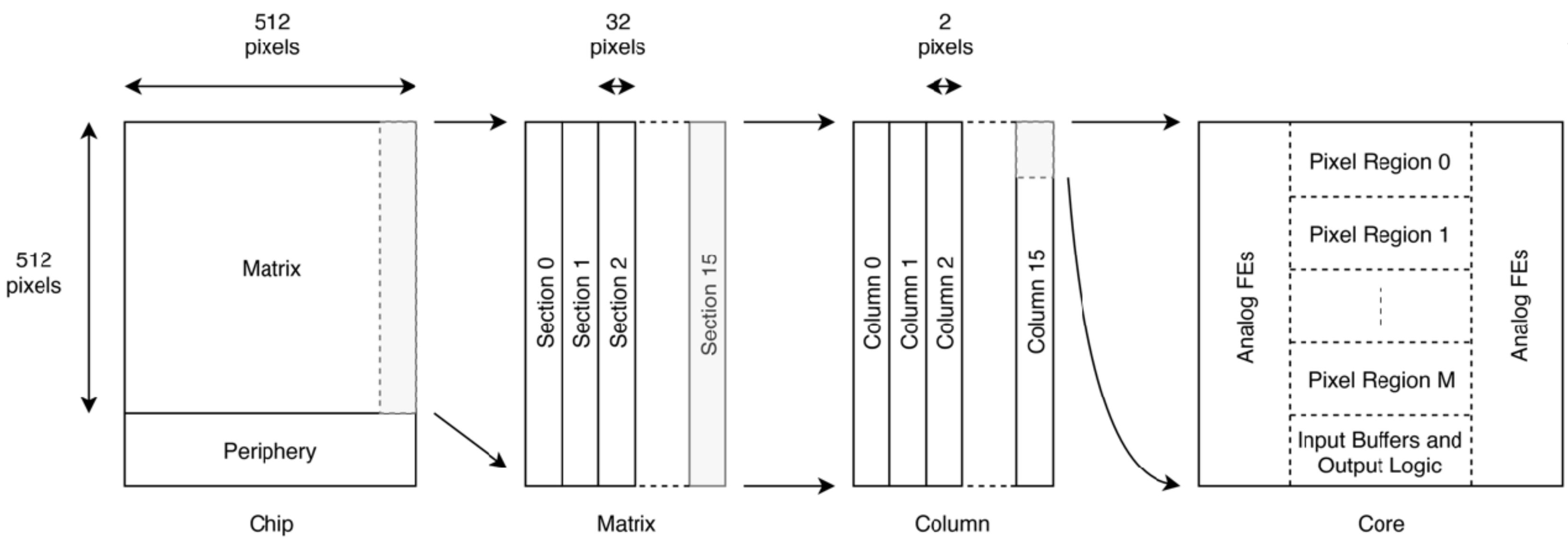
Stacked Power and Signal pads

ARCADIA-MD3: Integration



- The Matrix is composed of 16 identical Sectors (32x512), each of which contains 16 Double Columns
- Each 2x512 Double Column is composed of 16 2x32-pixel Cores: the minimum “synthesisable” entity bundling together 8 Pixel Regions for optimal PNR and Signal Propagation
- Clock-less matrix integrated on a power-oriented flow

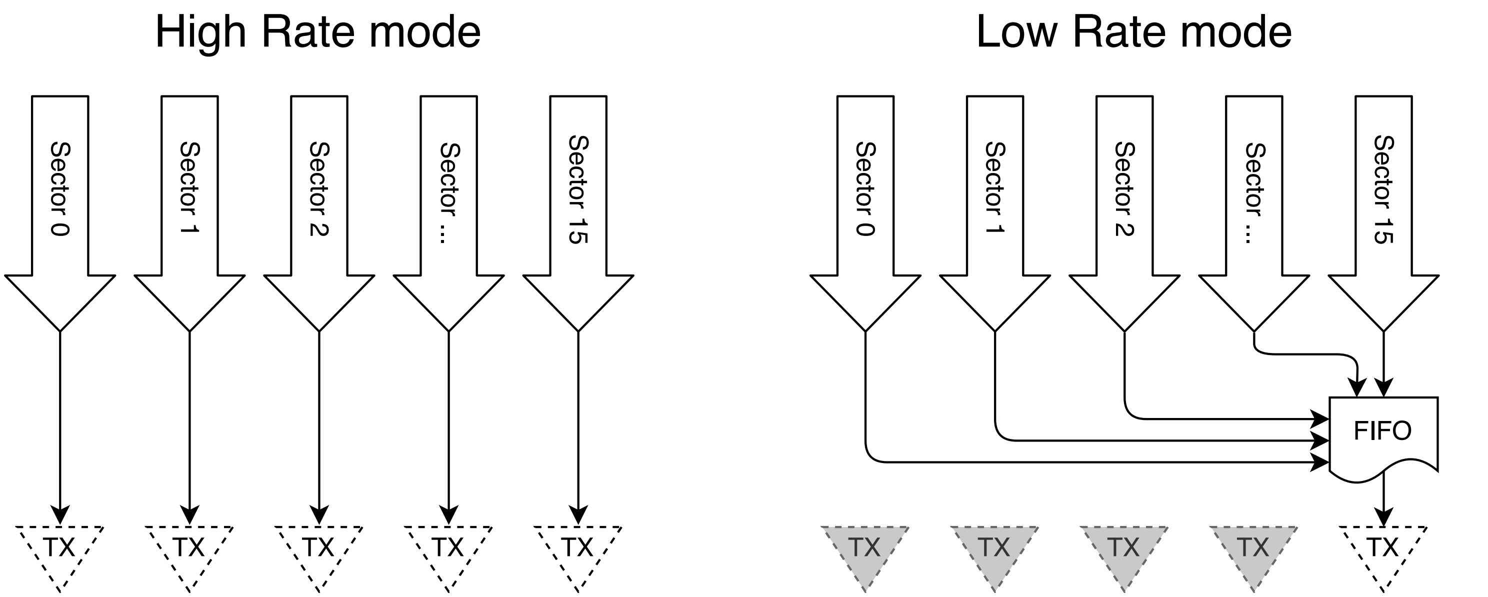
ARCADIA-MD3: Chip Architecture



- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm² silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm² (post-layout simulations, to be demonstrated: test-beam in late 2023)
- High-rate operation (16 Tx): 17-30 mW/cm² depending on transceiver driving strength (measured)
- Low-power operation (1 Tx): **10 mW/cm²** (measured: characterisation data in next slides in low-power mode)

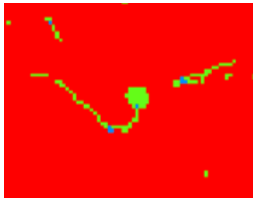
ARCADIA-MD3: Peripheral Dataflow

- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

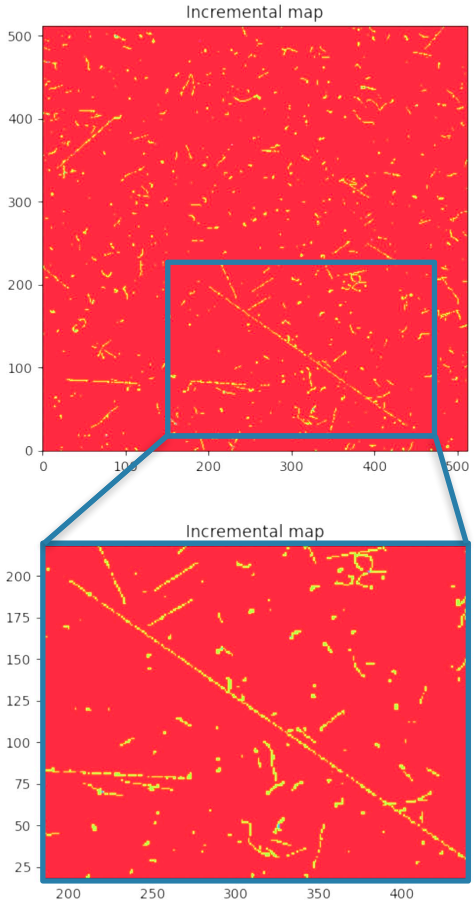


* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

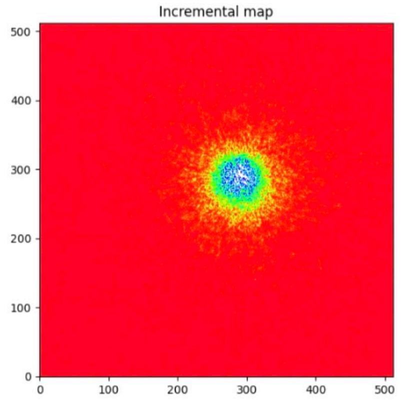
ARCADIA-MD3: charged particles

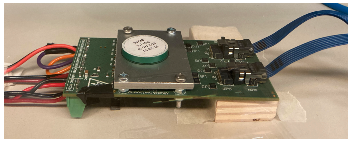


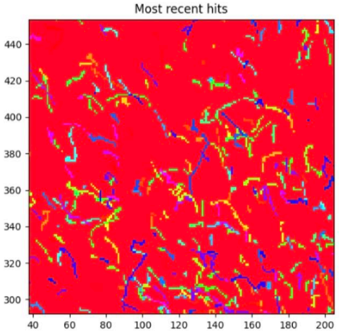
Cosmic rays
(tilted sensor)



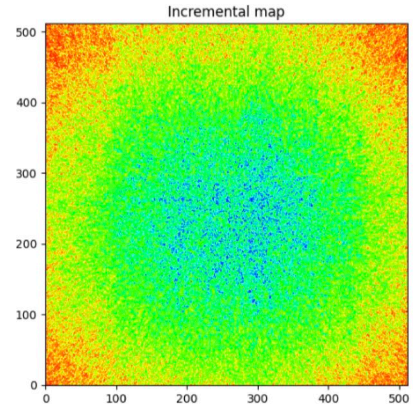
^{90}Sr
(collimated 1mm)

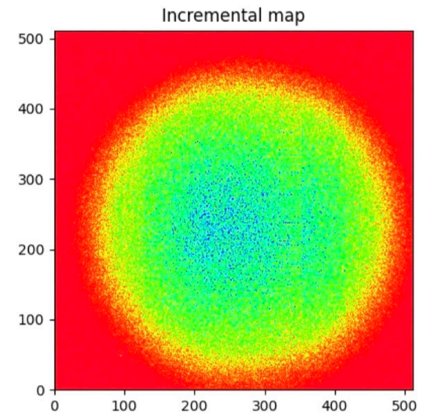




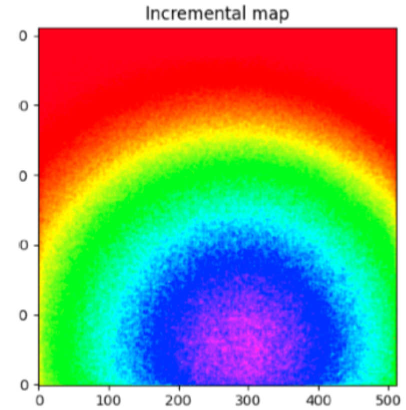


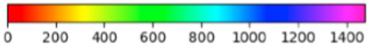
^{90}Sr
(uncollimated)

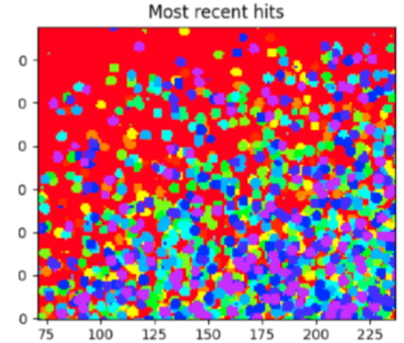




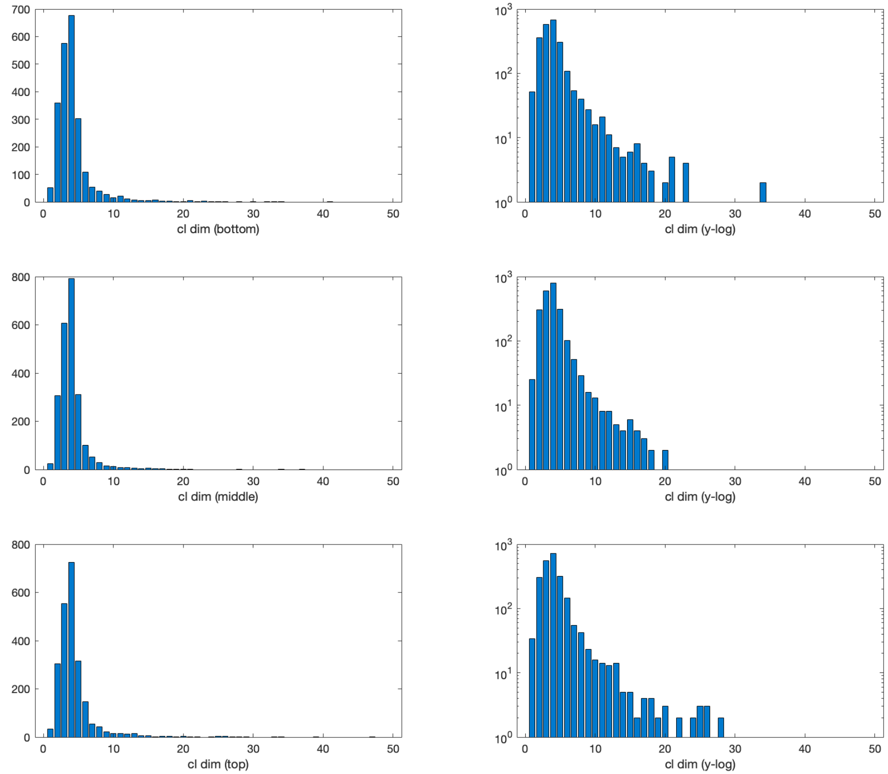
^{241}Am



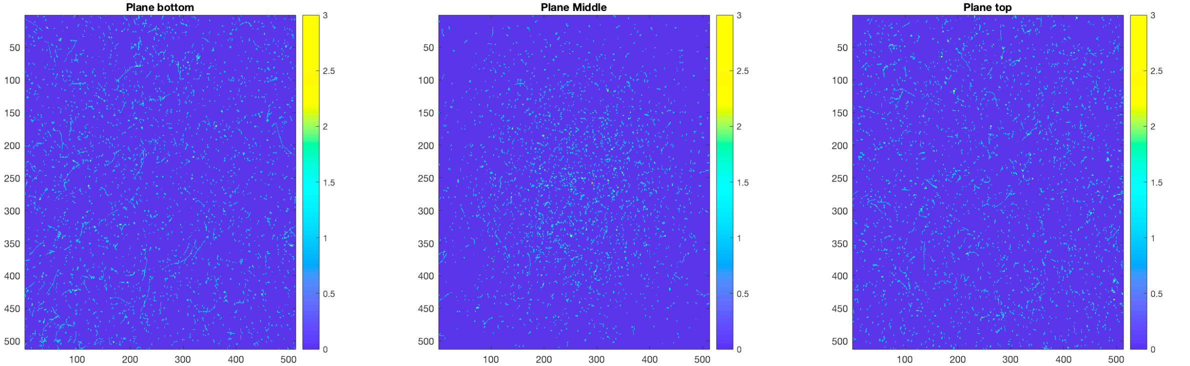


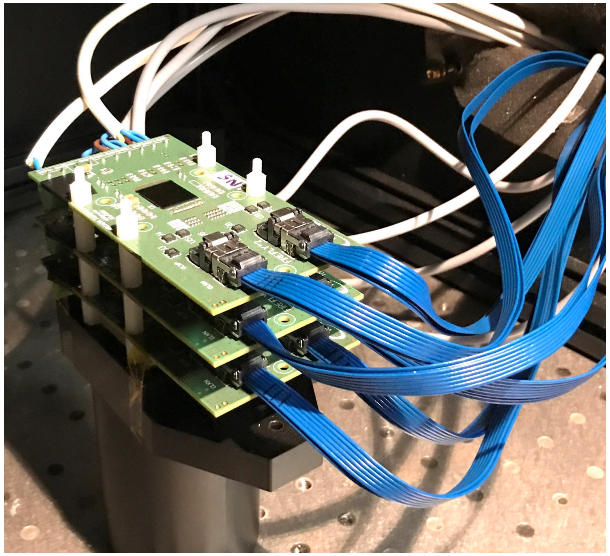


MD3 cosmic data: setup and cluster size



- Cosmic ray data taking: 1 week
- 3-plane MD3 installed on a black box, neither temperature control nor parameter optimisation (pixel discriminator V_{th} still to be equalised at double-column level).
- Threshold 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels





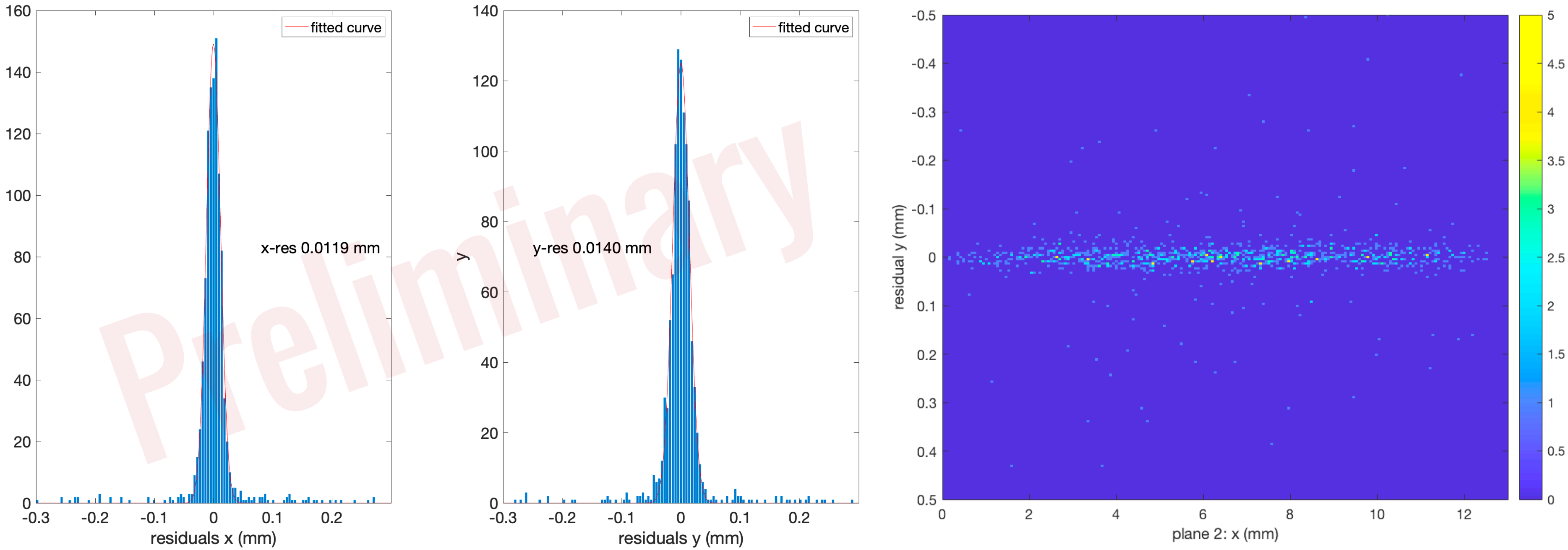
MD3 cosmic data: x-y residuals

Preliminary data without mechanical alignment (3-plane setup without external references), ignoring multiple scattering:

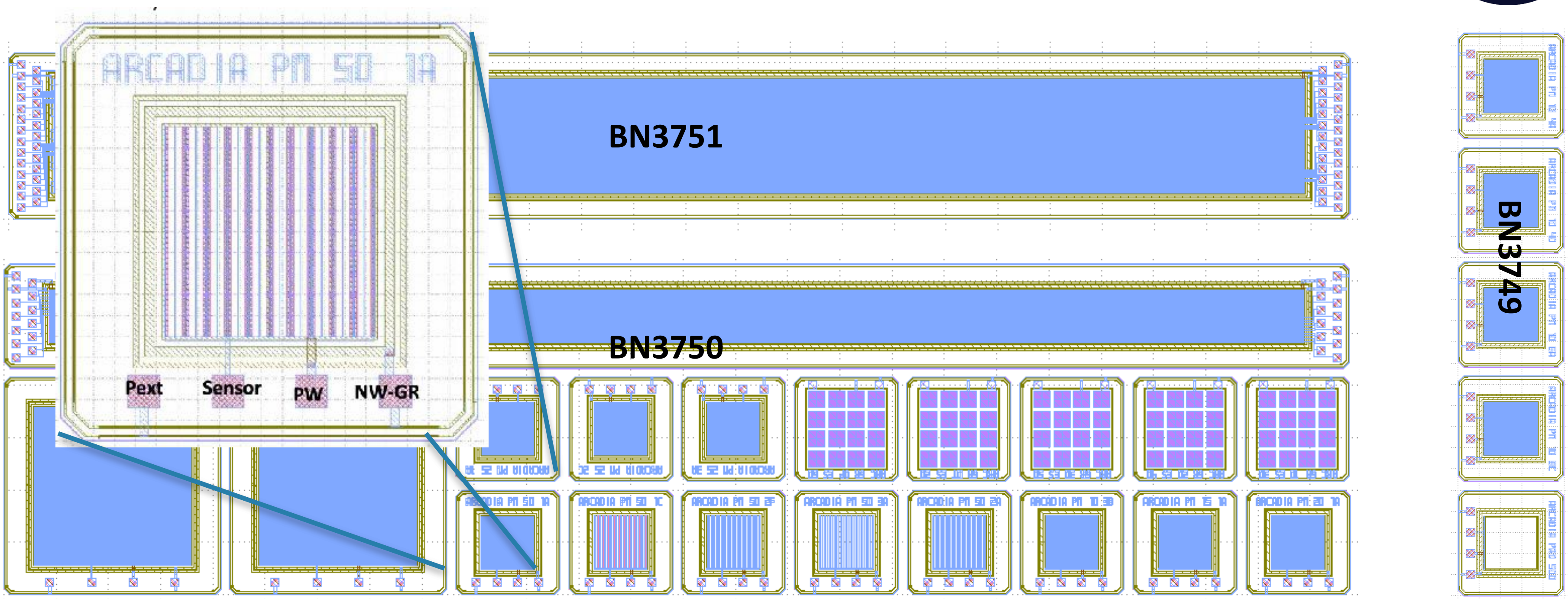
Selection criteria:

- 1 cluster per plane
- dt <= 10 clock cycles
- Cluster dimension <=4 in all planes

Selected ~46% of the synchronised events



Pixel/Strip Test Structures



- pixels come in different flavours:
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)
- and strips as well:
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

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FD Monolithic Active Microstrips

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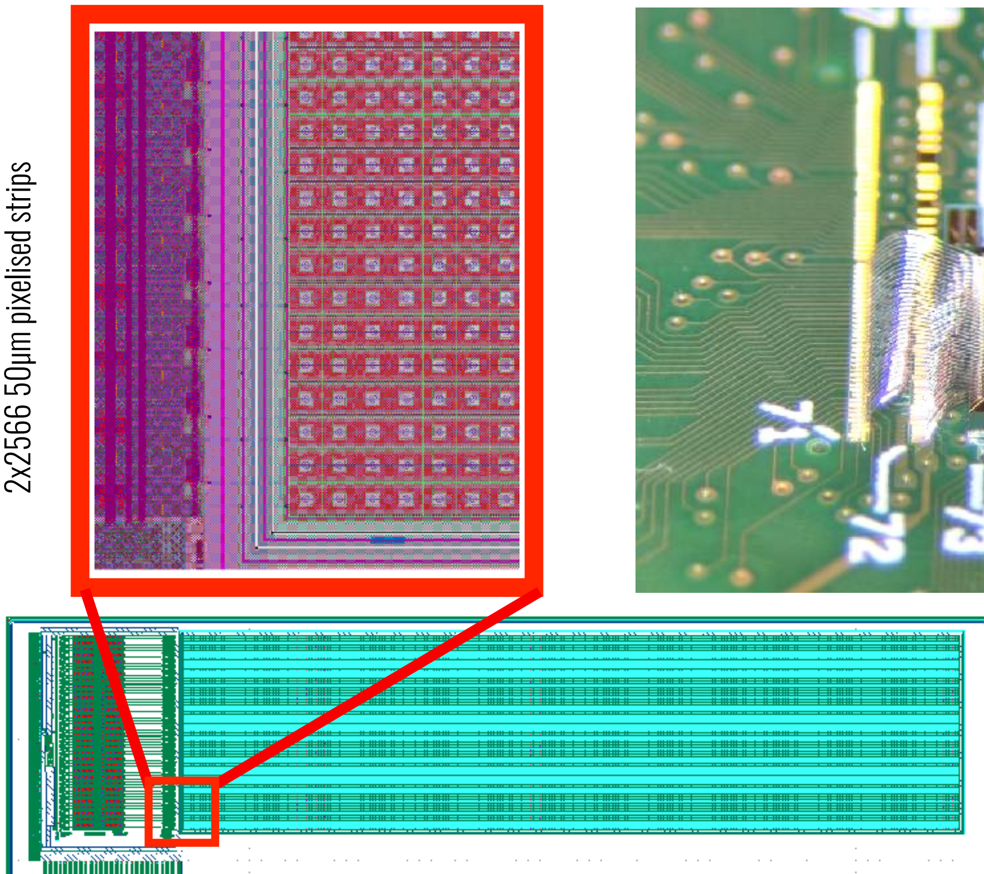
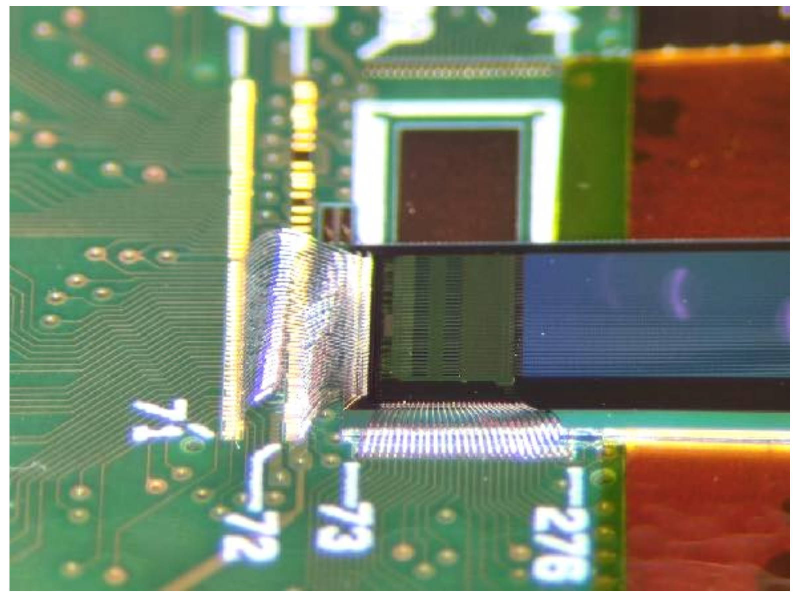
- Design and Production of continuous and "pixelised" strips, range 10 - 100μm pitch
- Proof-of-concept: CMOS monolithic strip block and readout electronics (active sensor area is 12800 × 3200 μm²)

Figure: CAD Layout of 32-block of 2x2566 50μm pixelised strips

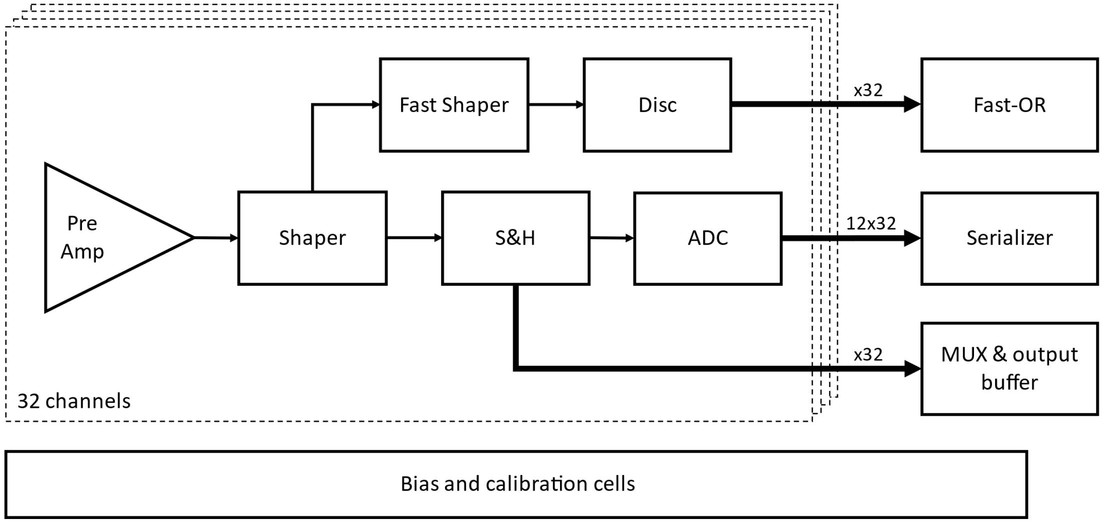




Fully Depleted Monolithic Active Microstrip Sensors: TCAD Simulation Study of an Innovative Design Concept. Sensors 2021, 21, 1990. https://doi.org/10.3390/s21061990

FD-MAMS 32-channel architecture

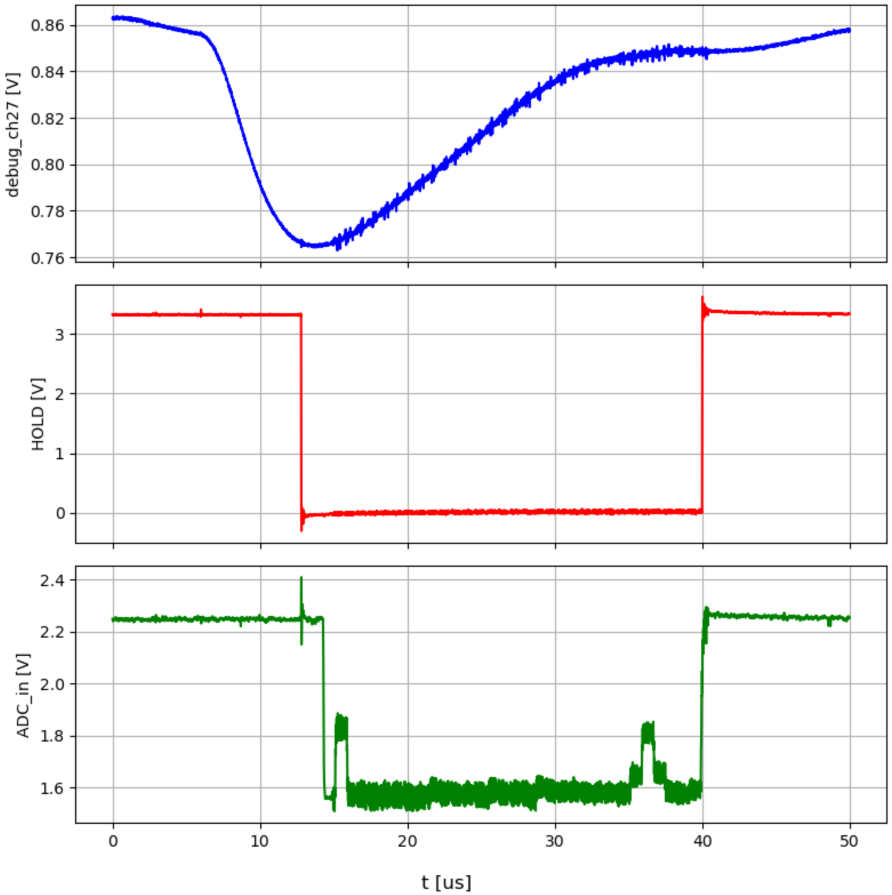
- preAmp: CSA + TP injection circuit
- Slow Shaper branch for charge measurement with externally controlled S&H circuit
- Analogue readout: MUX-differential output buffer
- Digital readout: Wilkinson ADC and serialiser
- Trigger output: Fast Shaper branch providing a fast-OR output

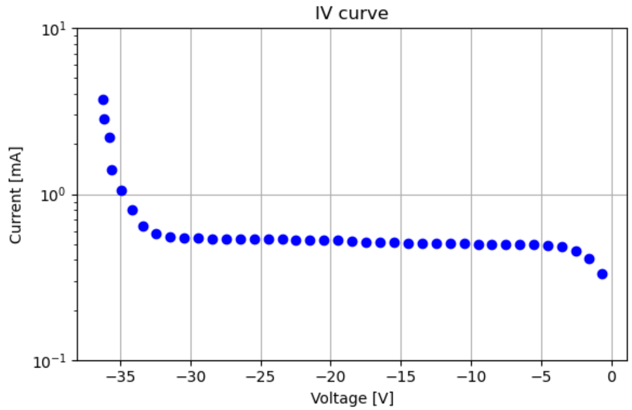


“A mixed-signal read out ASIC for silicon micro-strip detectors” (Mattia Barbanera), today at 12:15.

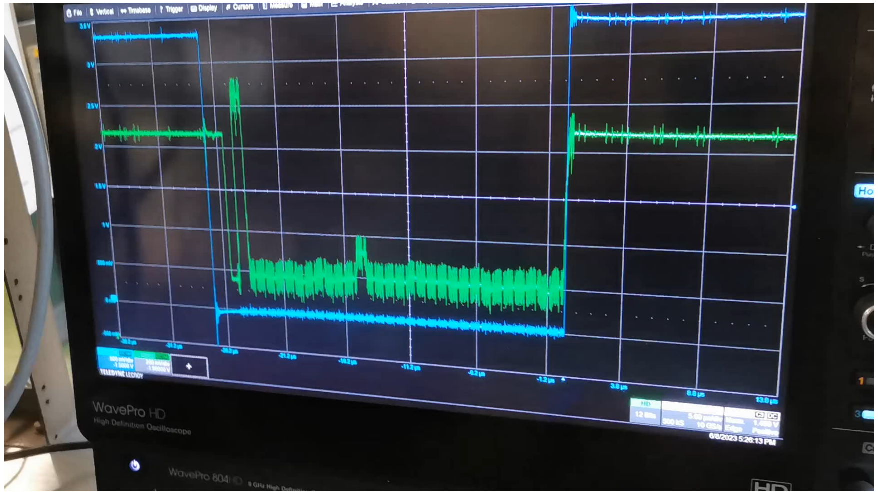
FD Monolithic Active Microstrips

First tests with ^{90}Sr





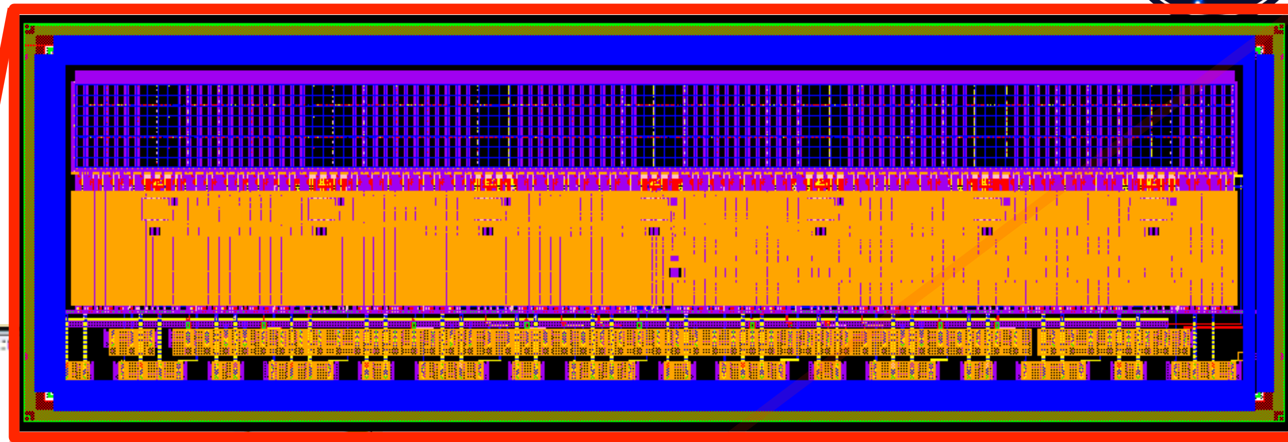
- ASTRA FastOR signal provides trigger to the FPGA
- FPGA sends HOLD signal and then start readout of analogue MUX

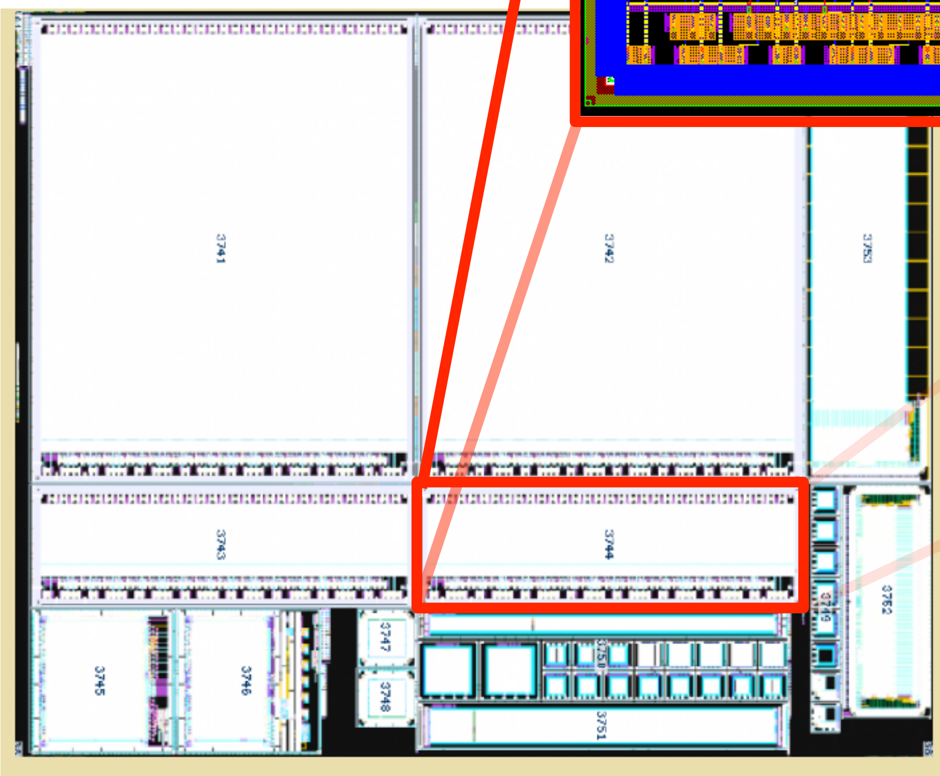


X-ray photon-counting demonstrator

896-pixel demonstrator

(8 x 112 pixels, 100um pitch)

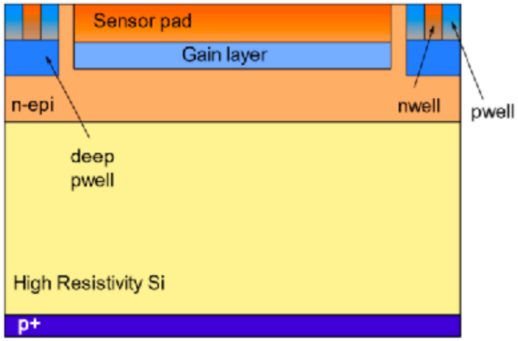


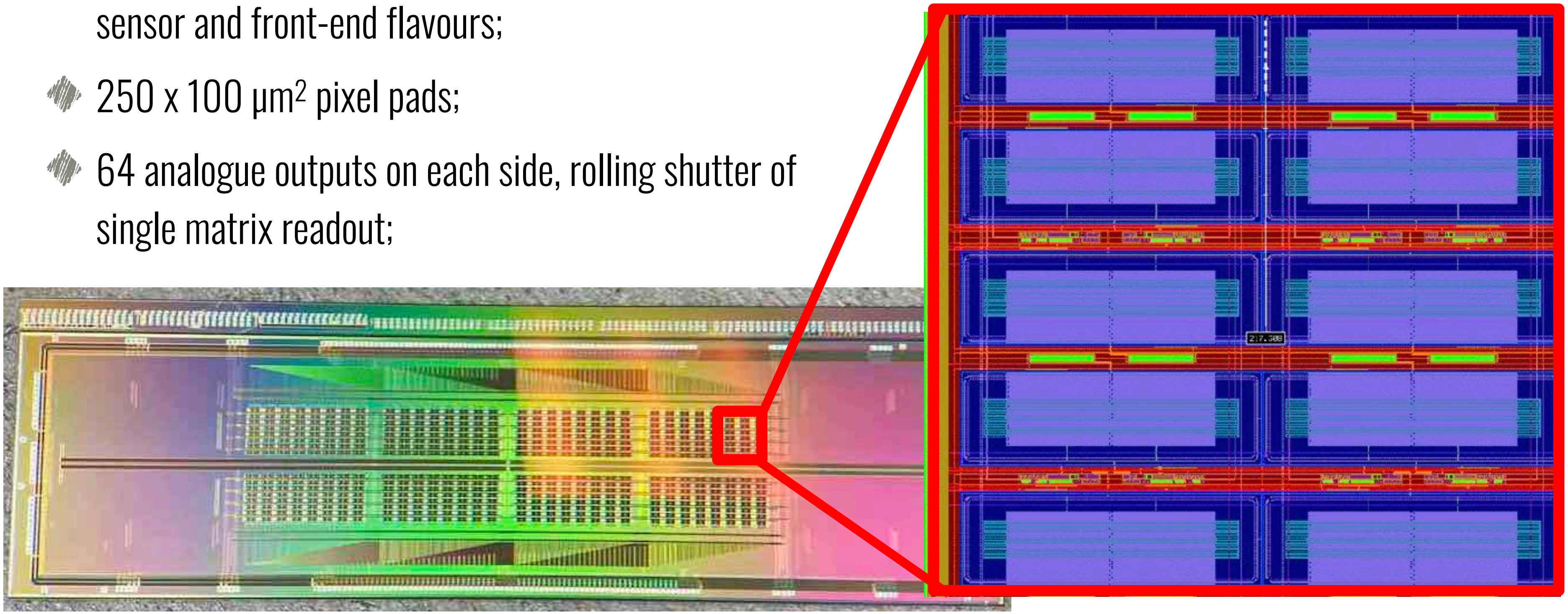


- Project tapeout with ARCADIA ER3
- Shall allow to test both a hybrid assembly of a CdTe detector and a fully-depleted CMOS silicon sensor X-ray imager (half of the matrix with bump pad connections for flip-chip assembly)
- (left) reticle floorplan for the ARCADIA engineering run and (top) CAD layout of the X-ray ASIC [13.4 x 4.2 mm] mini-demonstrator

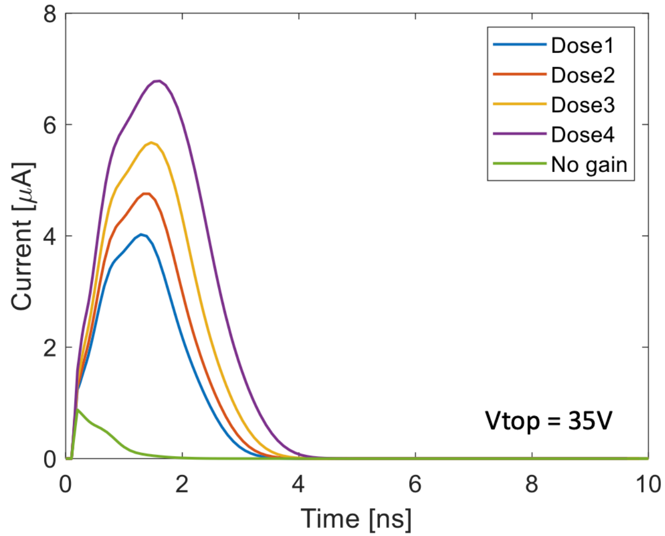
ARCADIA Sensor: R&D for fast timing

- partial lot of HR and p+ wafer splits implement an extra gain layer added to the sensor;
- first small-scale demonstrator 4 x 16 mm^2;
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- 250 x 100 μm^2 pixel pads;
- 64 analogue outputs on each side, rolling shutter of single matrix readout;

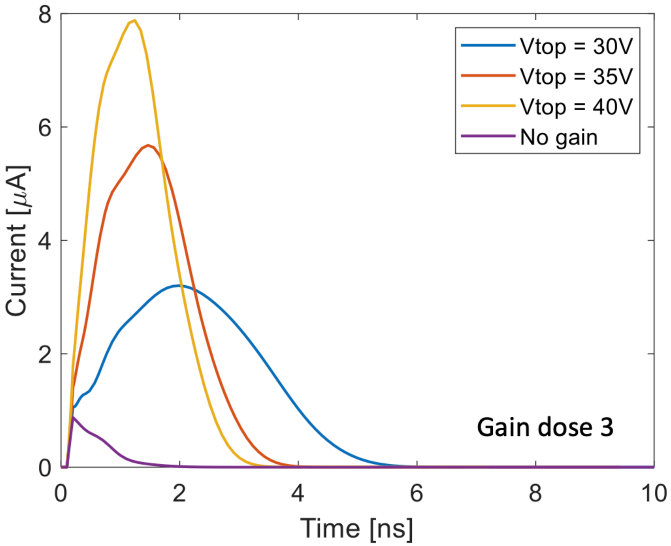




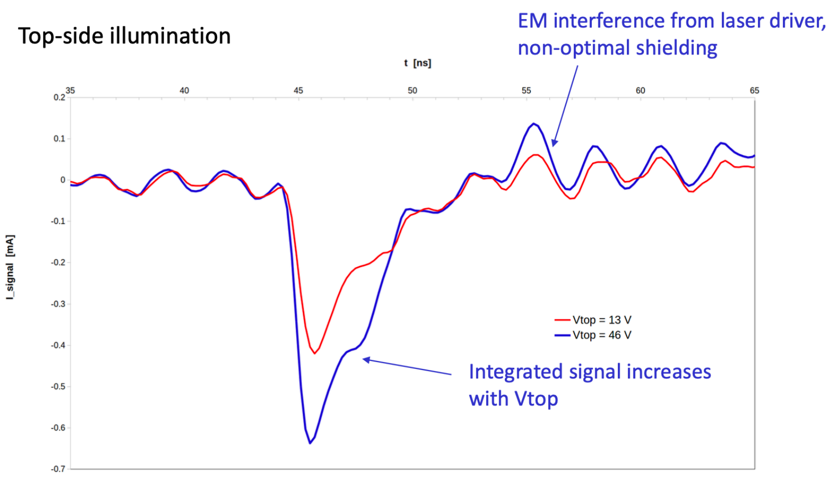
ARCADIA Sensor: R&D for fast timing



TCAD simulations with MIP-like signal

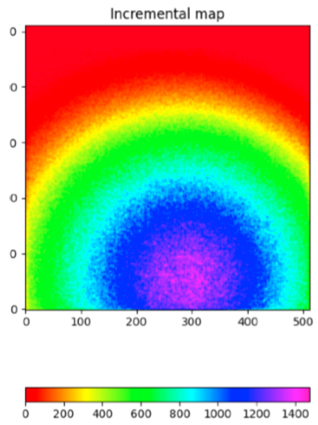


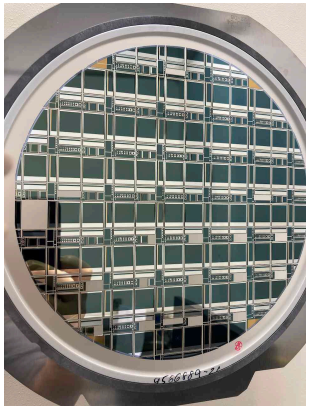
- 50μm active thickness, different gain dose splits, **gain target: range 10 - 30**
- first 200μm (BSI) devices powered on, C-V curve measured on the pad with gain suggest that the gain layer is present, though with n-type substrate the profile can not be completely evaluated
- 50μm devices just received from dicing, tests starting soon!

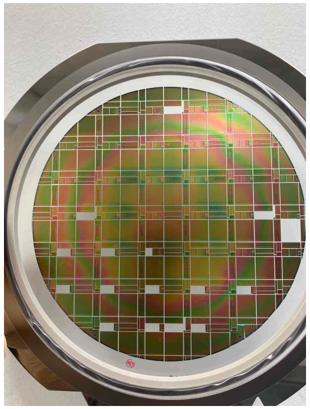


ARCADIA FD-MAPS: Status and Perspectives

- **ARCADIA:** CMOS sensor design and fabrication platform on LF11is technology
  - Sensor R&D and Technology, CMOS IP Design and Chip Integration, Data Acquisition
  - MD3: system-grade full-chip FDMAPS for Medical (pCT), Future Leptonic Colliders and Space Instruments
  - Scalable FDMAPS architecture with very low-power: **10 mW/cm^2**
  - Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
  - Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing
  - Custom BSI process allow to develop fully-depleted thick sensors (400μm) for soft X-ray imaging







Thank you for your time!

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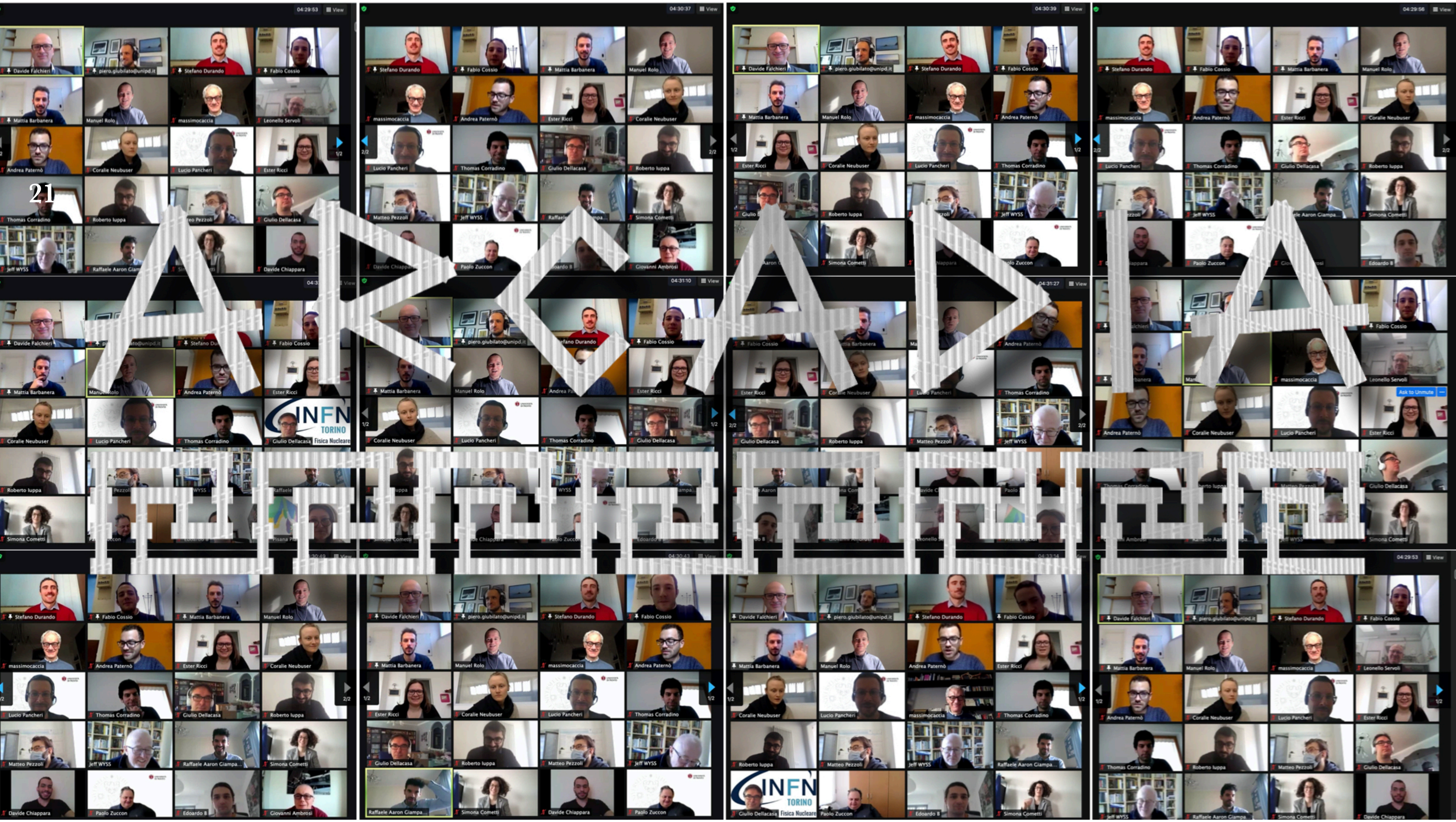
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Front-end FEB-MD3 and DAQ

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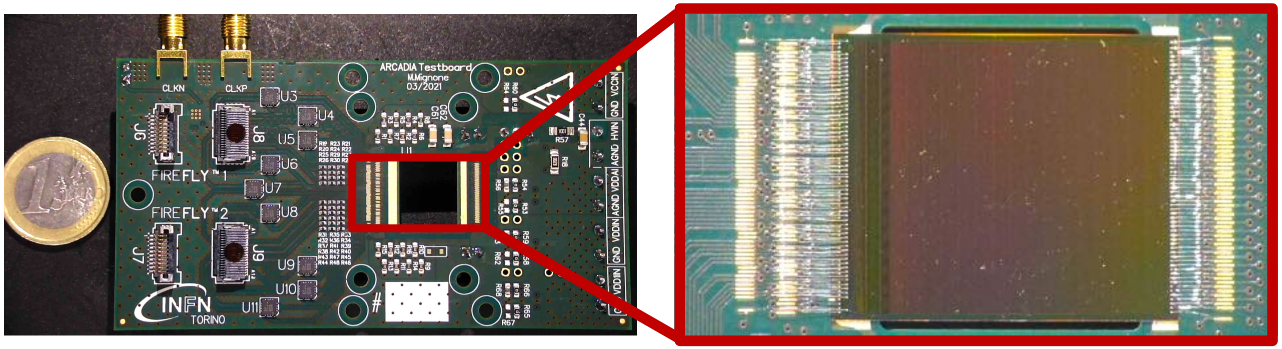
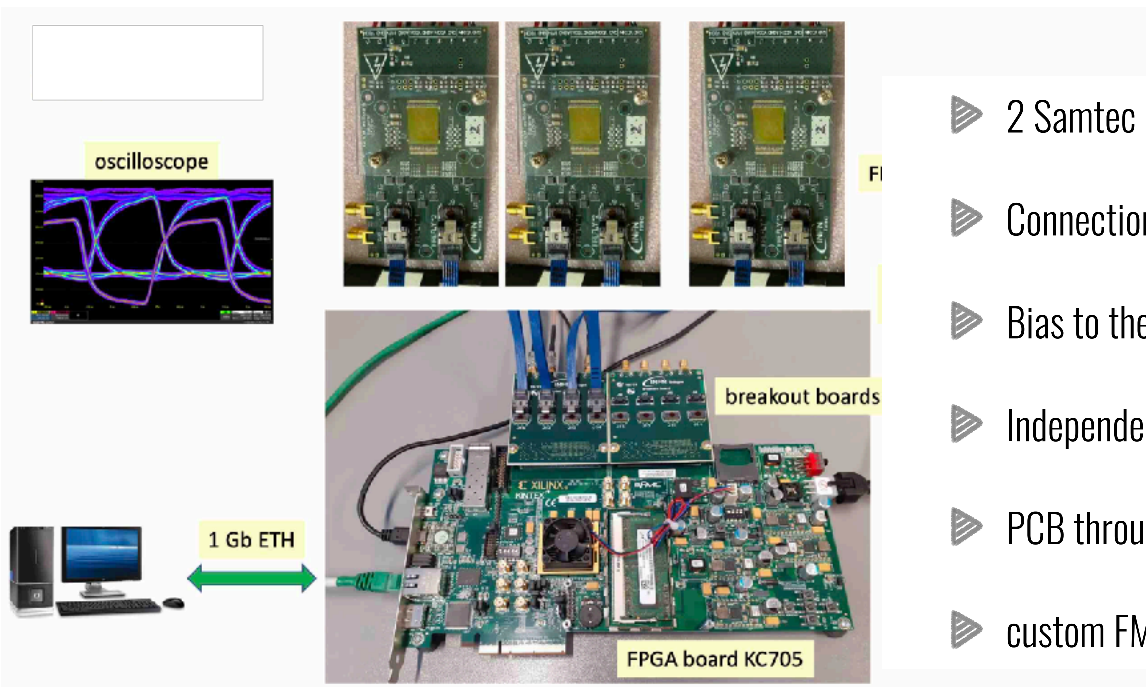




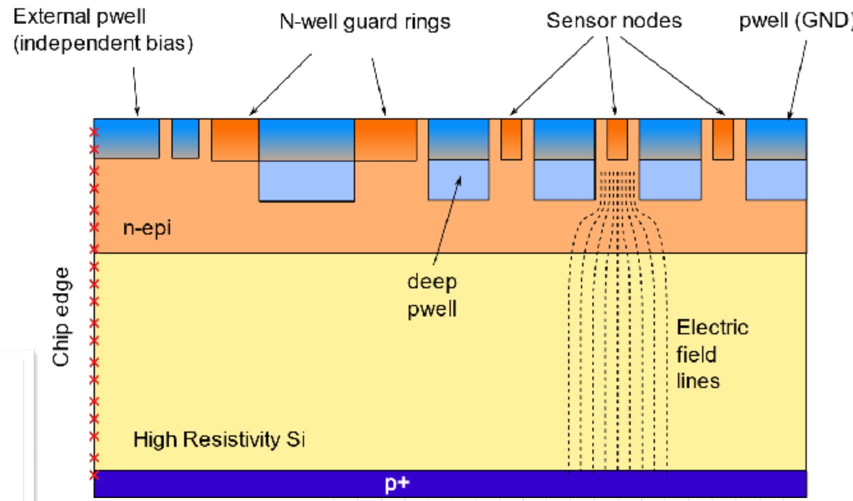
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- Bias to the DMAPS backside or (wirebonded) to top pads
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

ARCADIA pixel test structures

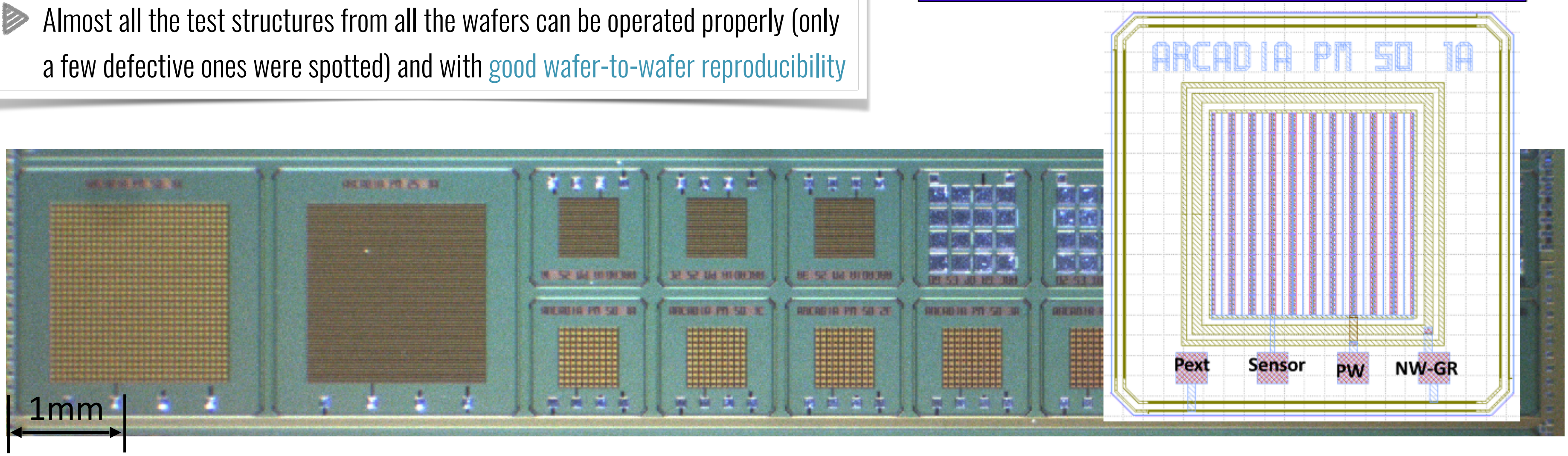
Small pixel arrays with all the pixels connected in parallel.
Pixel pitches: 50um - 25um - 10um

Target characterisation:

- Electrical characterisation: IV and CV curves (at the probe station)
- Pulsed laser characterisation
- Radiation hardness tests (neutrons, X-rays)

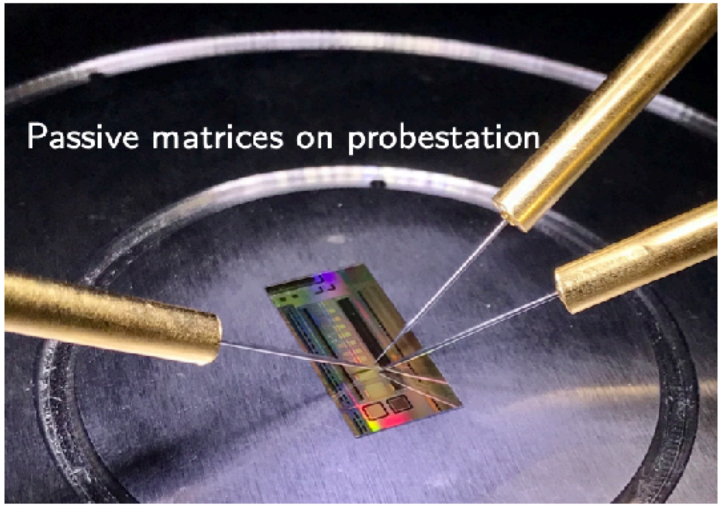


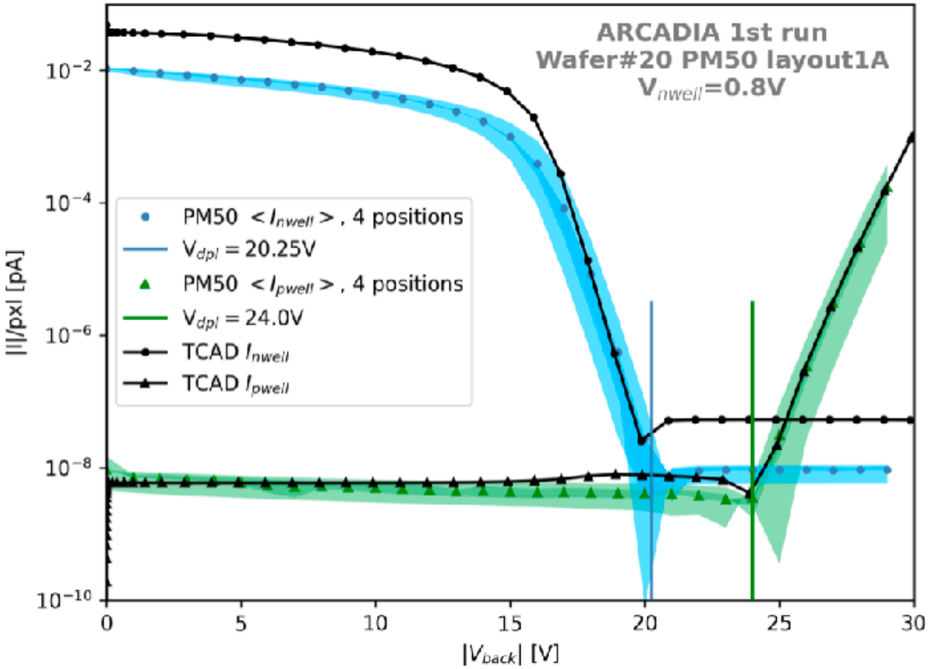
- TCAD simulations have shown a very good predictive power, after tuning the process parameters with IV curves (epi thickness, doping)
- Almost all the test structures from all the wafers can be operated properly (only a few defective ones were spotted) and with good wafer-to-wafer reproducibility

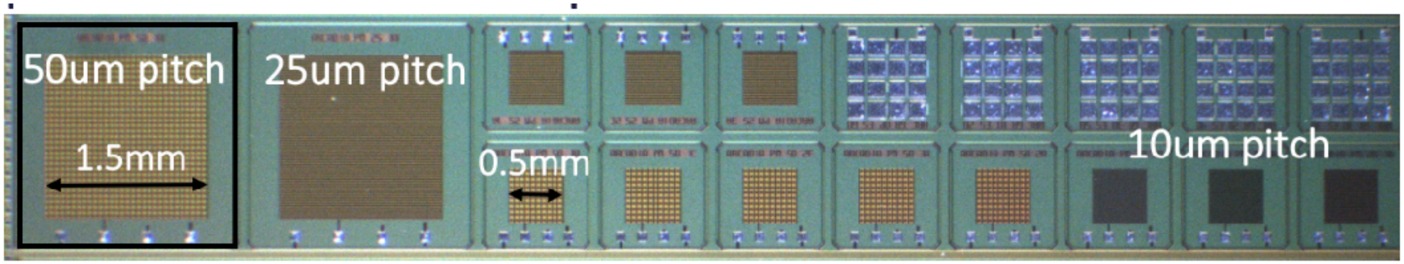


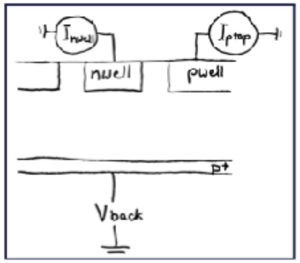
ARCADIA sensor characterisation

IV and CV measurements of test-structures: proven functionality, stable operation at full depletion, and good agreement with TCAD simulations









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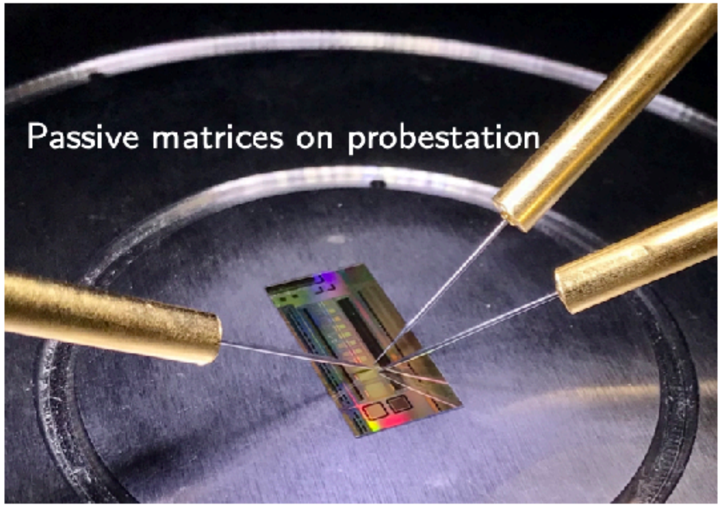
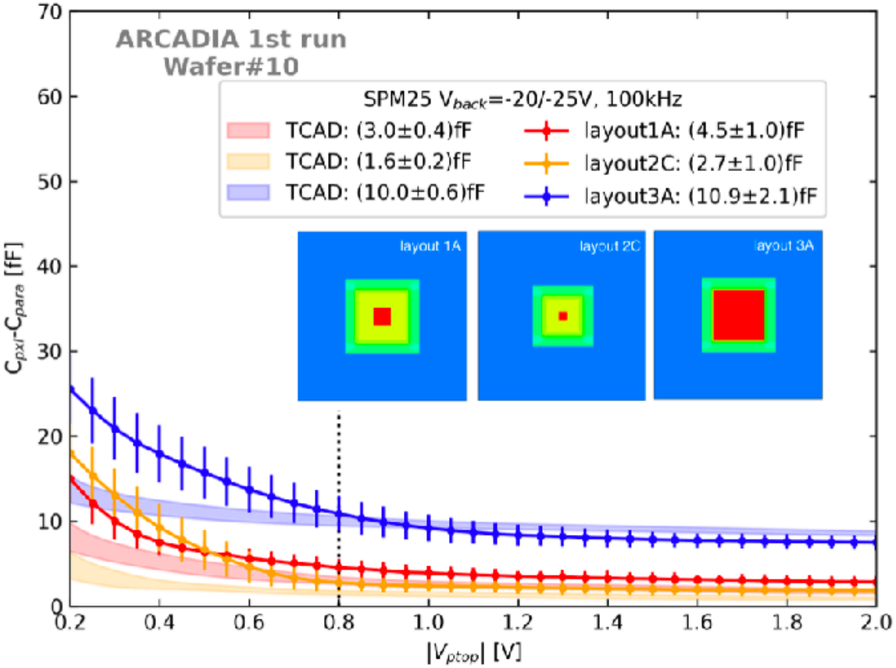
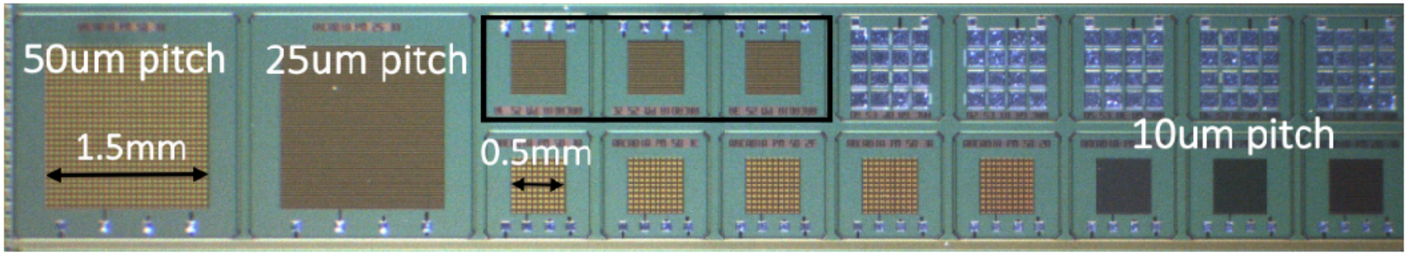
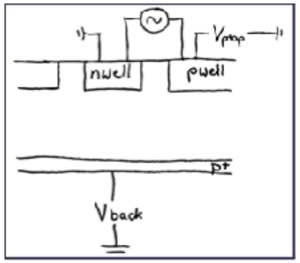




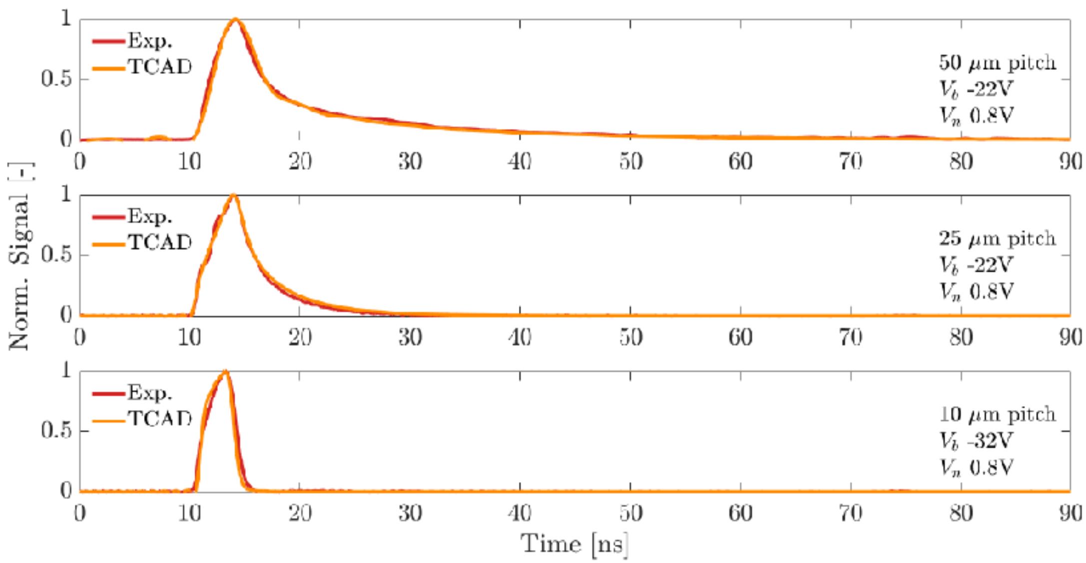


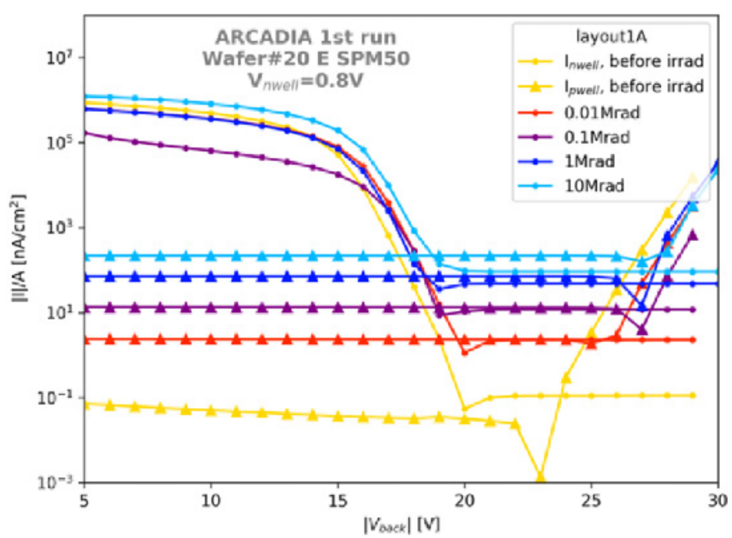


Pulsed laser and radiation damage studies

- Infrared laser diode @ 1060nm, 50ps FWHM: generation in the whole active thickness
- Pixel array test structures with 100um active width (maskless backside p+ implantation)

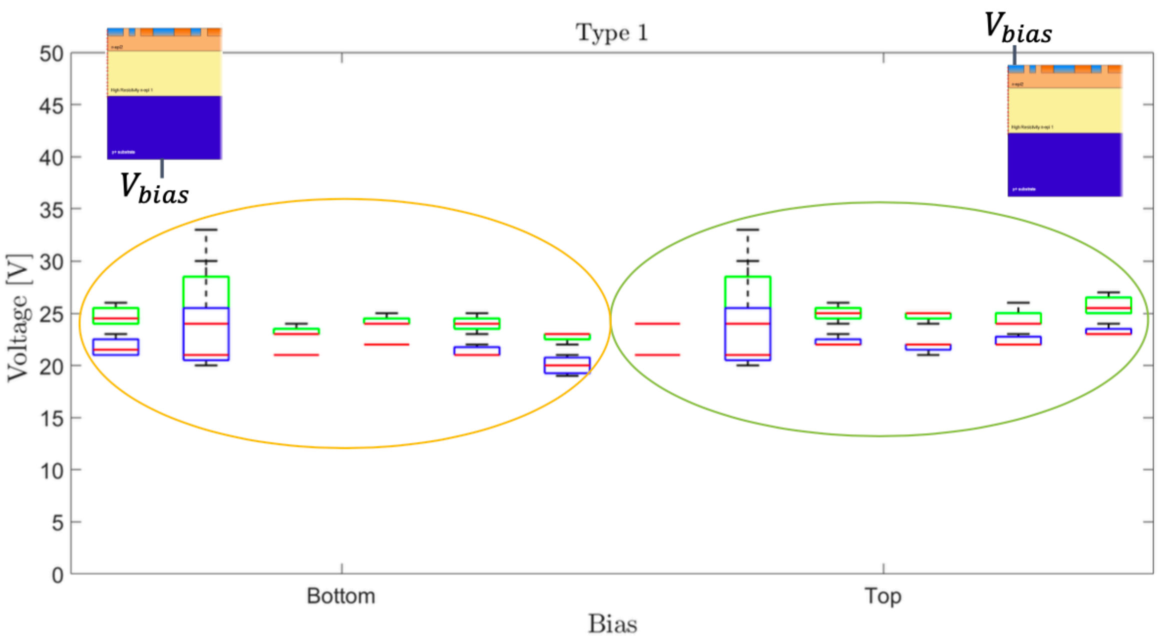
Experimental characterisation of ionising radiation damage: dark current increase with dose from 10 krad to 10 Mrad

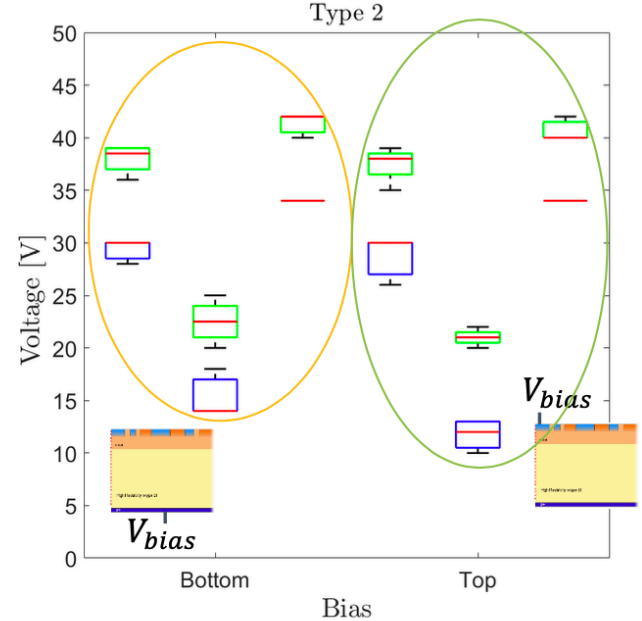




Sensor Biasing

The chip periphery behaves like a resistor: For substrates of Type 1 and 2, substrate bias can be applied both from the bottom and from the top



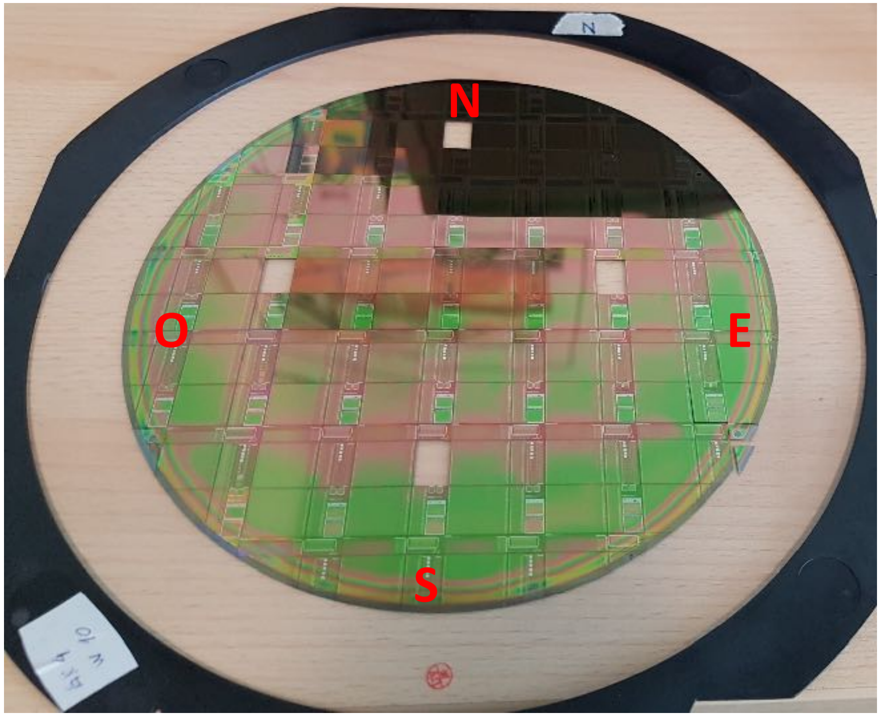


$V\,depl$ and $V\,PT$ are very similar for the two considered biasing schemes

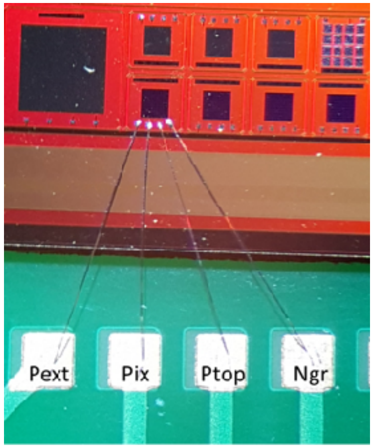
L. Pancheri

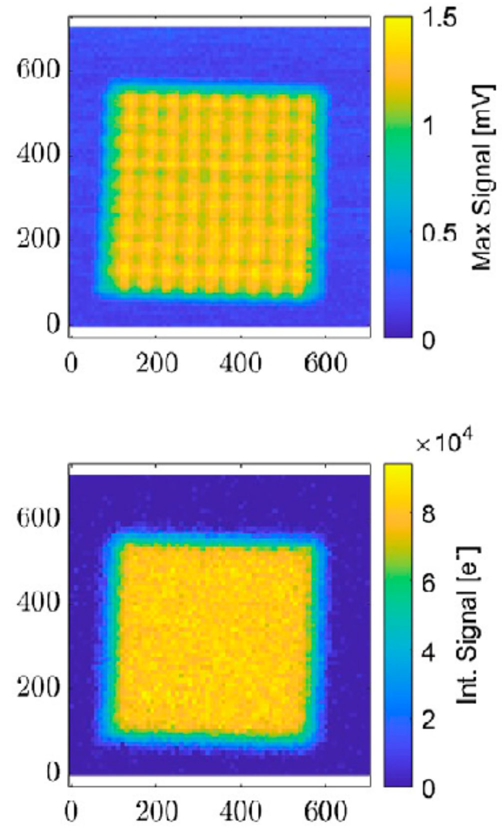
Test structures selection and packaging

At least 4 dies with test structures extracted from each wafer in different positions, to verify uniformity

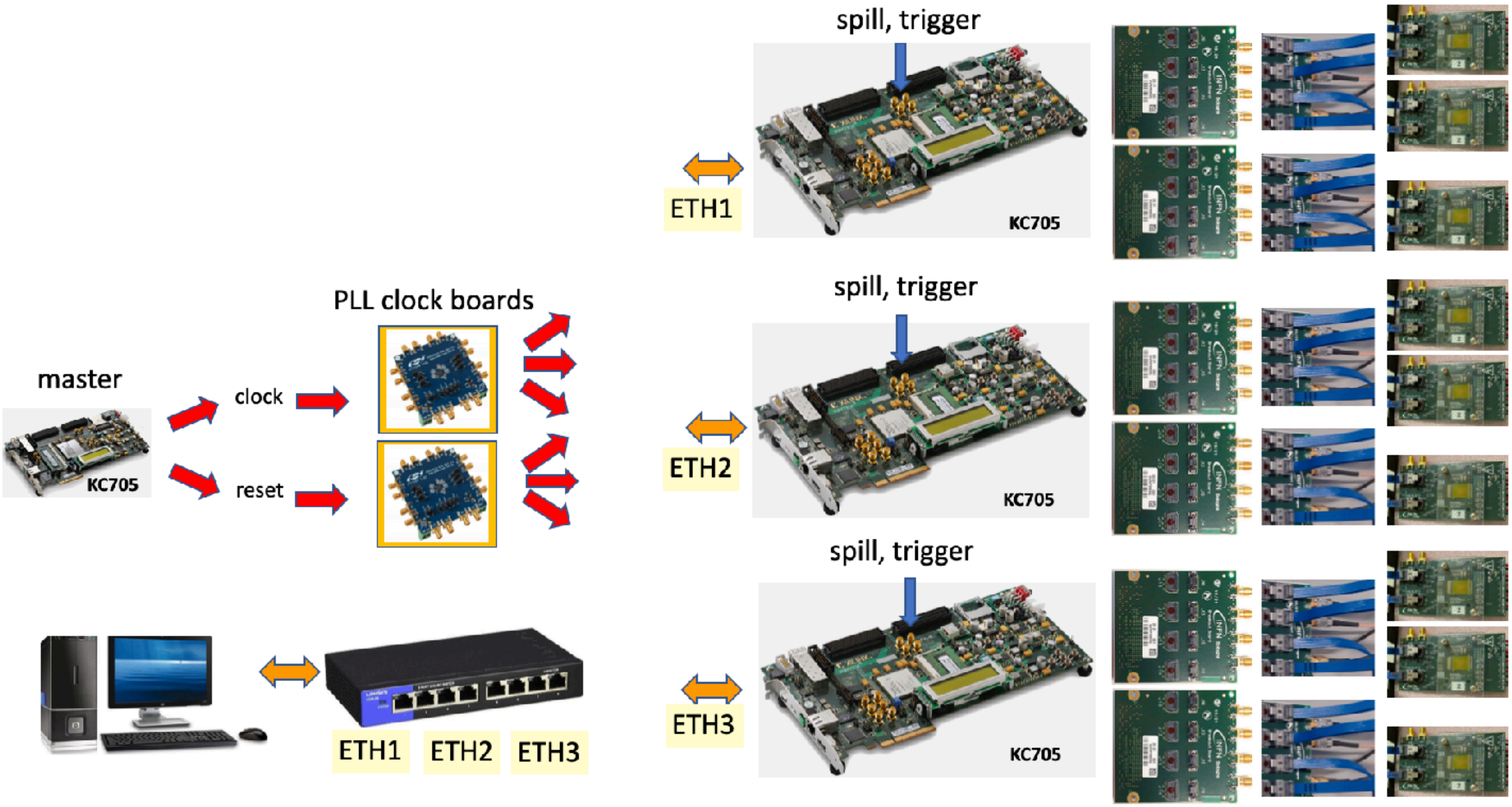


A few devices are bonded for laser irradiation tests: position-dependent signal and time response to short laser pulses (<100ps)

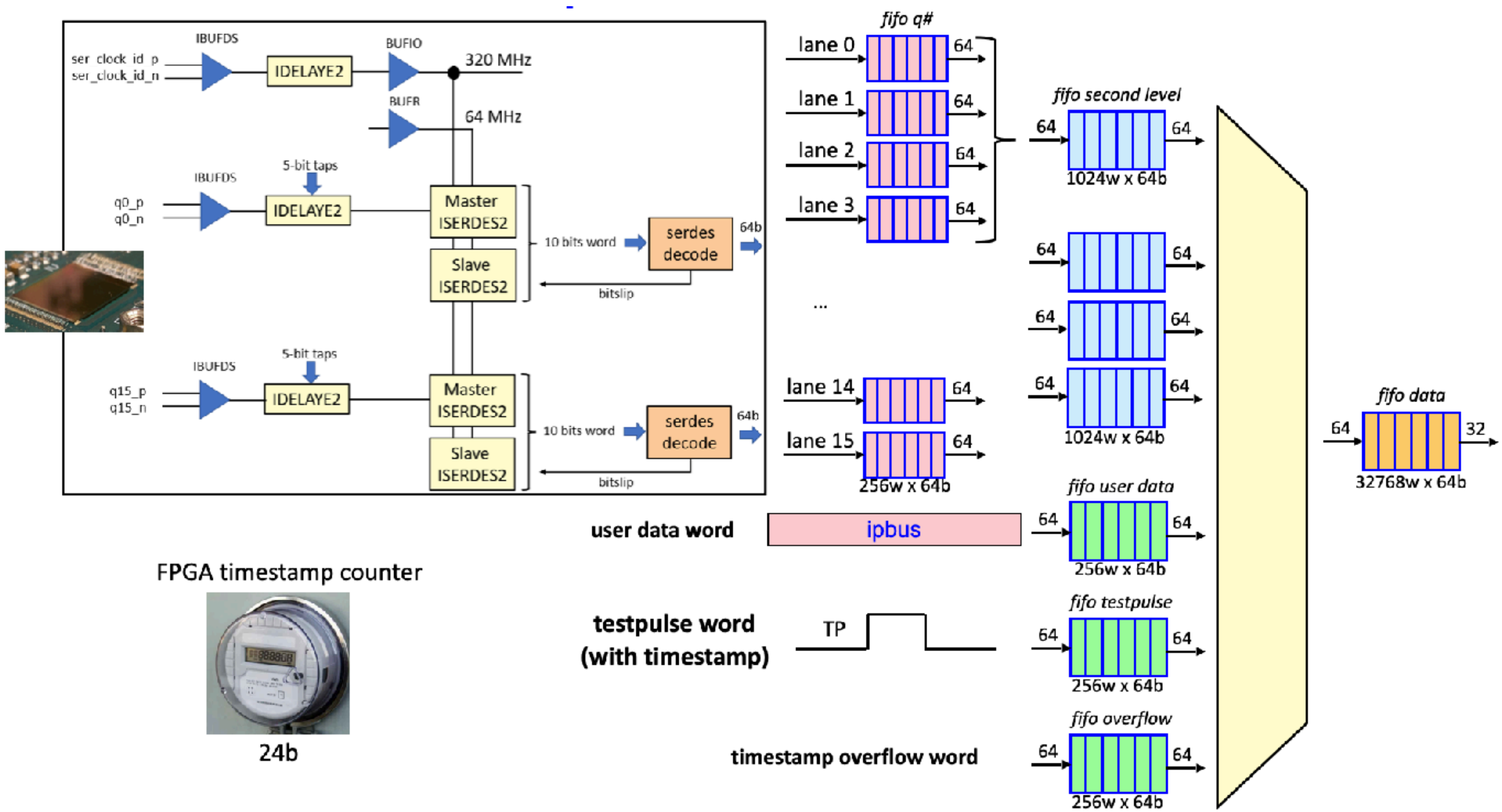




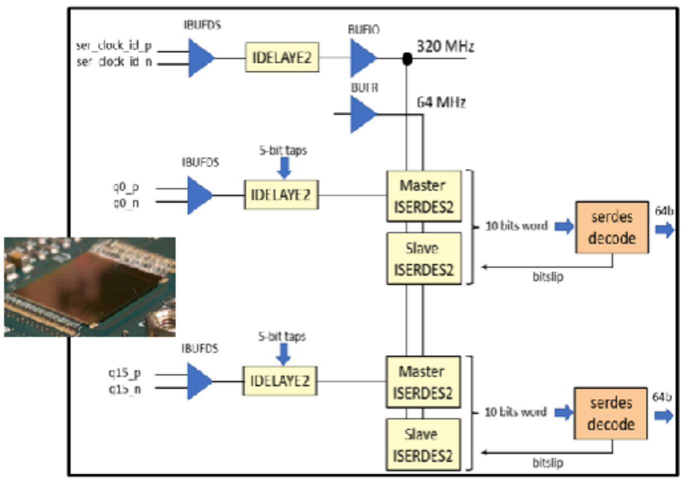
ARCADIA MD3 DAQ Hardware: Telescope



DAQ firmware: data-push architecture

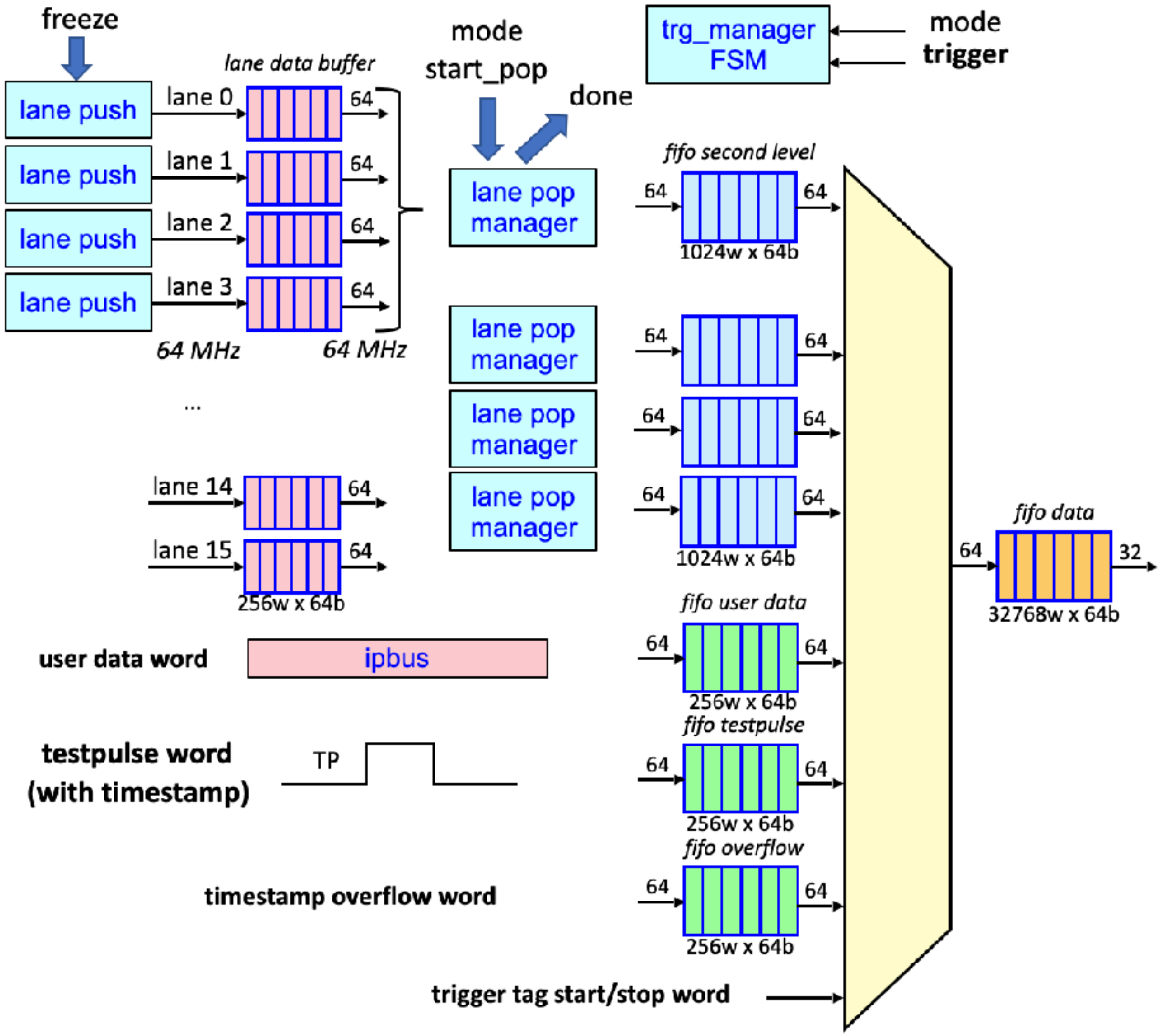


DAQ firmware: triggered architecture

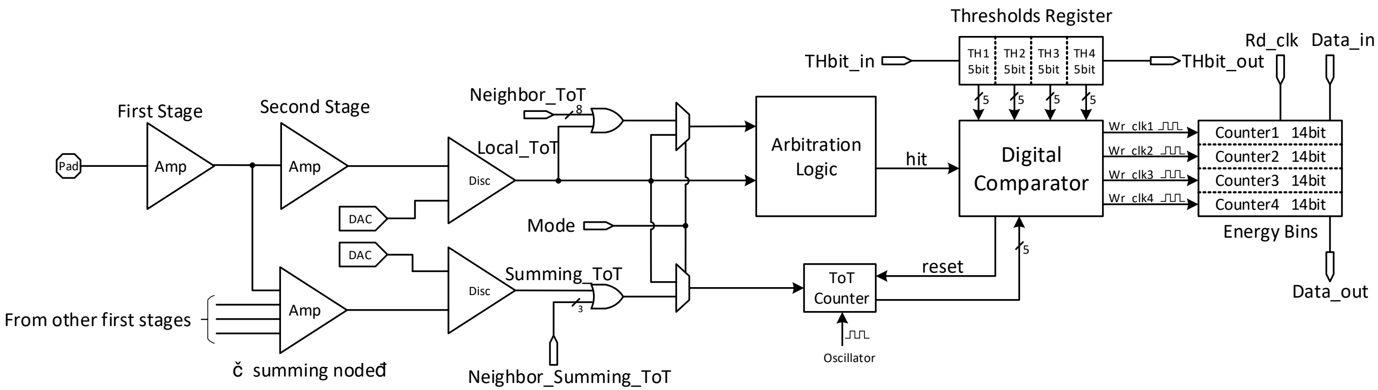


FPGA timestamp counter

24b



Pixel Readout ASIC for photon-counting Architecture and Chip Design



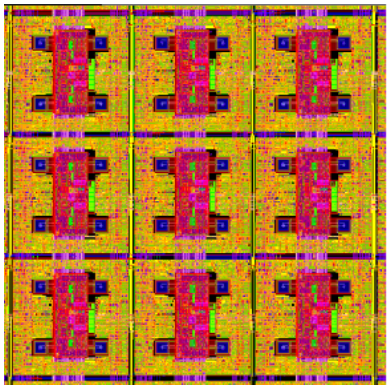
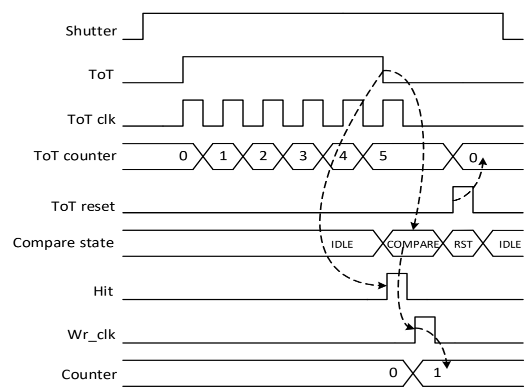
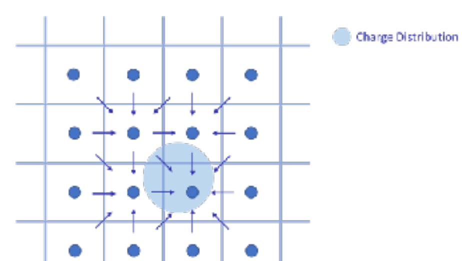


Figure: CAD layout of a 3x3 pixel region (each pixel is built with 2x2 50 μm cores



- ✓ The arbitration logic module compares local ToT with 8 neighbour ToTs to decide if local pixel has the largest read of the generated charge and then the hit signal is pulled up high
- ✓ The deposited energy is obtained by the ToT counter in which the numbers of cycles of oscillator clock is recorded
- ✓ A digital comparator assigns an energy bin to the event



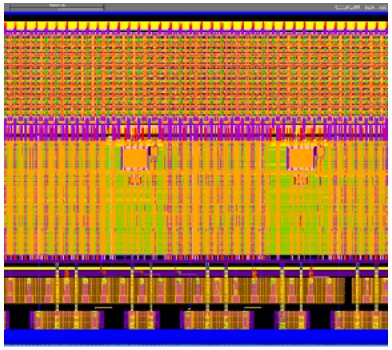


Figure: Data from a super-column (8 double columns) is serialised and sent off-chip with a C-LVDS transceiver

Pixel Readout ASIC for photon-counting
Sensor and simulation setup

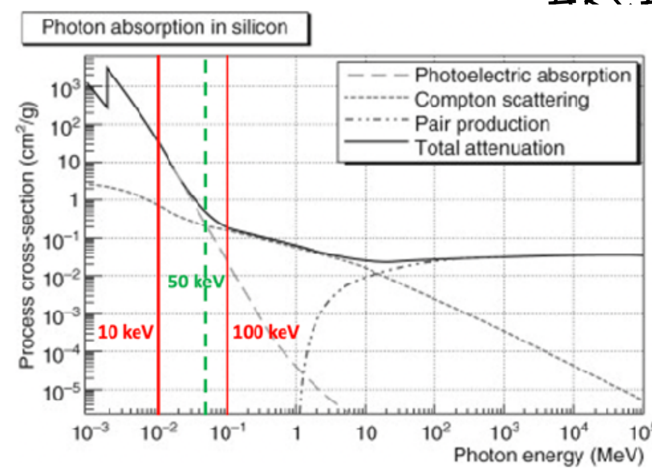
X-ray energy range: 10 - 100 keV, Photoelectric + Compton effects

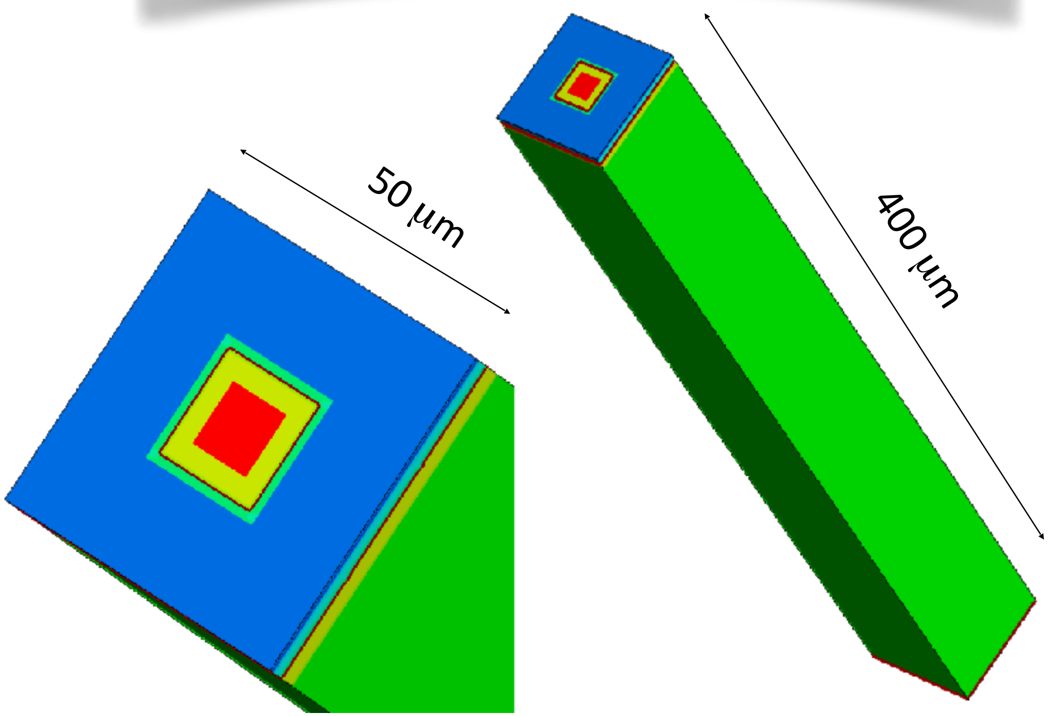
50 μm pitch, 400 μm thick ARCADIA pixel sensor

Punch through onset V_{pt} = -363.6 V

Capacitance @ V_{pt} = 12.8 fF

Voltage at collection electrode = 0.8 V





Scope:

- study charge sharing
- charge collection time < shaping time ~ 100 ns

Sentaurus TCAD

- electric and weighting field maps

Allpix2

- Monte Carlo signal generation
- 5x5 pixel matrix

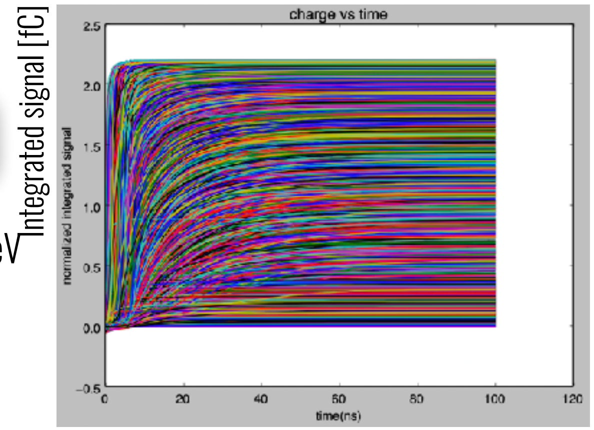
Pixel Readout ASIC for photon-counting
Signal simulation for 50 keV photons

Compton scattering

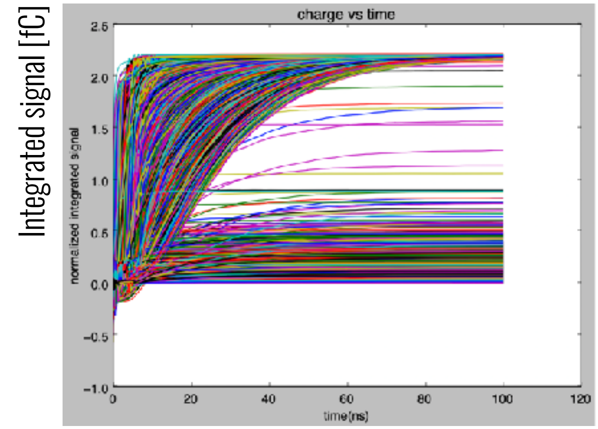
- Fraction of energy transferred to recoil electron: 9% mean, 17% max
- Charge deposit: 0.2 fC mean, 0.38 fC max

Photoelectric absorption

- K-shell 1s electron binding energy = 1.839 keV
- Kinetic energy of K-shell 1s photoelectrons
- = 50 keV – 1.839 keV
- Charge deposit: 2.14 fC



Central pixel signal only



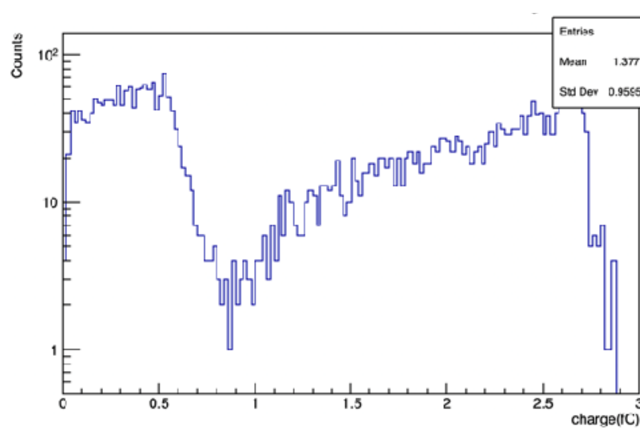
Full 5x5 matrix signal

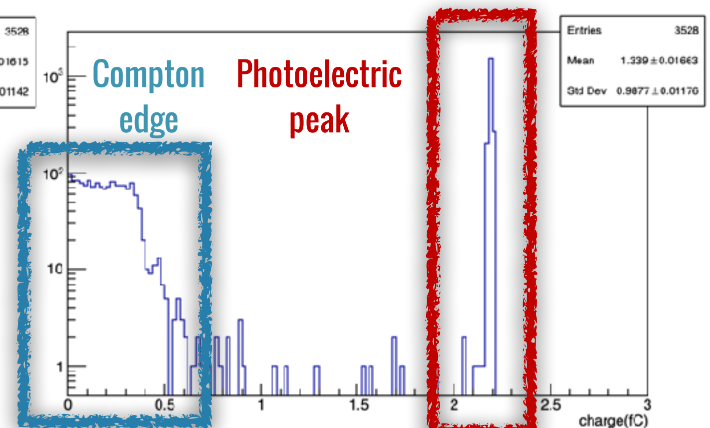
Monte Carlo simulation

- 100k incoming photons
- Perpendicular incidence
- Random incidence point over the CENTRAL pixel of the 5x5 matrix

Detected photons (Compton + photoelectric, no threshold) = 3528

Detection efficiency = ~4%





Collected charge [fC]