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A Configurable 64-channel ASIC for Cherenkov Radiation Detection

ASI-INFN agreement for EUSO-SPB2 n. 2021-8-HH.0

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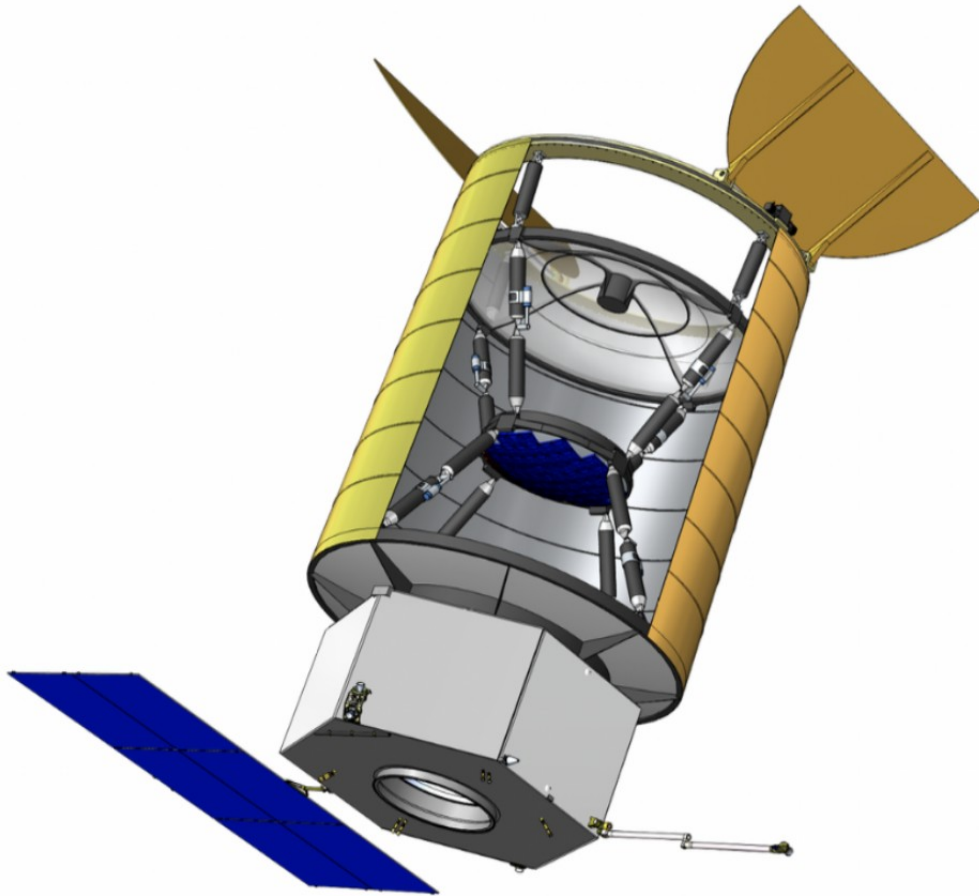A. Rivetti[1], M. E. Bertaina[1, 3], Antonio Palmieri[1, 3]

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[2] Politecnico di Torino – Department of Electronics and Telecommunications, Torino, Italy.

[3] University of Torino – Physics Department, Torino, Italy.

Angela V. Olinto, POEMMA and EUSO-SPB: Space Probes of the Highest Energy Particles, 2018

- Detection of **Extensive Airshowers** (EASs) generated by **Ultra-High Energy Cosmic Rays** (UHECRs) beyond 100 PeV and **Cosmic Neutrinos** (CNs) through Cherenkov radiation processes.
- The fast sampling of the signal is mandatory: 200 MHz.
- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- A system to readout a camera plane composed by a matrix of Silicon Photo-Multipliers (SiPMs).

2

SiPMs plane

ASICs plane

FPGAs plane
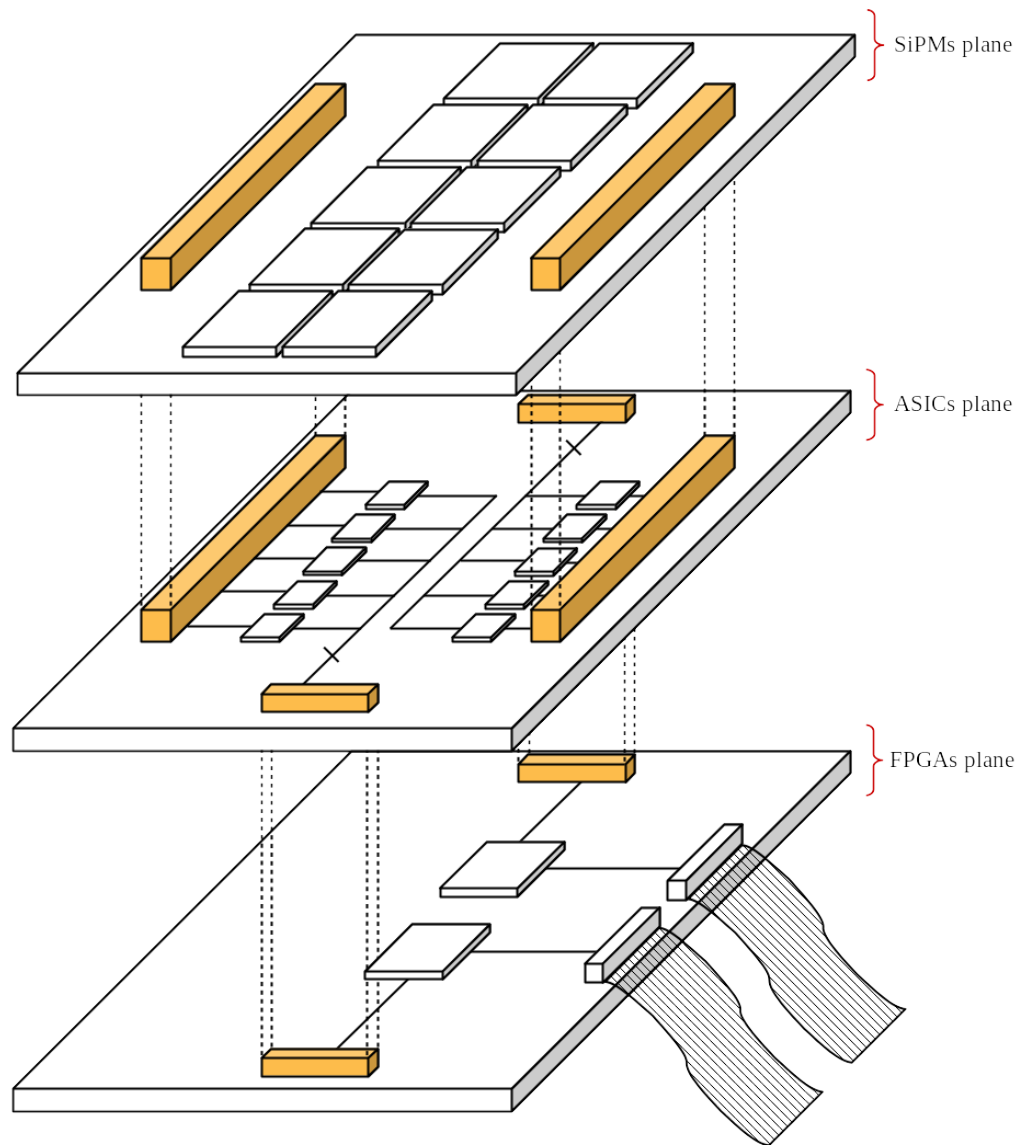
- 3 planes:
  - SiPMs
  - ASICs
  - FPGA
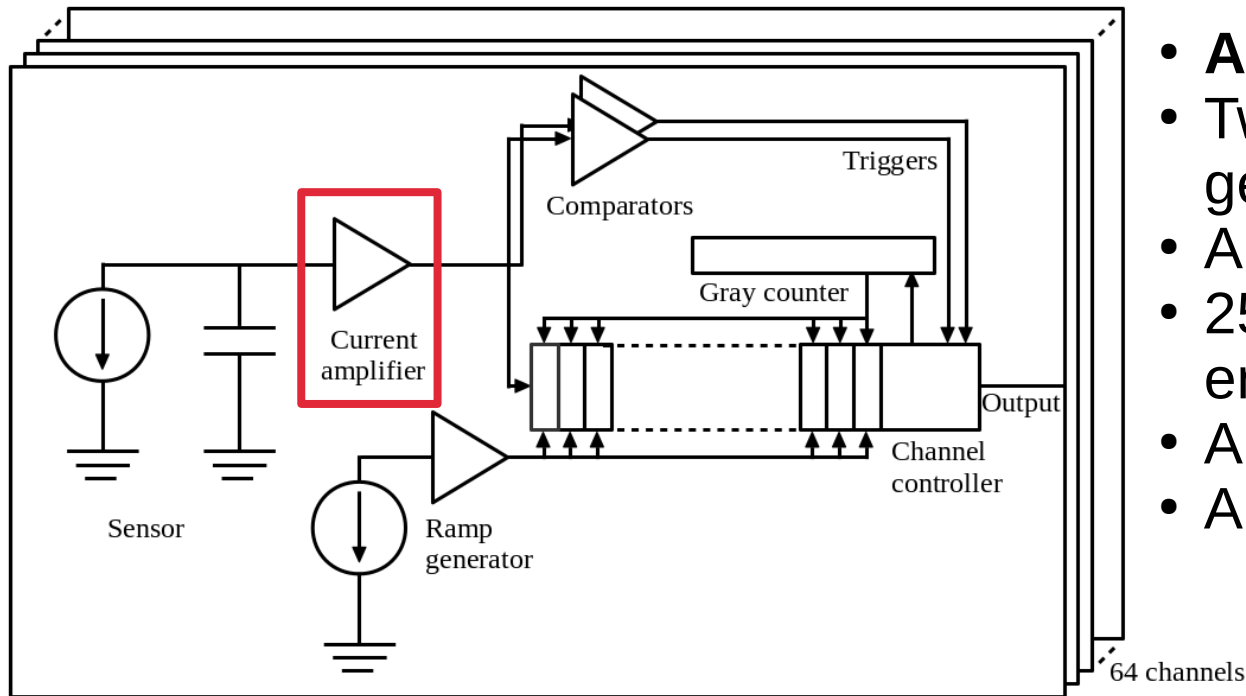- 2 FPGAs to split the readout of the ASICs.
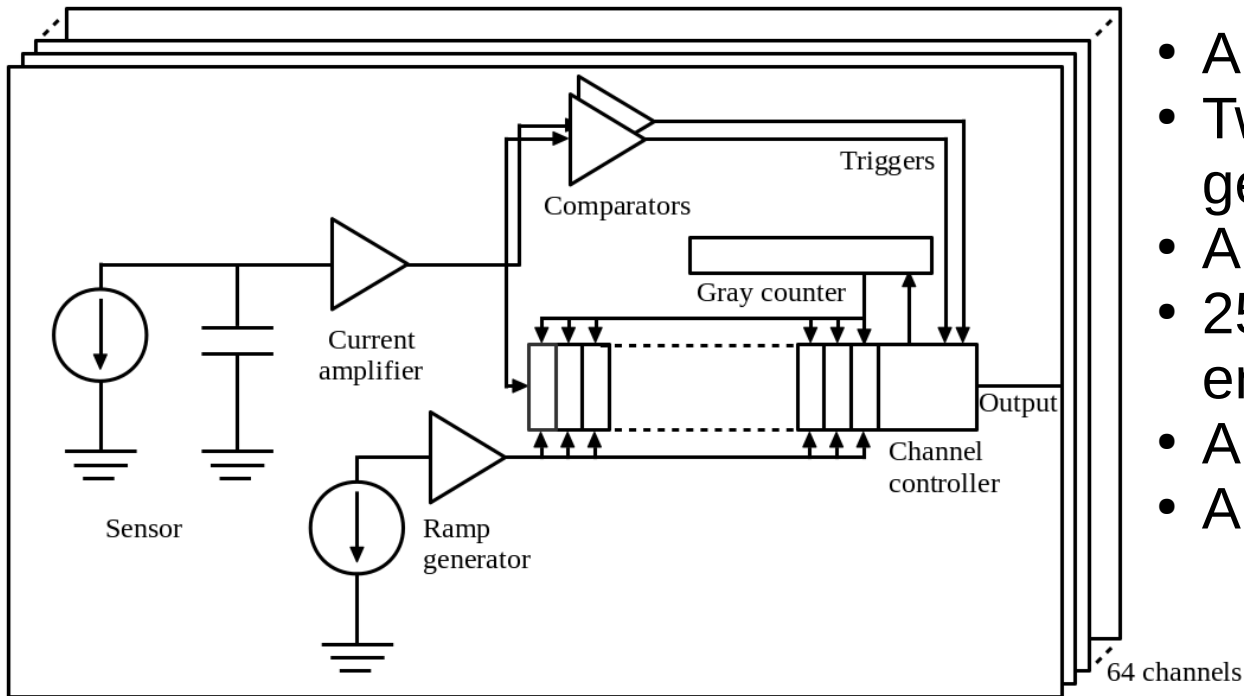
3

ASIC architecture

- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.

No full sampling system.

- **An input amplifier**.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
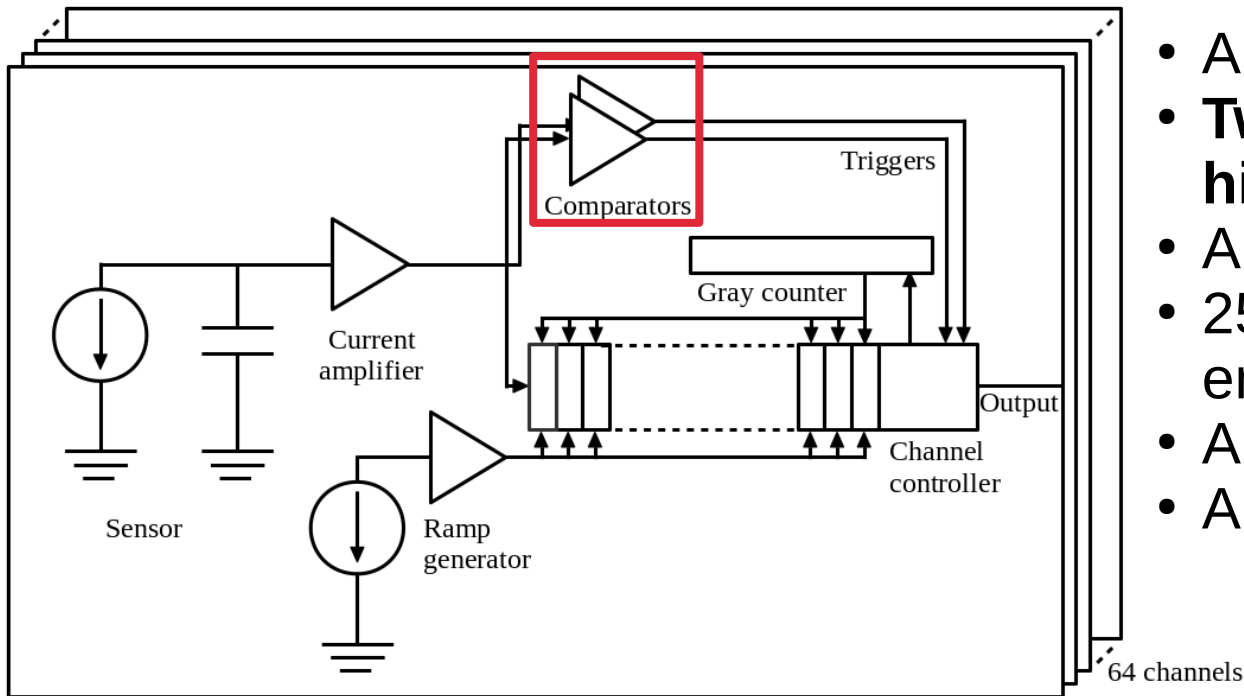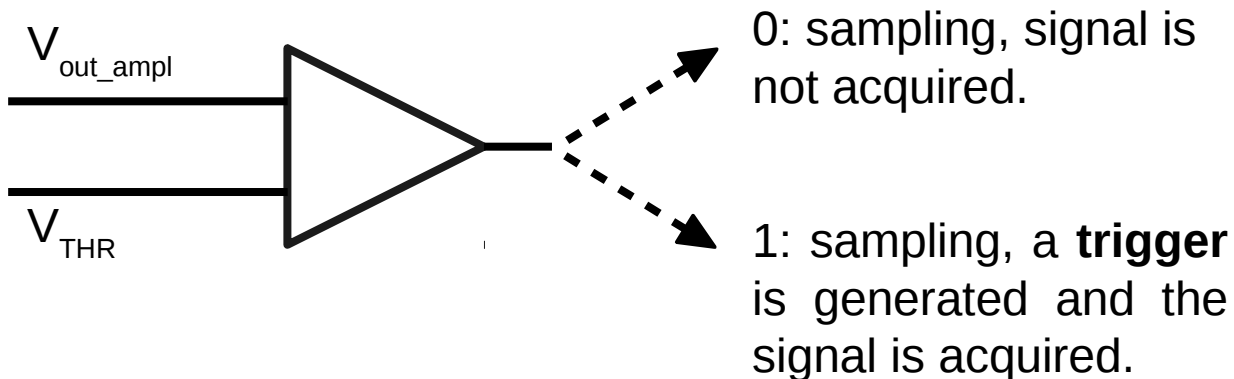- A ramp generator.
- A digital Gray counter.

- An input amplifier.
- **Two comparators for hitmaps generation.**
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
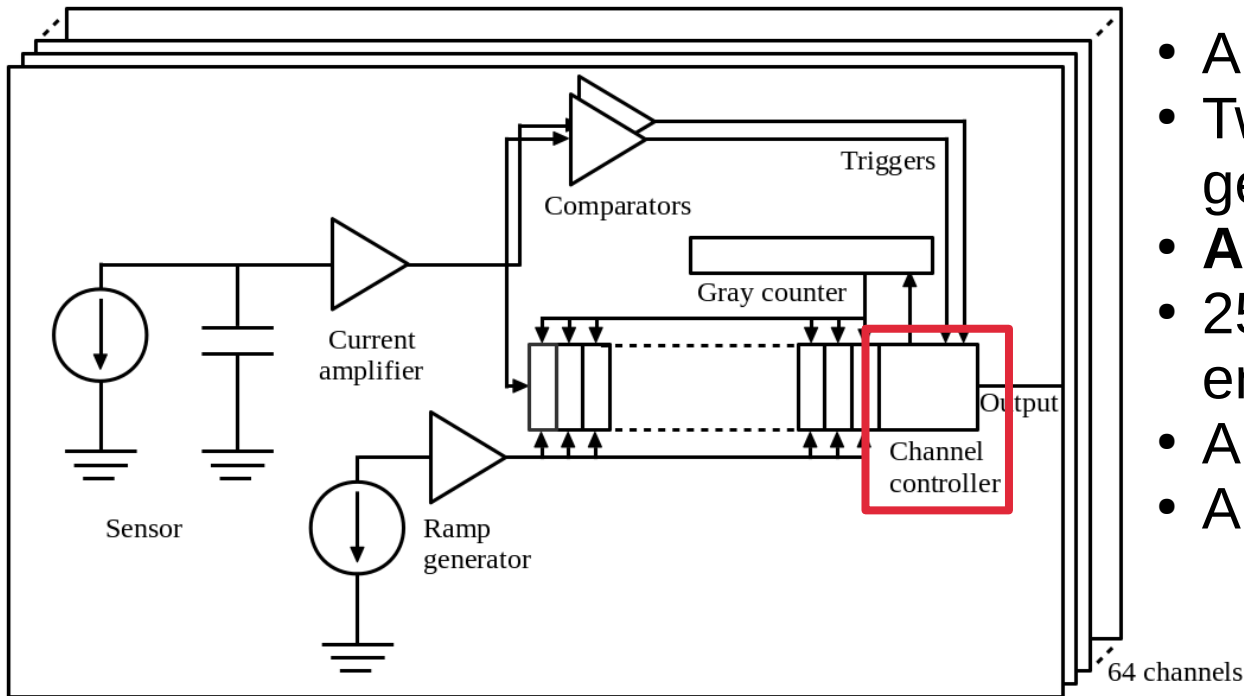- A digital Gray counter.

V_{out_ampl}

V_{THR}

0: sampling, signal is not acquired.

1: sampling, a **trigger** is generated and the signal is acquired.

6

- An input amplifier.
- Two comparators for hitmaps generation.
- **A digital channel controller.**
- 256 memory cells with embedded Wilkinson ADC.
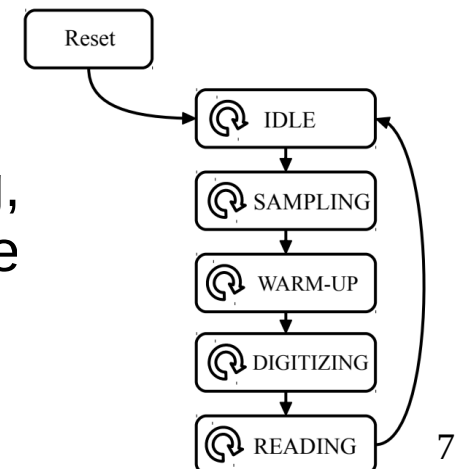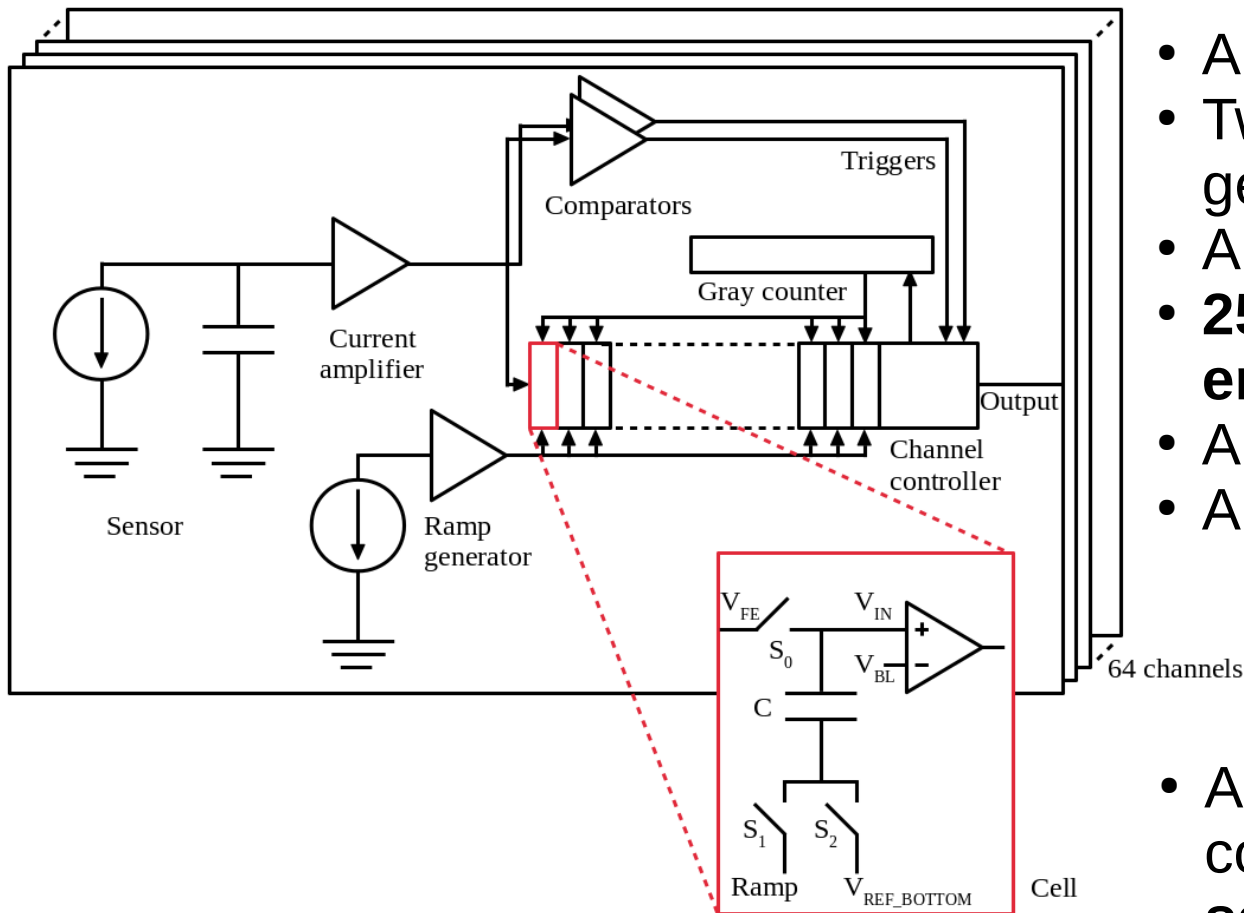- A ramp generator.
- A digital Gray counter.

- Manager of the sections (namely of the cells).
- The cells must address **5 states**: idle, sampling, warm-up, digitizing and reading. These processes are implemented with a **Finite State Machine** (FSM).
- **Channel configurability** (256, 64, 32 cells).
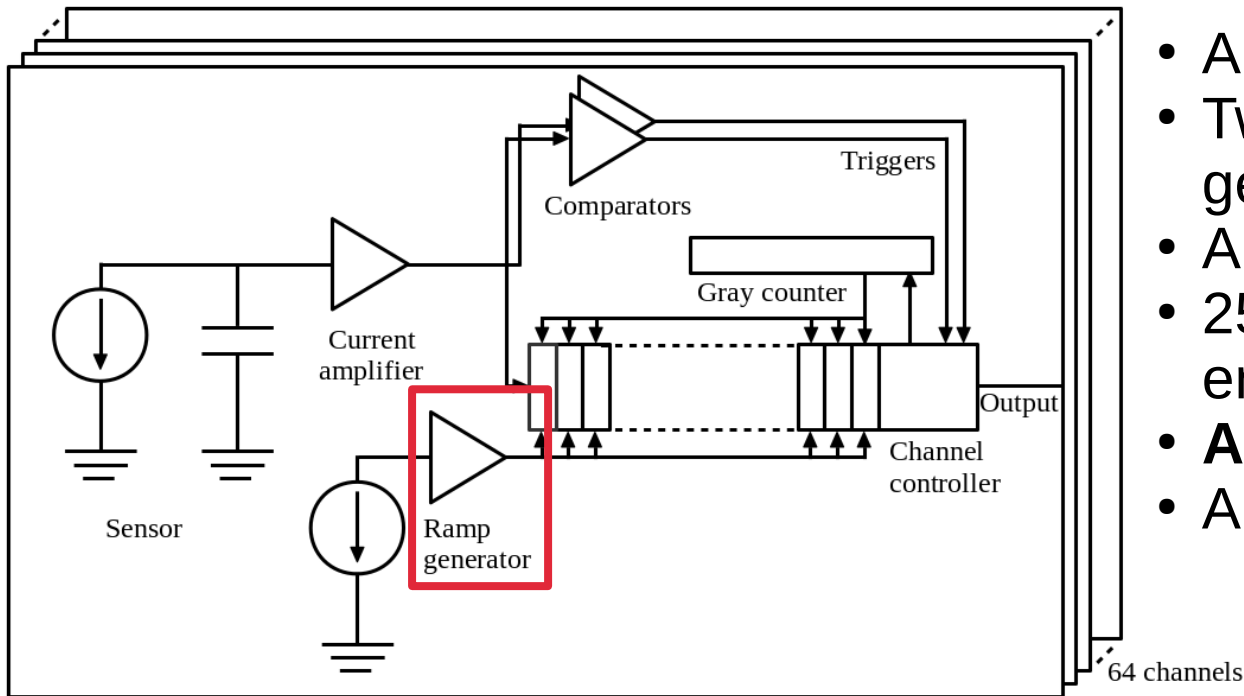
7

ASIC architecture

- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- **256 memory cells with embedded Wilkinson ADC**.
- A ramp generator.
- A digital Gray counter.

- A single ramp generator is connected to all the cells → **same gain**.

- The 256 cells are partitioned into smaller **segments** to **derandomize** the incoming signal: a group of 32 cells is organized into a **section**. The chip can be configured to operate with 32, 64 or the full 256-cells depth.

8

- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- **A ramp generator.**
- A digital Gray counter.
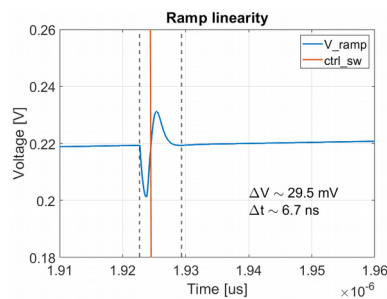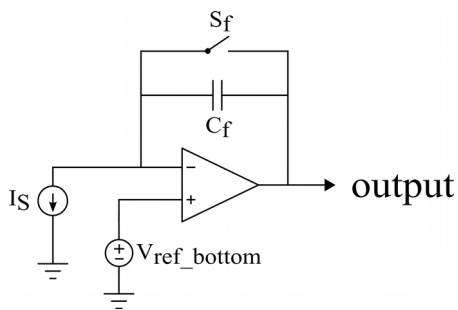
- **Sampling**: the switch is closed so the output is equal to the reference voltage.
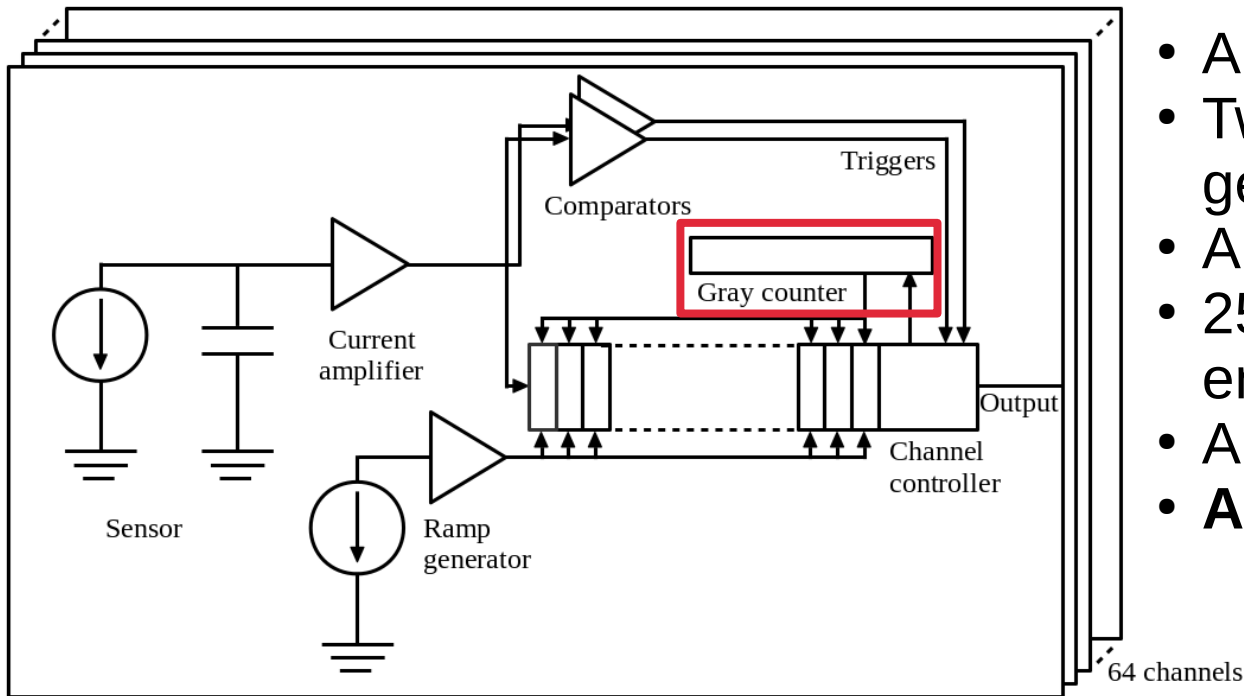- **Conversion**: the switch is open and C_f integrates the current thus providing a ramp.

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- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- **A digital Gray counter.**

- It is exclusively driven by the channel controller and enabled during the **digitizing** process.
- The counter is progressively increased by one at each clock cycle until the saturation of the counter itself occurs. The ramp generator is accordingly activated during this time window.
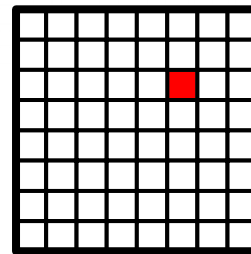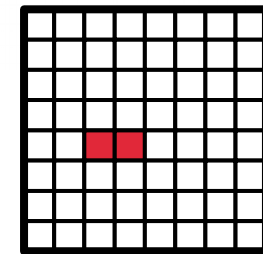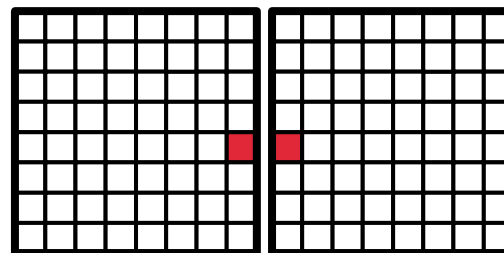- **Configurable** in the range 8-12 bits.

FSM simulation
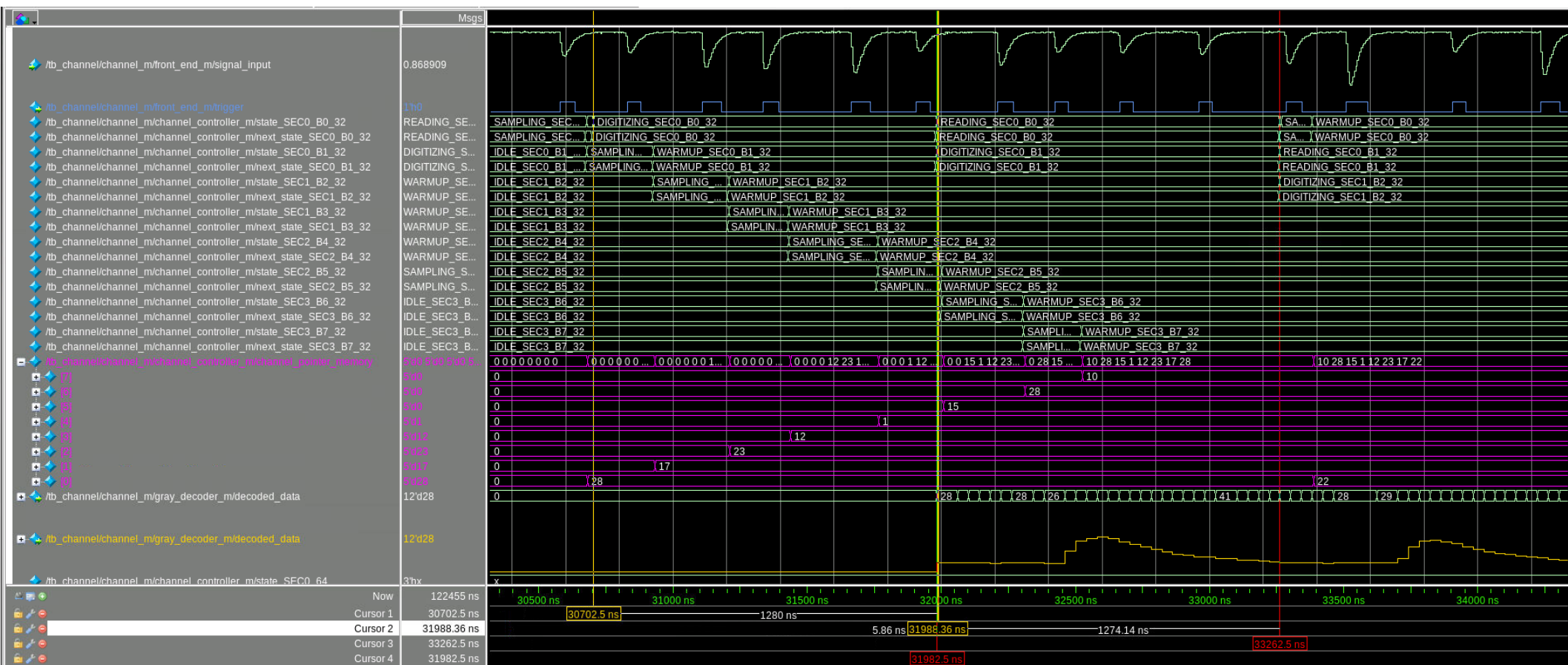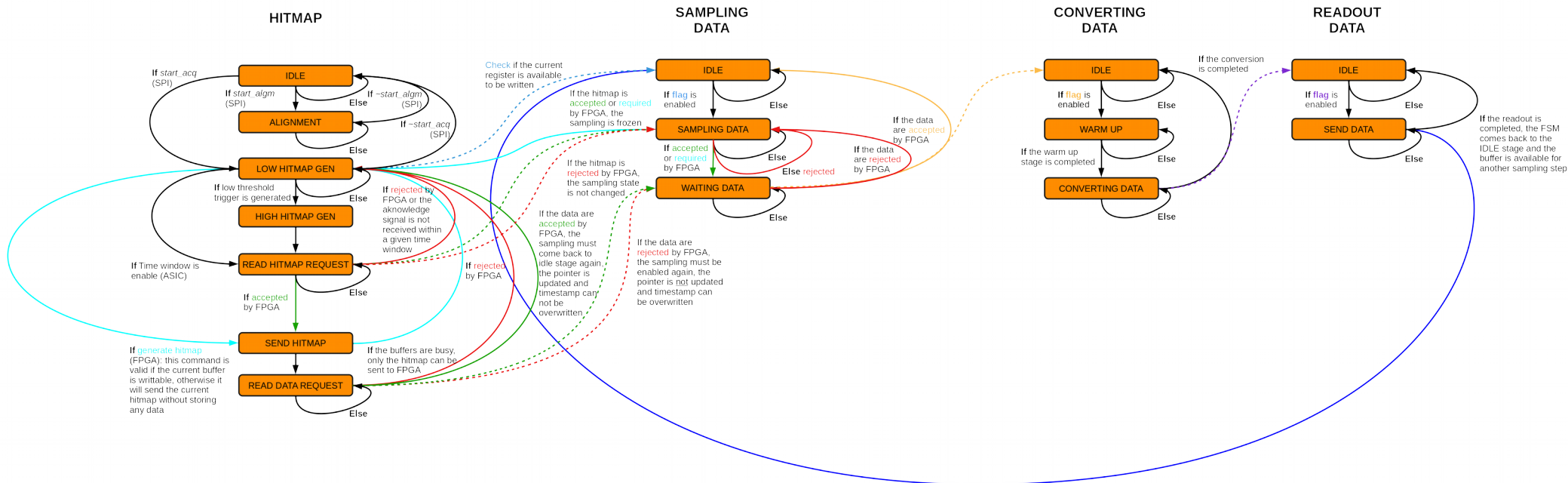
Three modes:

- **TIME WINDOW**
- **THRESHOLD DRIVEN**
- **FPGA REQUEST**
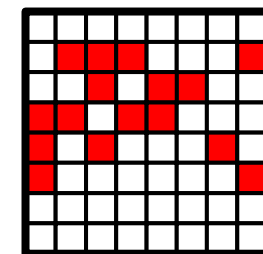
High threshold

Low threshold

On the edge

Light pollution

HITMAP
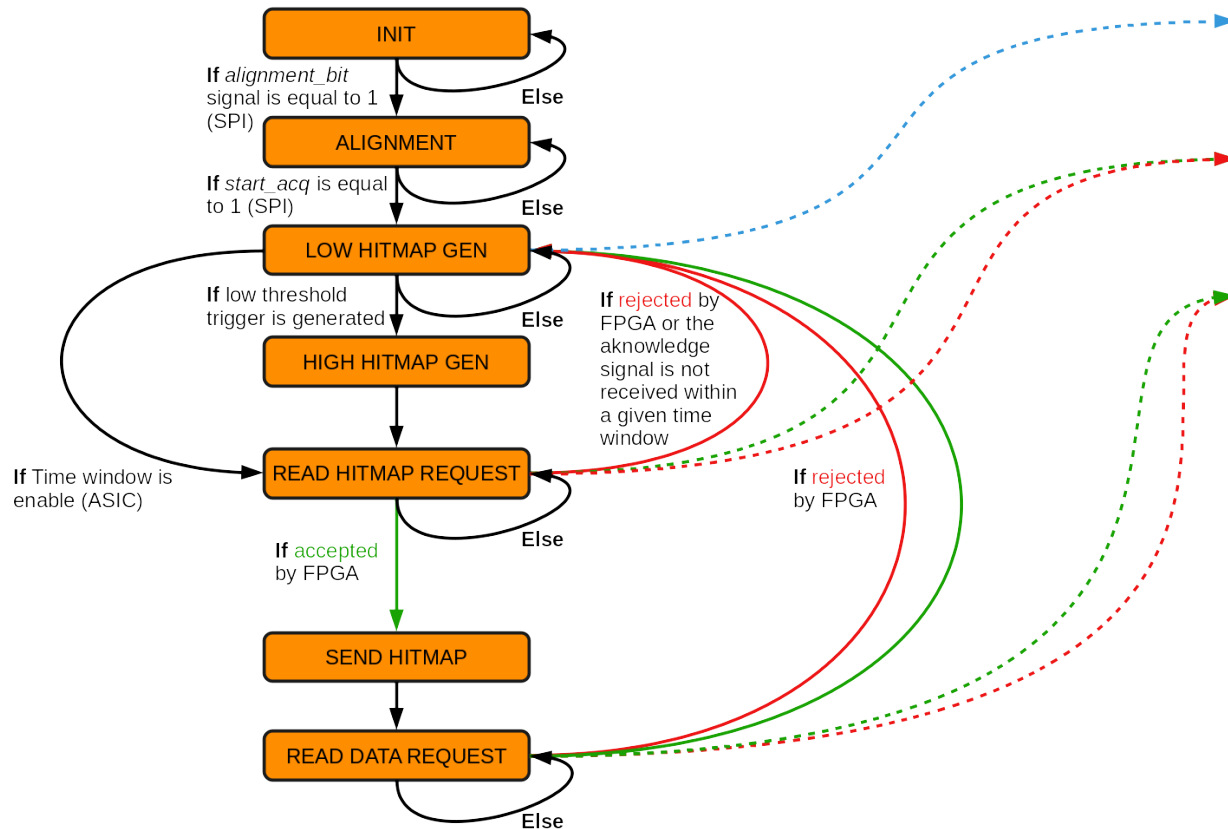
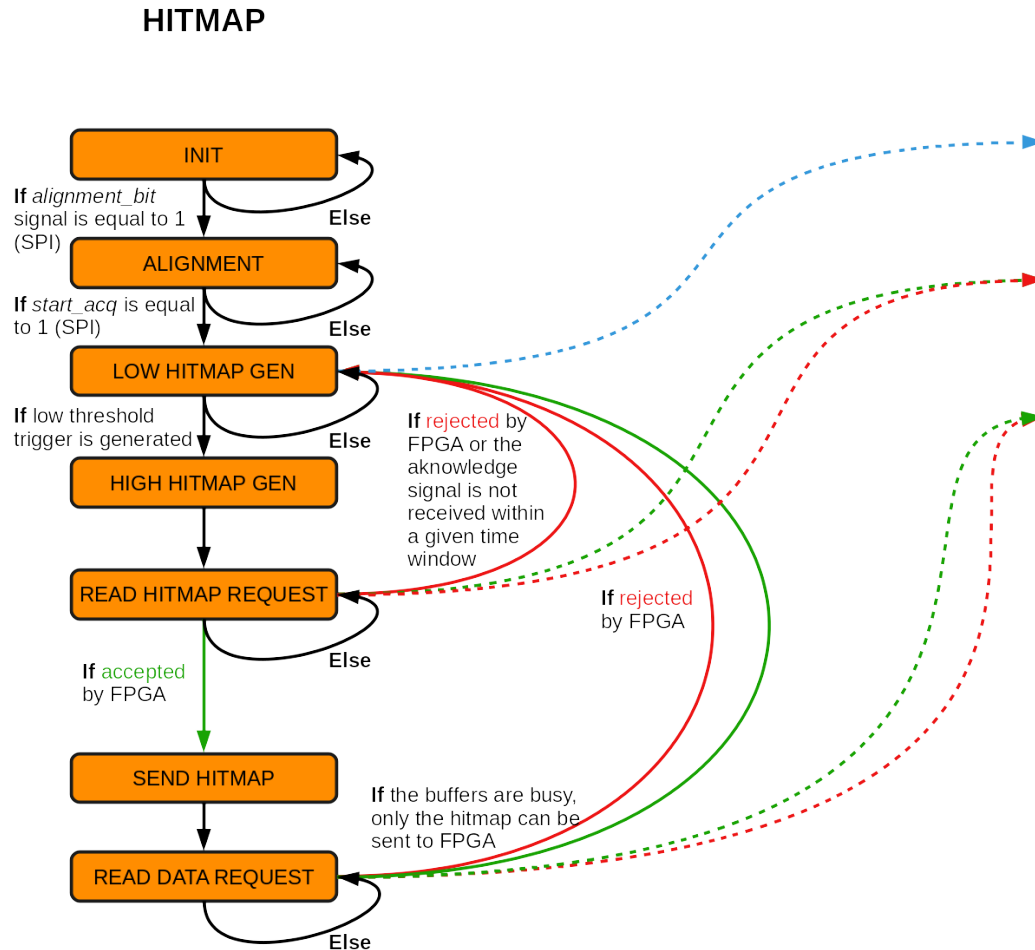- **TIME WINDOW**: 6 bits-programmable time window (64 x 5 ns = 320 ns) to generate a hitmap. The ASIC sends a read request to the FPGA. Only the low threshold hitmap is sent. Then, the FPGA can accept or reject the hitmap, thus the ASIC can digitize and send out the data or comes back to the sampling stage.

13
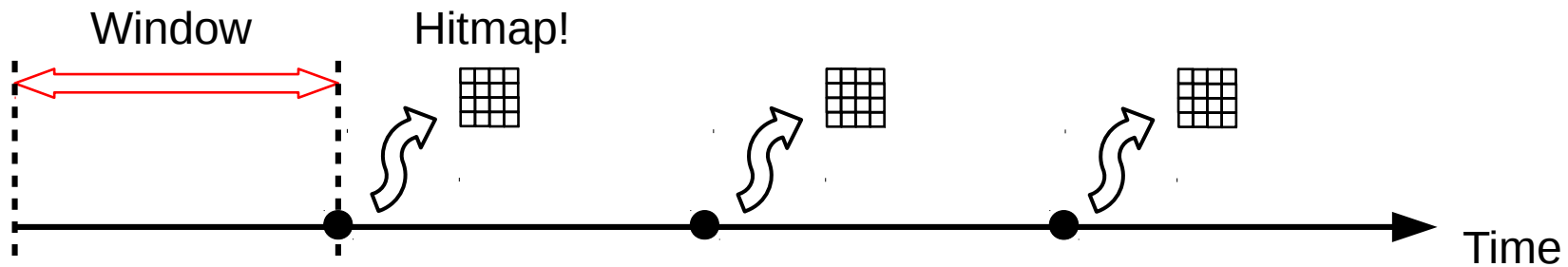
Hitmap logic

HITMAP

- **THRESHOLD DRIVEN**: if one of the 64 channels is above the low threshold, then the ASIC waits a programmable time window to monitoring the high threshold as well. A read request is sent to the FPGA, sending the high hitmap or the low one. Then, the FPGA can accept or reject the hitmap, thus the ASIC can digitize and send out the data or comes back to the sampling stage.

Hitmap logic
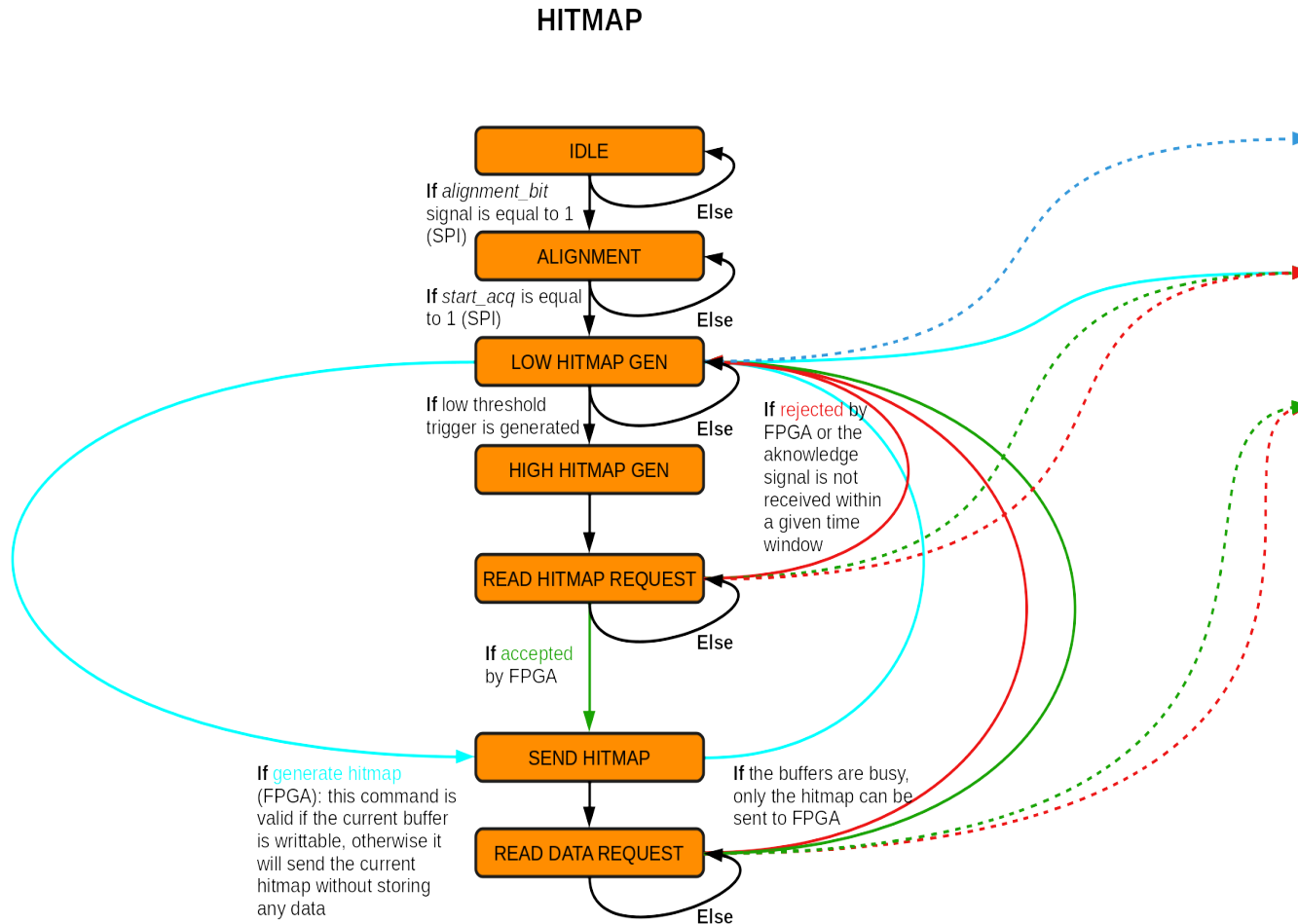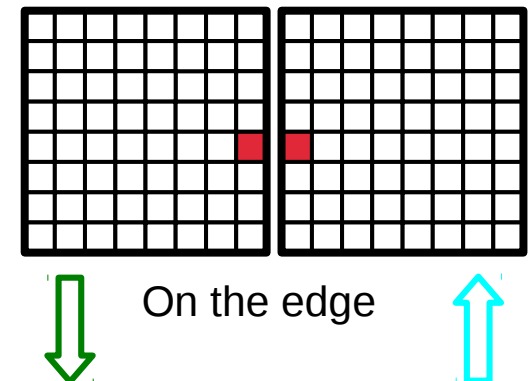
HITMAP

- **FPGA REQUEST**: the FPGA requires the low threshold hitmap generation anytime. Then, the FPGA can further require the digitization and the readout of the stored data or drive the ASIC back to the sampling stage.

On the edge

1
5

Serial bus

ASIC

RESET

CLK_200

CMD_FPGA [1:0]

SPI_EN

SPI_MOSI

SPI_CLK

TP

input

READ_RQ

HITMAP

DATA

SPI_MISO
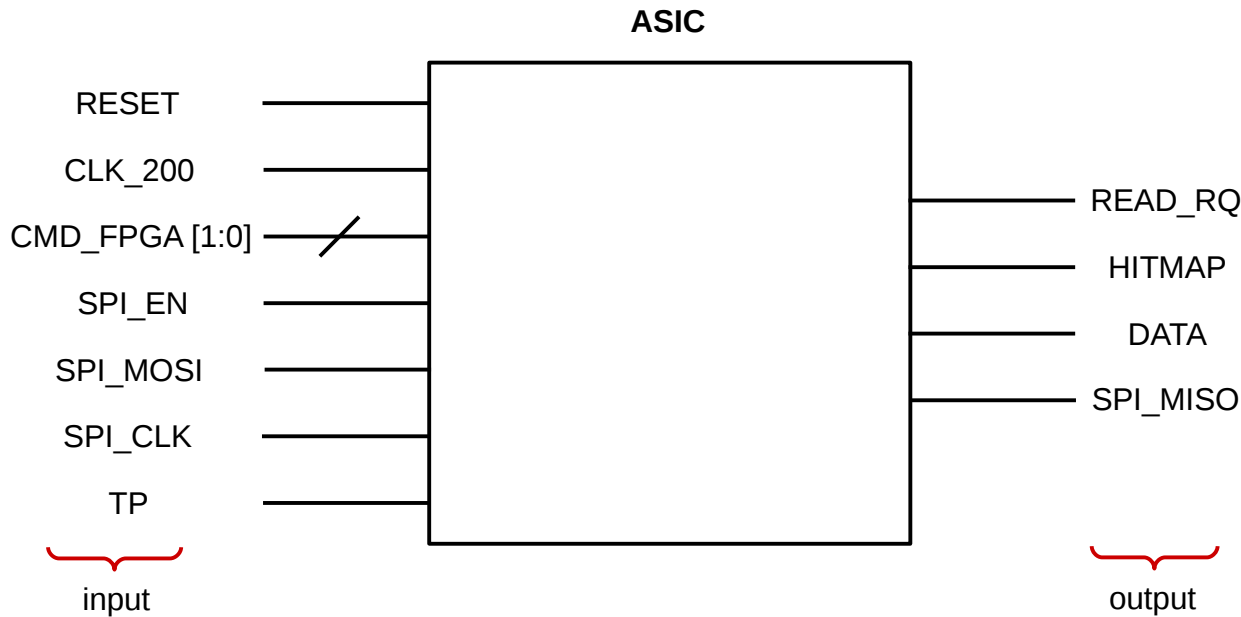
output

- **12** differential LVDS lines.
- Communication with a clock at **400 MHz** in DDR.
- To configure the ASIC: 1 dedicated **SPI**.
- 240 communication lines for the ASIC board + 640 connections with SiPMs.

From SiPMs

64 channels for ASIC

ASICs

120 digital lines to FPGA

Bus to FPGA
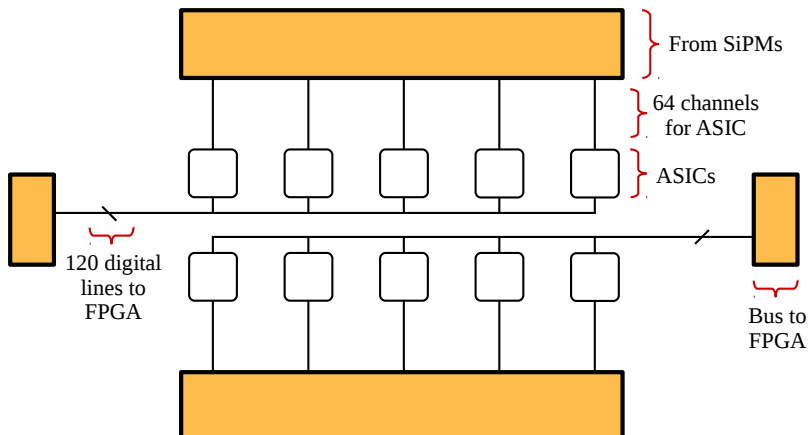
Serial bus
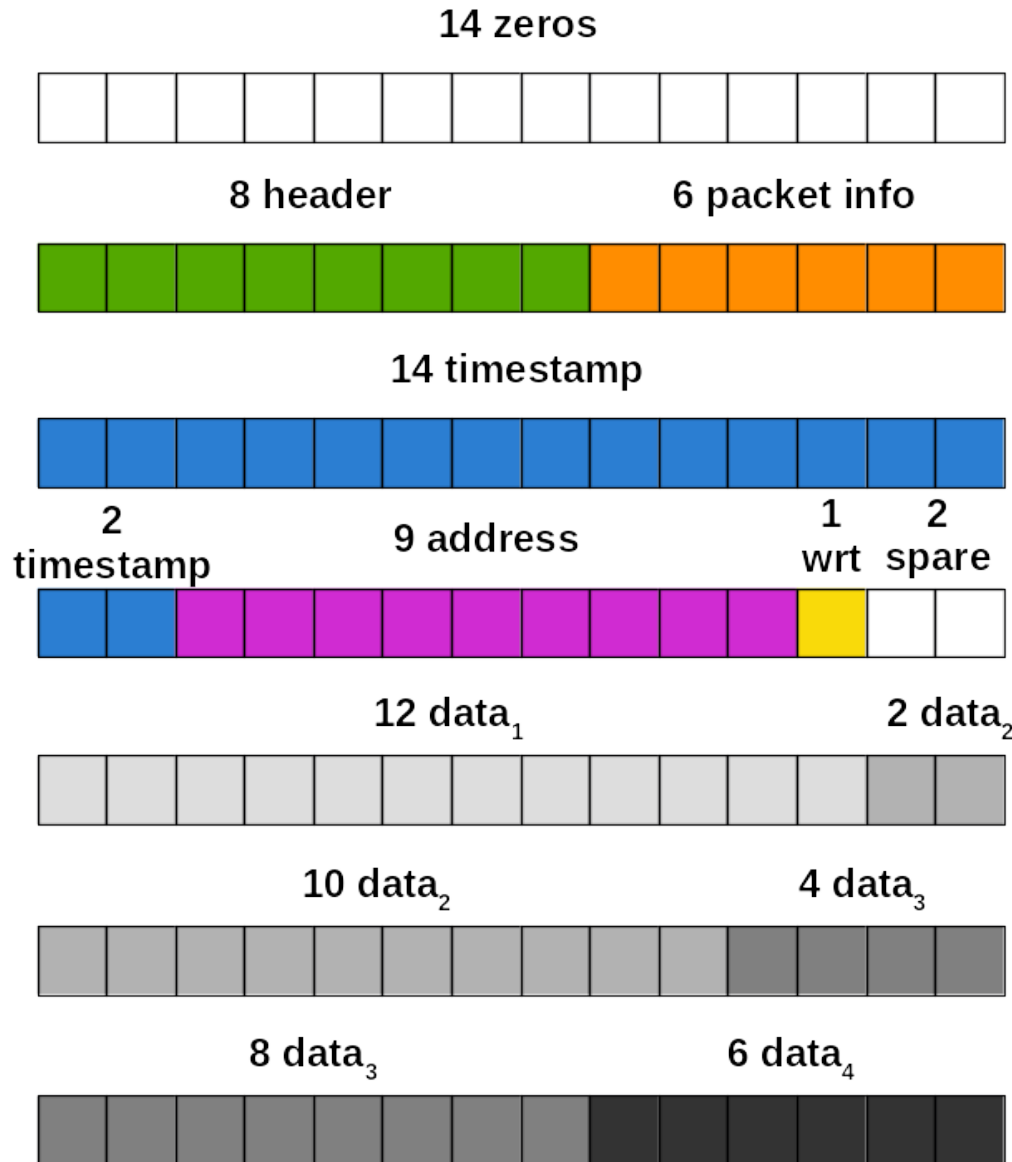
- Word size = 14 bits
- The output data stream is variable depending on the configuration:
  - Section: 32, 64, 256 cells
  - Resolution: 8-12 bits

Example
- Configuration: 32 cells, 12 bits.
- Each channel will send 434 bits
- Each ASIC will send 27776 bits (~**34.7 µs**).

Place & Route

Section: 32 cells

Capacitor

Cell layout

Analog slice

Digital slice

Cell schematic

Cell area: 20 x 44 µm^2

Power

Block	Power (μW)	Area (μm^2)	N	Power$_T$ (μW)	Area$_T$ (μm^2)
Cell	2.5	352.44	256	640	90224.64
Section	2.5	96.48	8	20.0	771.84
Section controller	31.36	839.88	4	125.44	3359.52
Gray counter	42.4	376.20	1	42.4	376.20
Gray decoder	2.86	357.48	1	2.86	357.48
Channel controller	430	8083	1	430	8083
Total				1260.7	103172.68

- Worst case, low power library.
- Estimation before P&R, based on the area of standard cells (no routing).
- Imaging mode.
- Segmentation 32.
- clock gating enabled.
- Range: 2135 ns (from sampling to readout stage) at f_s = 200 MHz.

Summary

- Detection of Extensive Airshowers.
- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- High level of configurability:
  - Segmentation:
    - 32 cells
    - 64 cells
    - 256 cells
  - Resolution:
    - 8 - 12 bits
  - Trigger:
    - Internally generated
    - Externally provided
  - Mode:
    - Sparse
    - Imaging
- **Production run** before the end of 2023.

Backup

ASIC architecture
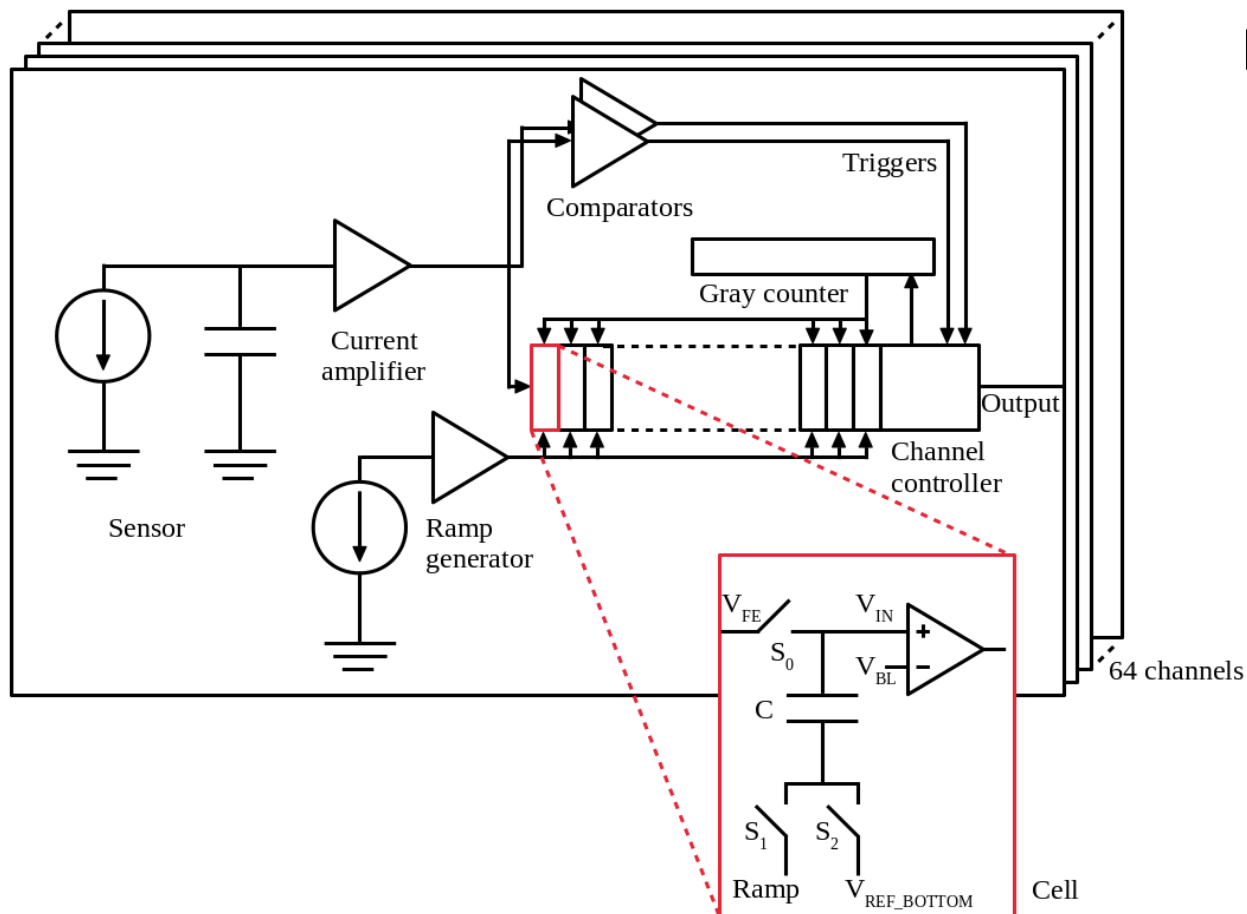
Design status:
- Mode:
  - Sparse
  - Imaging
- Segmentation:
  - 32 cells
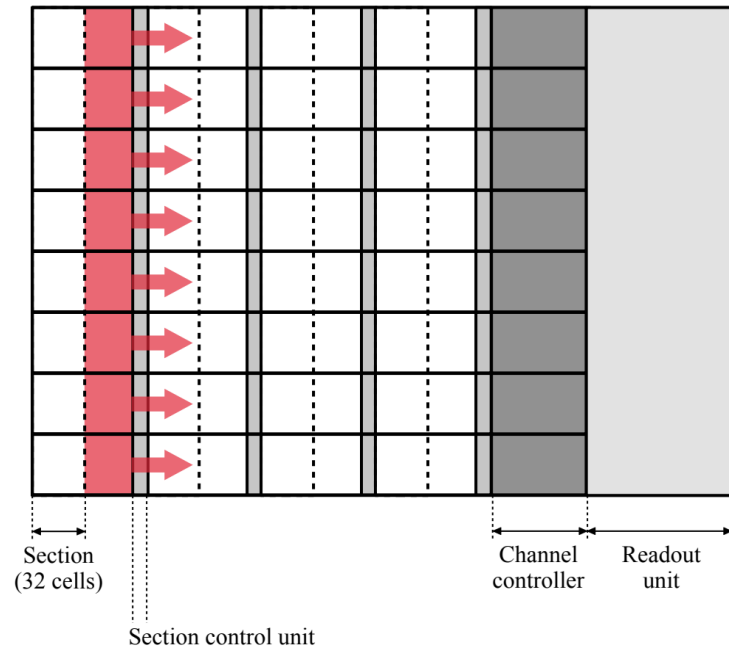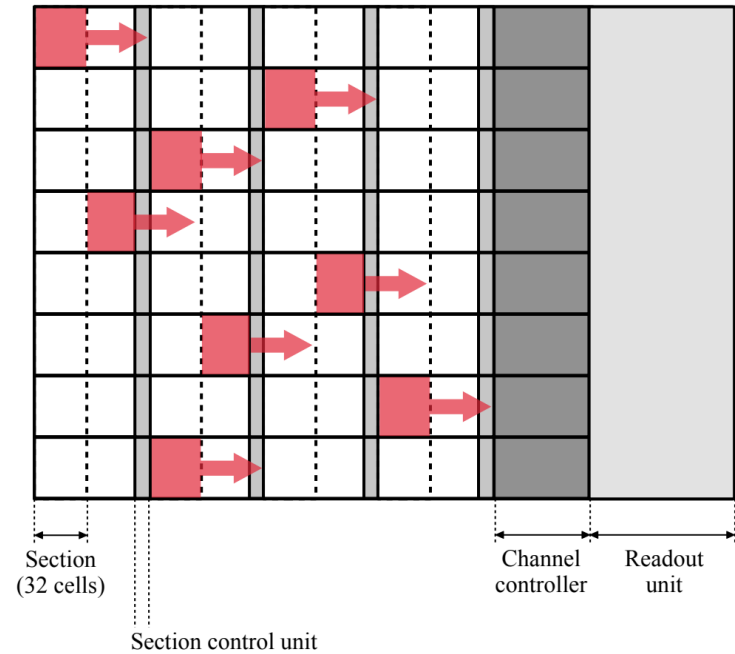 - 64 cells
  - 256 cells
- Resolution:
  - 8 - 12 bits
- Trigger:
  - Internally generated
  - Externally provided
- 8-channels readout

Mode

Imaging mode

Sparse mode

Derandomization

The input signal follows the Poisson distribution. The probability of receive n events is:

$$P_n = \mu^n \frac{e^{-\mu}}{n!}$$

Supposing to have an event rate of **100 kHz**, and a dead-time of **8 µs**, the probability of loosing an event is:

$$P_{loss} = 1 - e^{-0.8} \simeq 0.55$$

By using **n segments** this probability is evaluated as:

$$P_{loss} = 1 - \sum_0^n \mu^n \frac{e^{-\mu}}{n!}$$

With 4 segments P_{loss} would be equal to about 0.5%

Front-end

SiPM Preamp Buffer Pole-zero cancellation

VBIAS

IB3

IB2

VCAS

Vout

Iin

IB1

RL

- Current amplifier.
- g_m boosting.
- Configurable stage: two polarities.

R_Z

C_C

C_Z
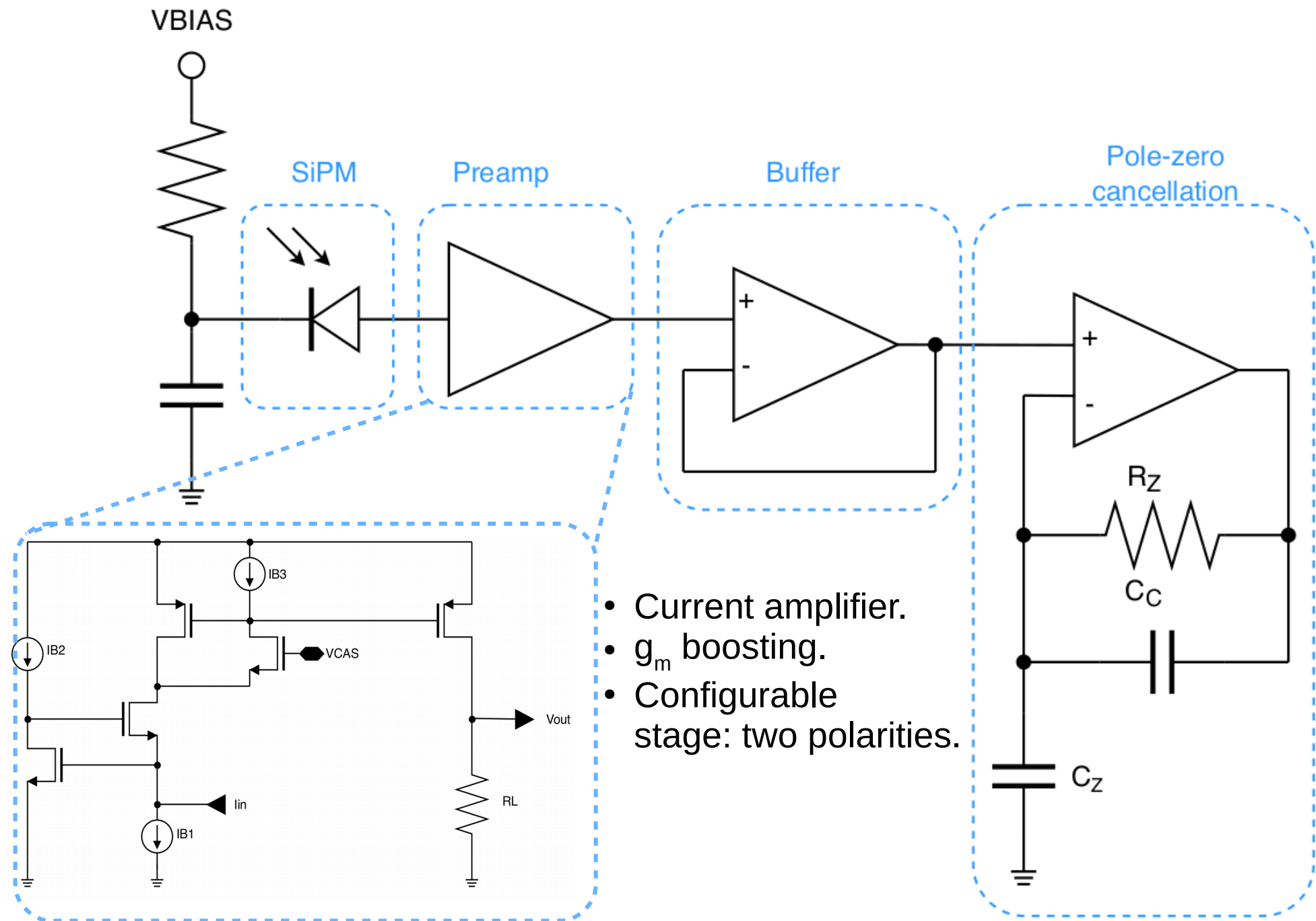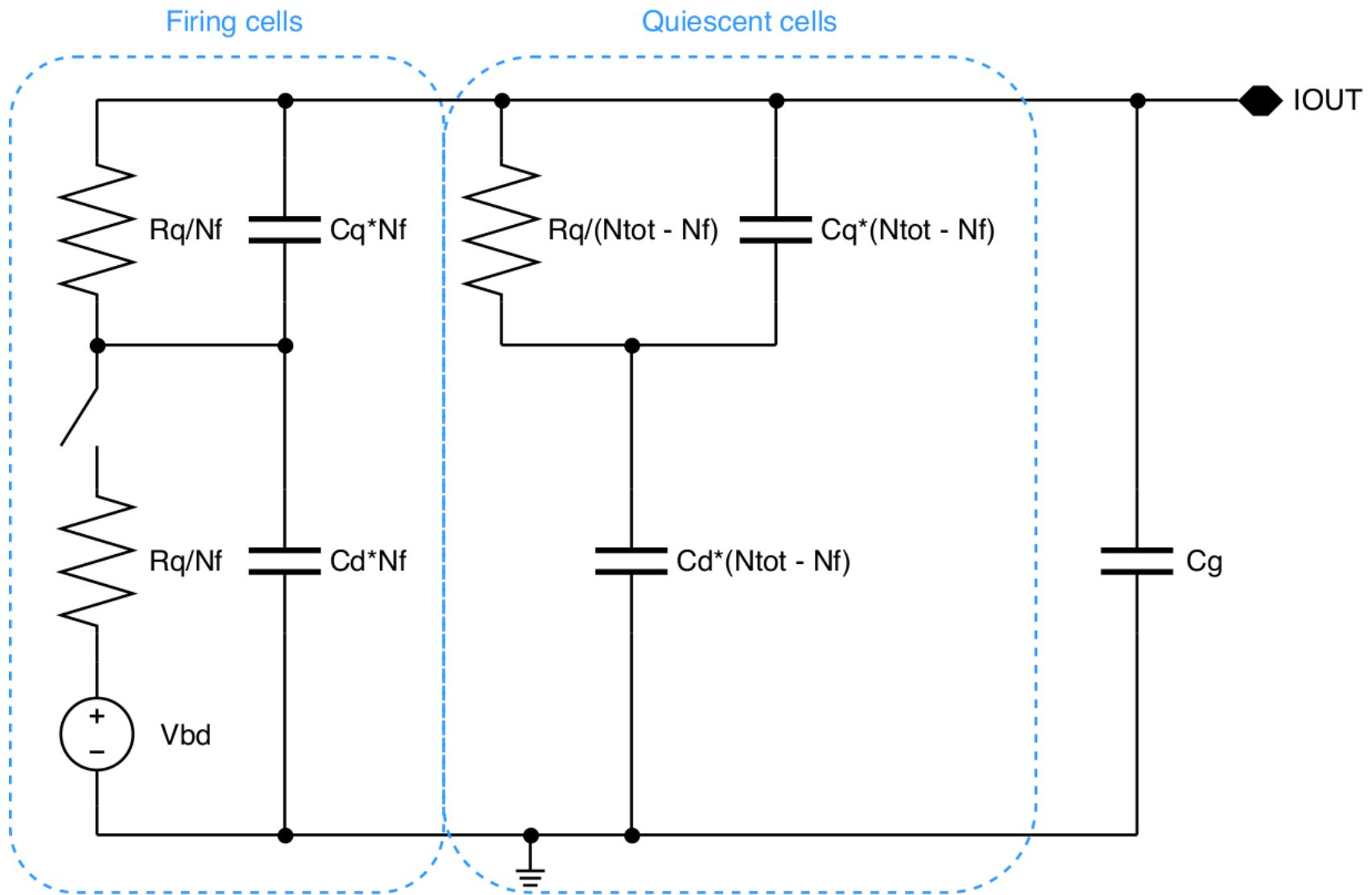
SiPMs

SiPMs: FBK, pitch of 25 μm, 3 x 3 mm, 2 arrays of 8 x 8 pixels.

SiPMs

- Background:
  - Radiation damage.
  - Background photons due to scintillation processes or fluorescent materials.
  - A signal can be directly induced in SiPM by high charge ions.
- By considering a **threshold** at 7 photon-electrons, the estimated **background rate** is ~1 kHz and it will rise up to 200 kHz.
- The estimated **event rate** is ~100 events per year.
- The estimated **total dose** is ~1 krad/year.
- The expected **Dark Count Rate** (DRC) is ~ 22 Mhz at the end of the mission (3 years).

Power

Block	Power (μW)	Area (μm^2)	N	Power$_T$ (μW)	Area$_T$ (μm^2)
Cell	2.5	352.44	256	640	90224.64
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Total				1260.7	103172.68

- Digital block designed for the readout of a group composed by 8 channels (this circuit is not included in the table):
  - Digital readout controller: area 2896 µm², power 0.3495 mW
  - Serializer: area 896 µm², power 0.1464 mW.
  - Divided by 8: + ~0.06 mW per channel.