

A mixed-signal read out ASIC for silicon micro-strip detectors

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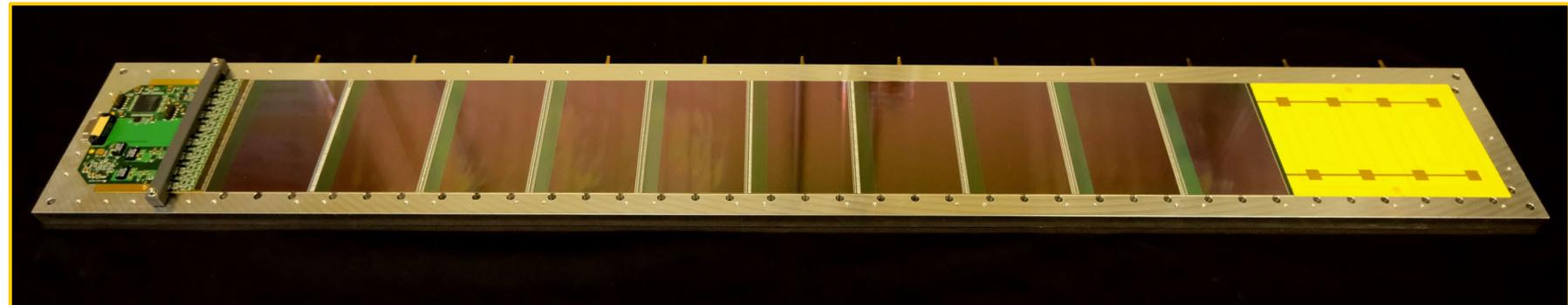
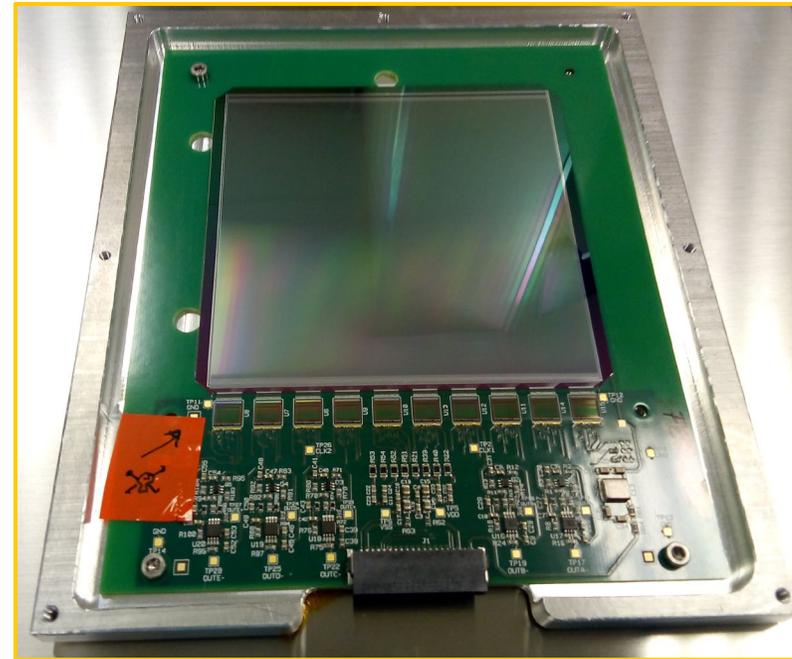
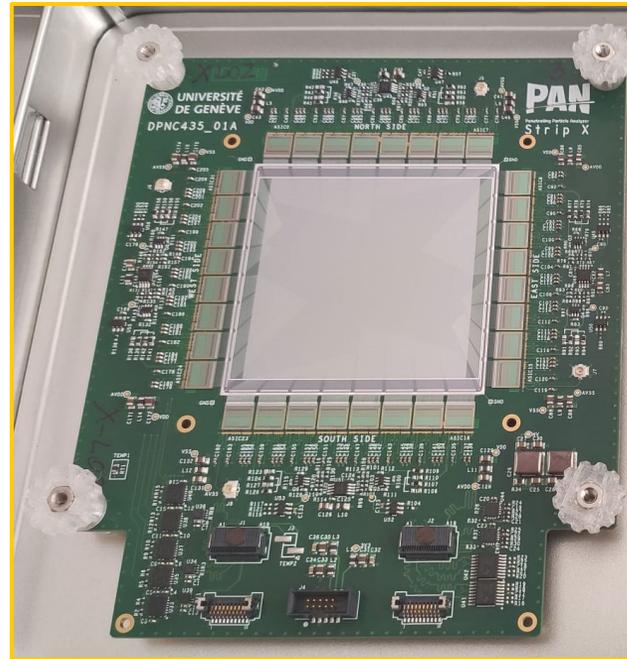
- We extensively use μ Strip detectors
 - Charge measurements
 - Position measurements

- Mainly because they
 - Cover large areas with relatively low power consumption
 - *e.g.* AMS: 5 m², 155 W
 - Add few material in the particles path
 - *e.g.* FOOT: 150 μ m per layer

- PLUS: Already tested and used in space and radioactive environments

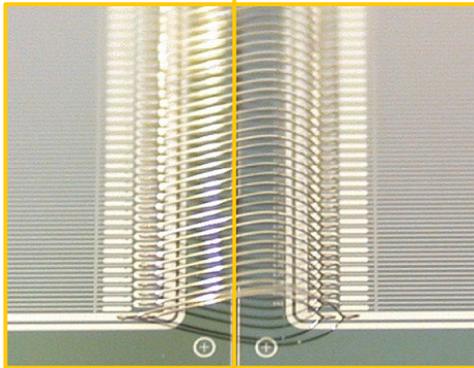
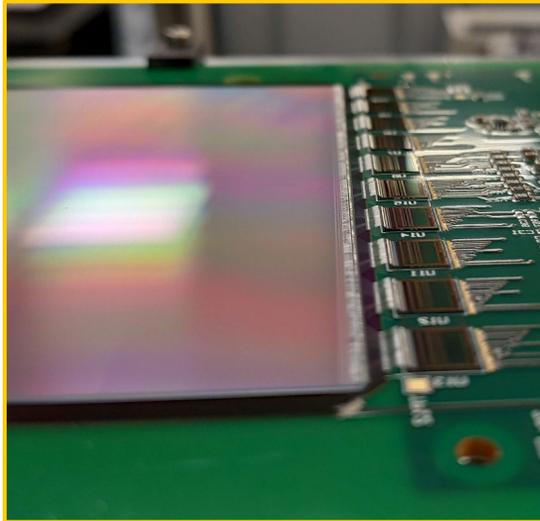
Silicon μ Strip Detectors @ PG

AMS-L0
PAN
HERD
FOOT

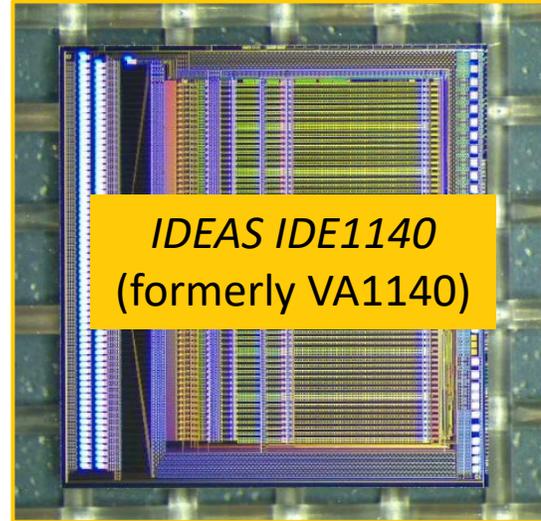


Three main components

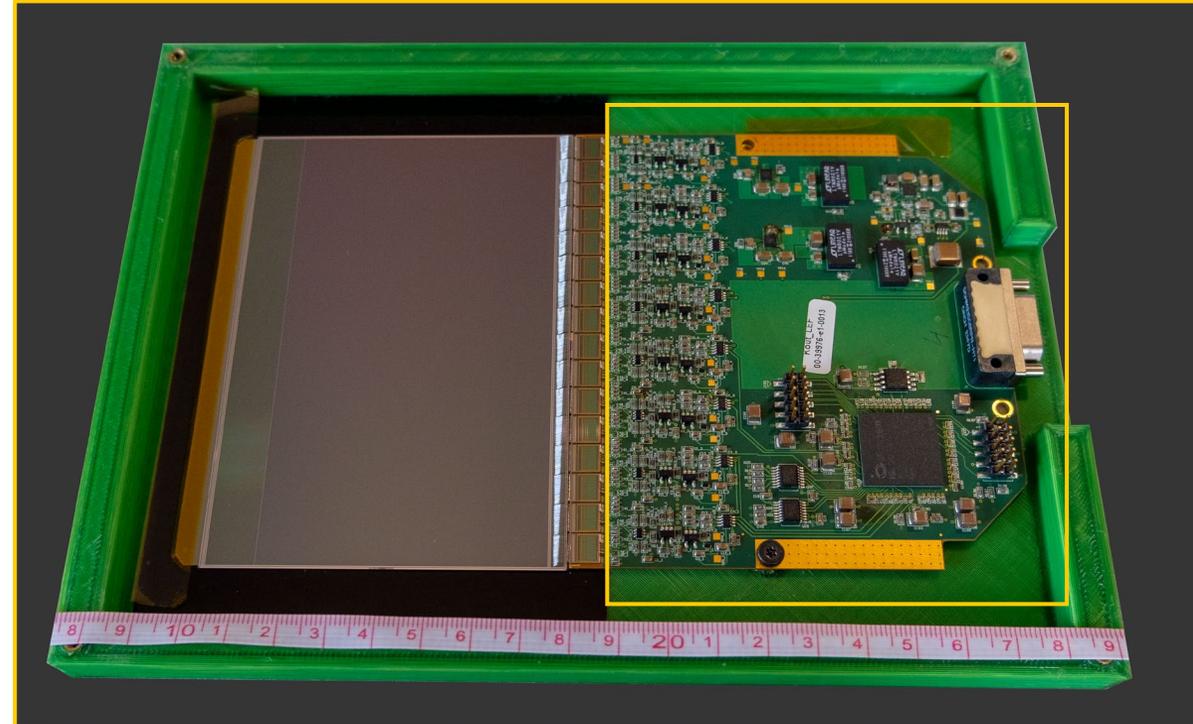
Silicon sensors



Readout ASICs



ADCs and DAQ system



A detailed, high-resolution image of a microchip die, showing a complex grid of circuitry in various colors (purple, blue, green, yellow) against a dark background. The die is rectangular with a dense pattern of connections and internal structures.

ASTRA: Adaptable Space sTrip Readout ASIC

Designed by INFN Torino

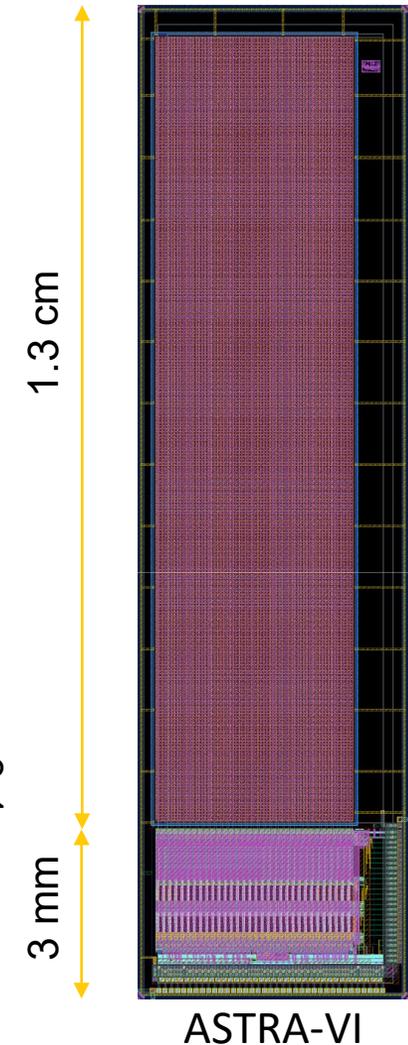
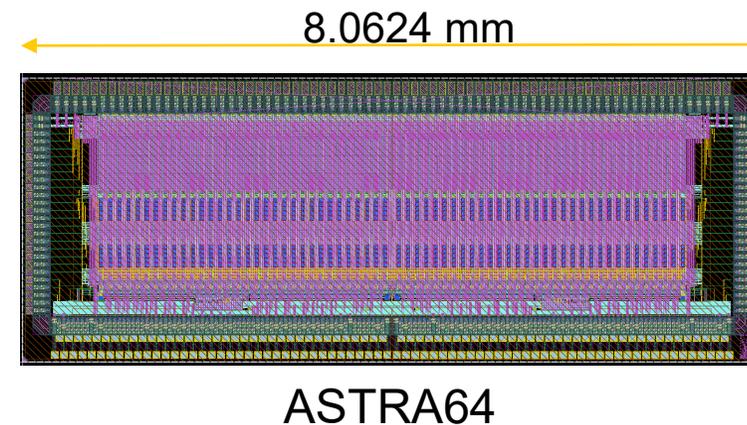
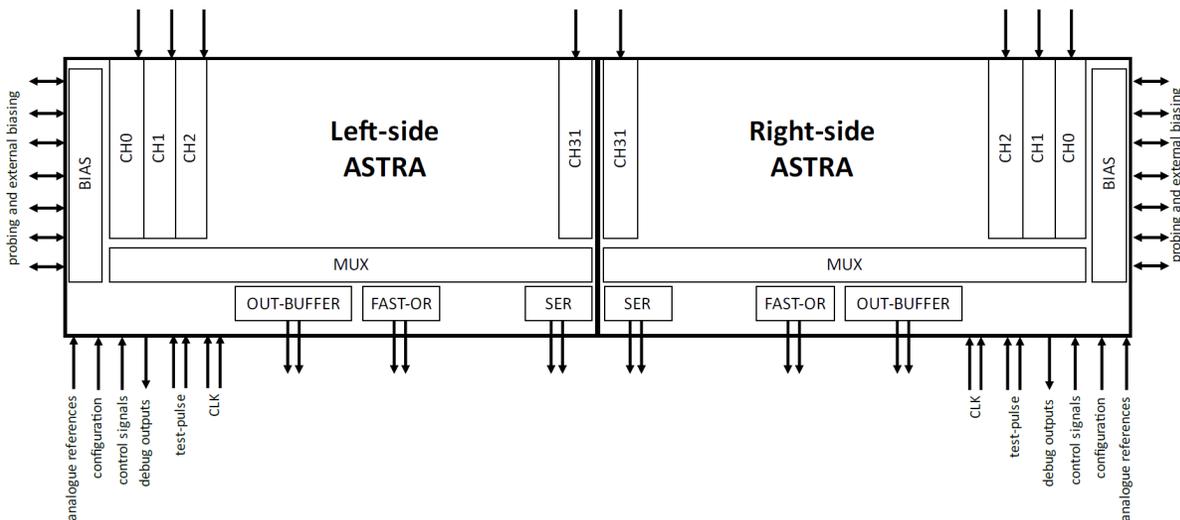
- Electronics for the read-out 110- μm -pitch silicon μStrip Detectors
- Electronics+Sensor Monolithic ASIC

	ASTRA Requirements
Channels	64
Dynamic Range	± 160 fC
Linearity Region	± 160 fC
Shaping Time	Adjustable in $1 \div 10$ μ s
ENC	< 1000 e ⁻ @ C_{in} 100 pF
Output	Multiplexed pulse height Digitized pulse height Channels FastOR
Power supply	Positive (only) supply
Channel power consumption	< 1 mW per channel
Production Process	110 nm CMOS
Size	6x6 mm ²

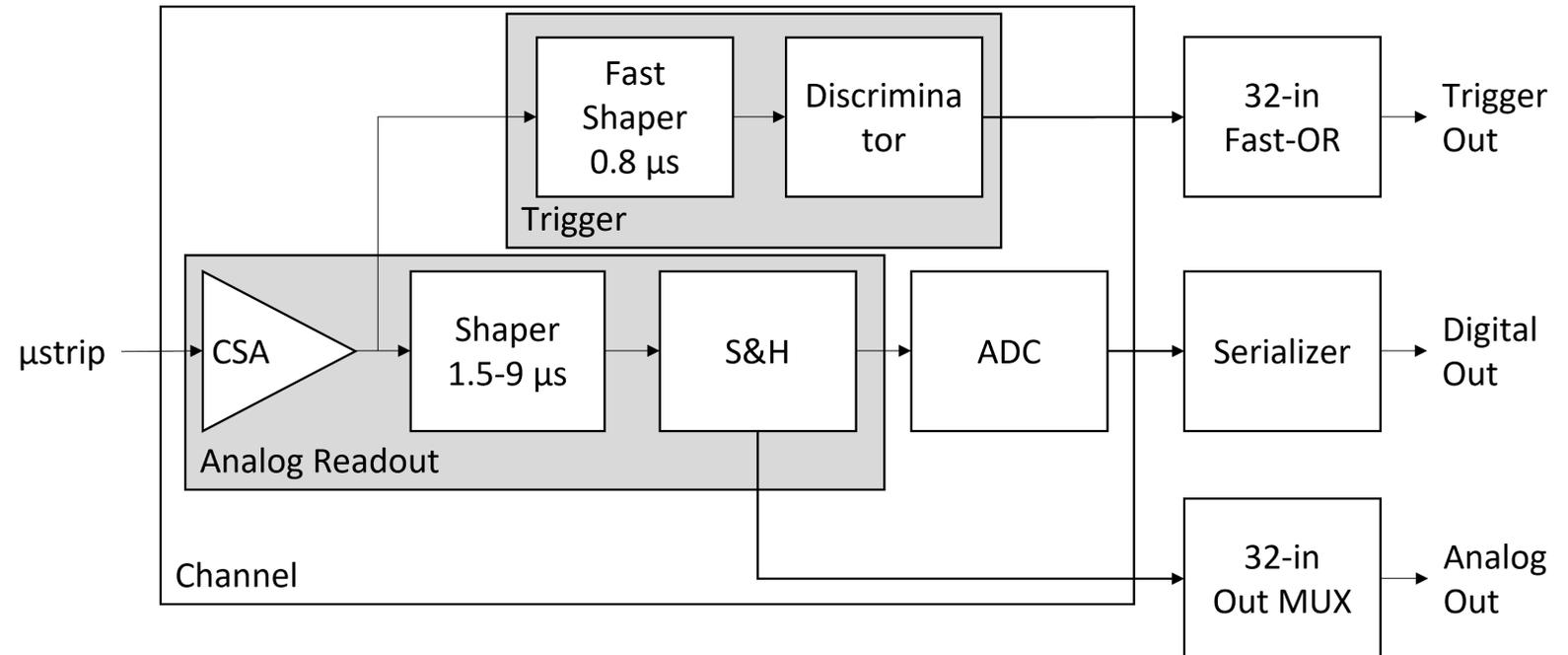
- Requirements tailored to HERD Silicon Charge Detector (SCD)
- Produced at LFoundry
 - Only HVT transistors (1.2 V) available

ASTRA: Adaptable Space sTrip Readout ASIC

- First prototype in the framework of the INFN project **ARCADIA**
 - 64 channel read-out: ASTRA64
 - 32-strips fully-depleted monolithic active CMOS microstrip sensor: ASTRA-VI
- The two versions share the same electronics
 - configurable Gain
 - configurable Peaking Time
 - configurable Readout mode (analog or digital)

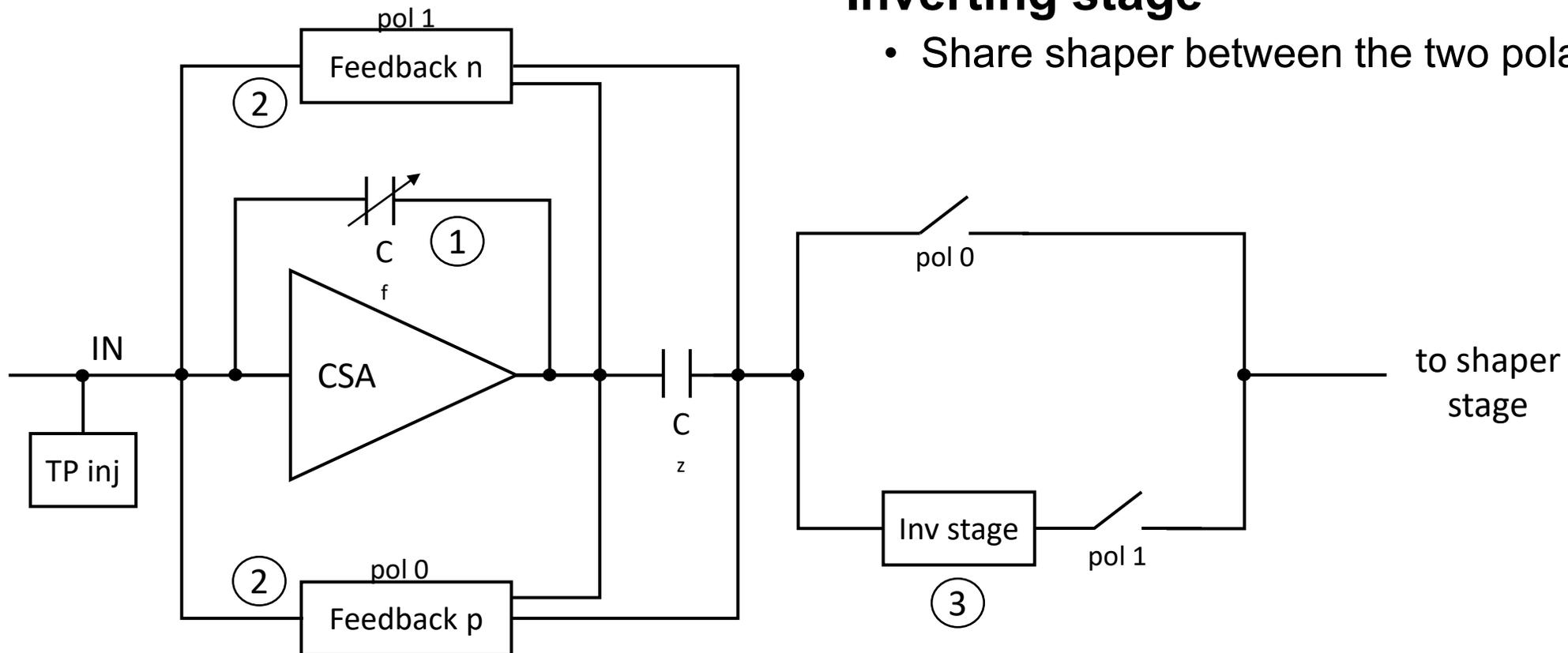


- **PreAmp**
 - Charge Sensitive Amplifier
 - Test-pulse injection circuit
- **Slow Shaper**
 - Charge measurement
 - Externally-controlled S&H circuitry
- **Analogue readout**
 - MUX-differential output buffer
- **Digital readout**
 - Wilkinson ADC and serializer
- **Fast Shaper**
 - Trigger output
 - Fast-OR output



- **CSA**

- Both input polarities
- Two programmable gain configurations
 - 4.2 mV/fC, 7.6 mV/fC

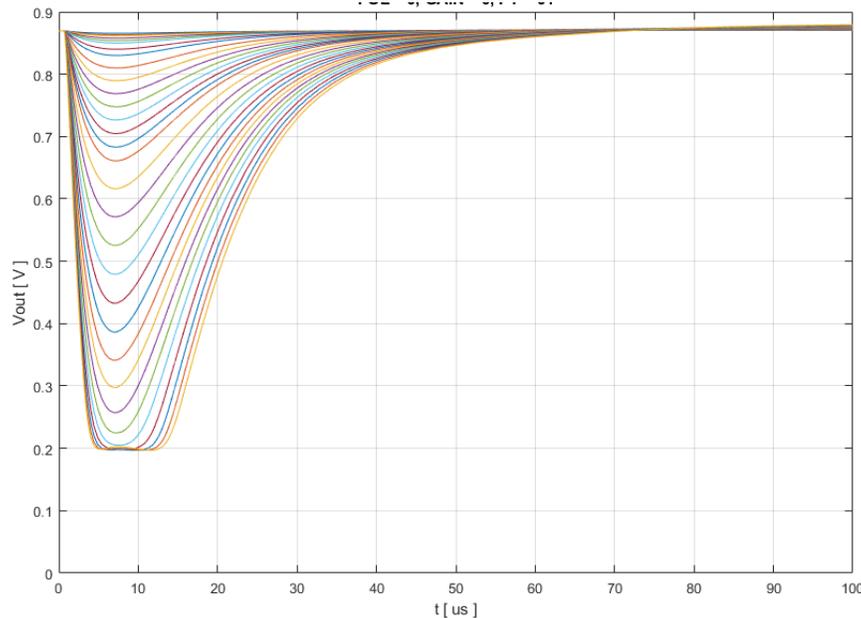
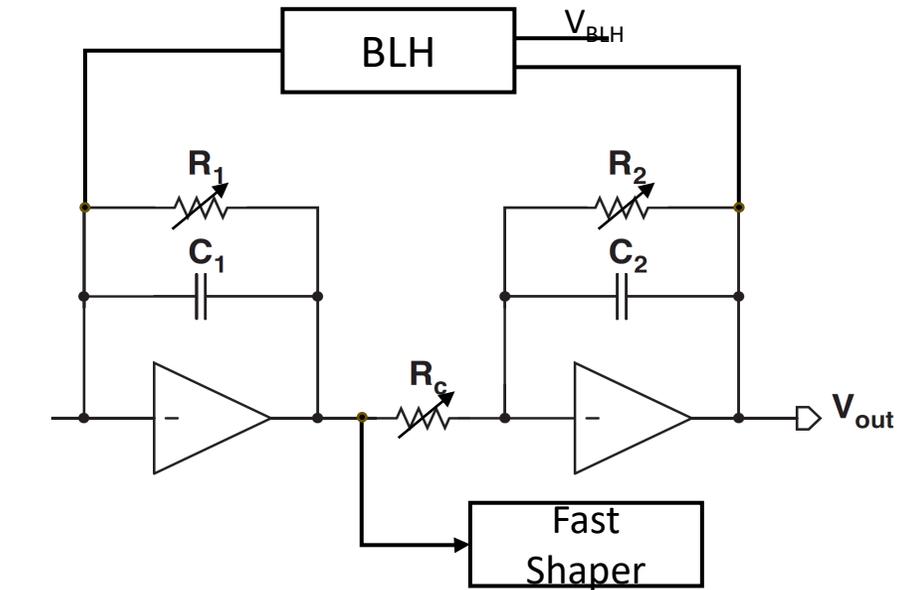


- **Gm feedback** implemented with current mirrors

- Output charge amplification with pole-zero cancelation

- **Inverting stage**

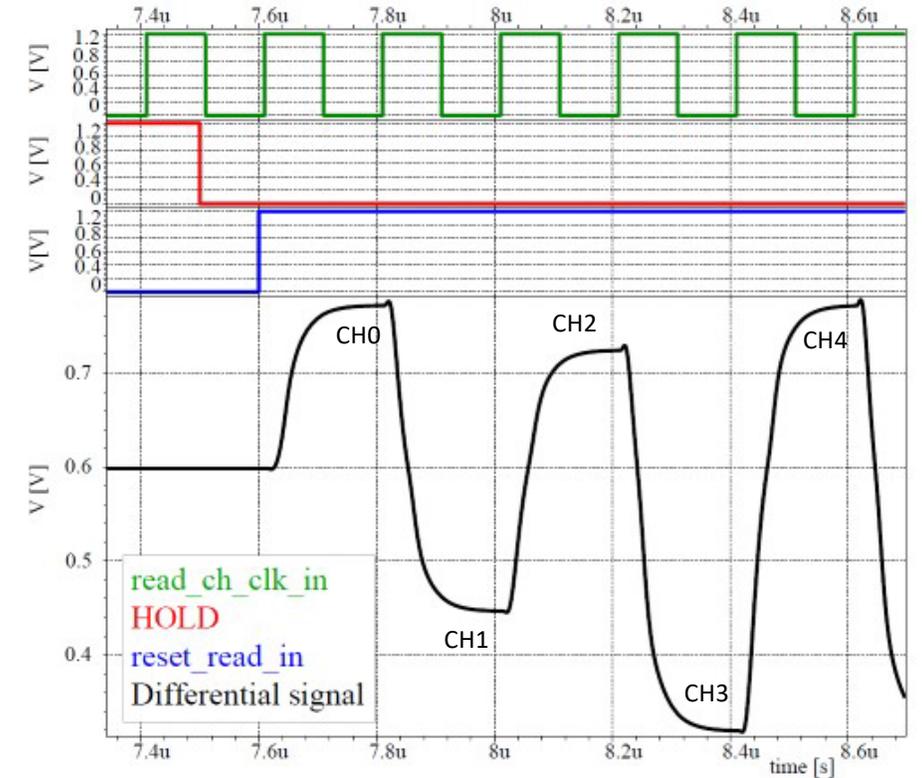
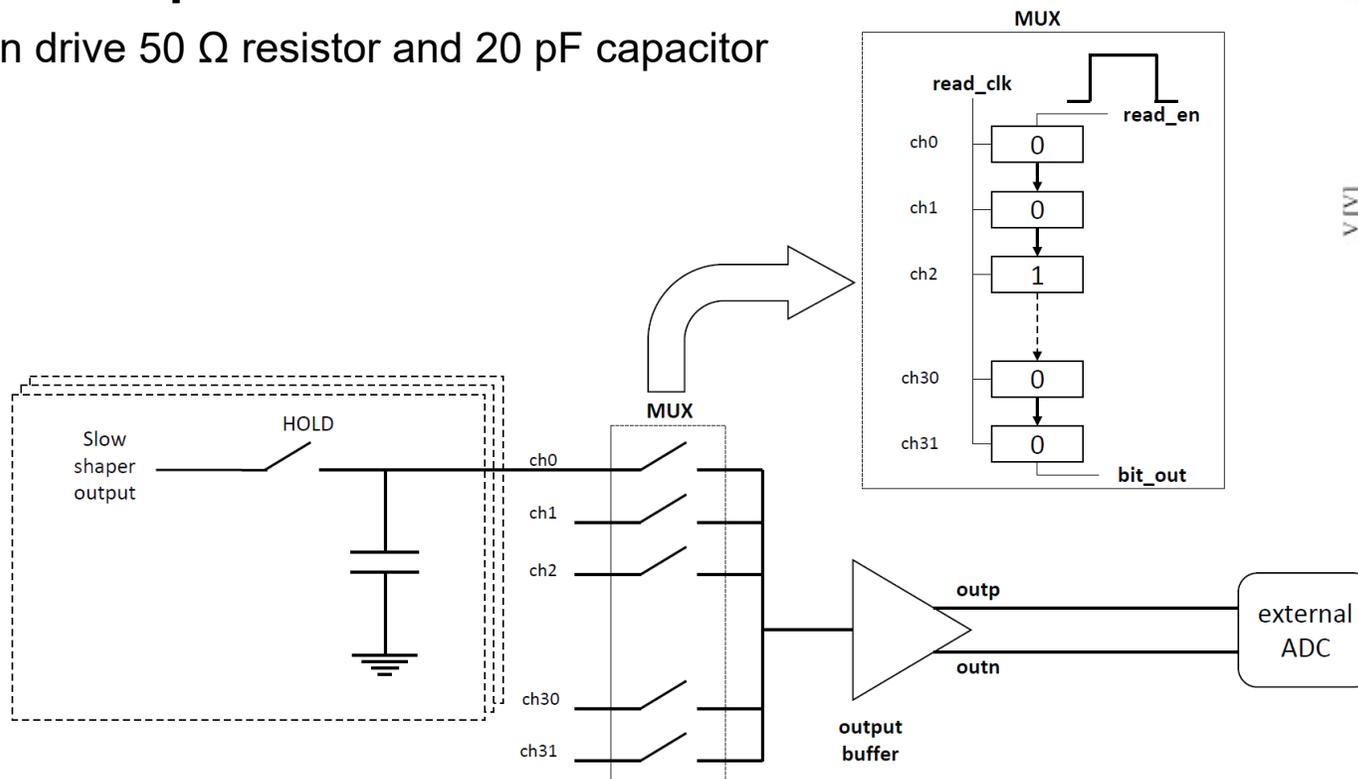
- Share shaper between the two polarities



- CR-RC Shaper
- **Four** programmable **peaking time**
 - 1.5 μs , 3.5 μs , 6.5 μs , and 9 μs
- Shaper core amplifiers share CSA architecture
 - Down-scaled bias current and transistors size
- **Baseline holder (BLH)** circuit
 - Control Shaper DC output voltage
 - Nominal $V_{\text{BLH}} = 870 \text{ mV}$

Analog Readout

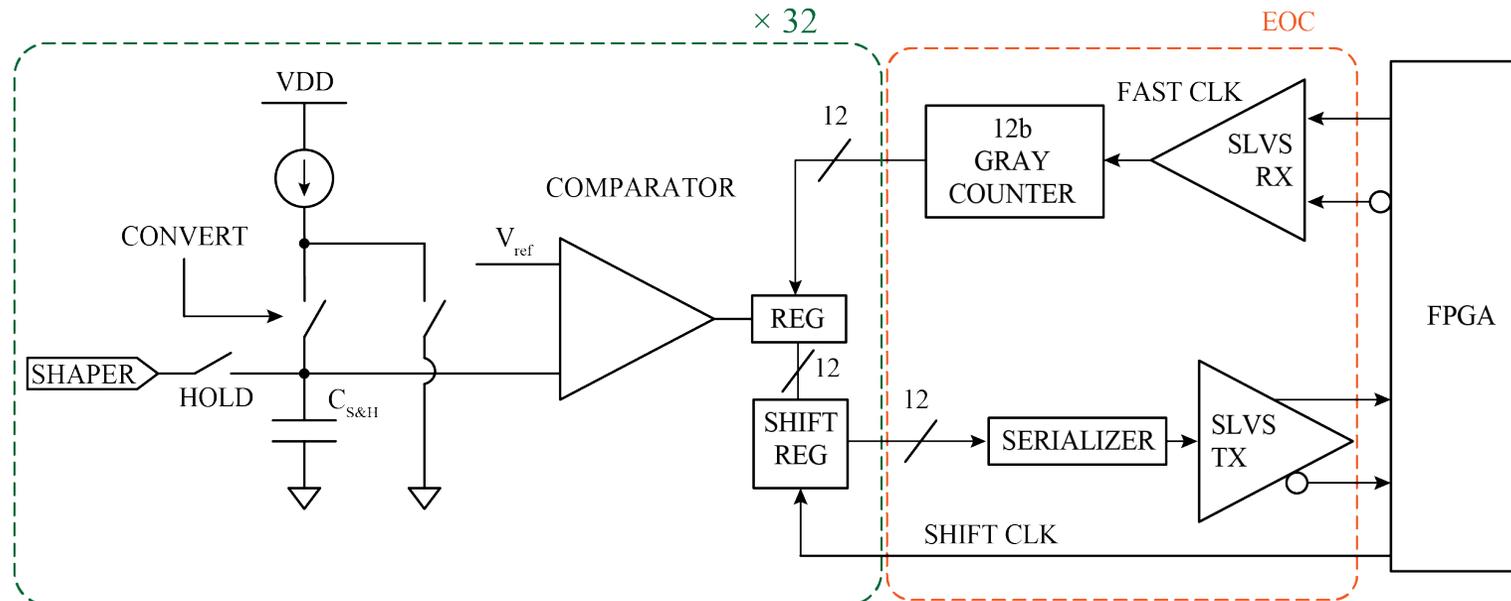
- **External HOLD** signal
 - Store shaper output peak voltage for each channel
- **MUX** to send off-chip the sampled signals
 - Max. 5 MHz read-out clock
- Unity-gain single-ended to differential cascode amplifier
- **Class-AB output buffer**
 - Can drive 50 Ω resistor and 20 pF capacitor



- S&H signal digitized by on-channel **Wilkinson ADC**
 - Programmable recharge current
 - Output: **12-bit Gray counter** of the recharge time
- Single **Serializer + SLVS TX link**
 - Data output at Double-Data-Rate
 - $t_s = 80 \text{ ns} \rightarrow t_{ro} = 2.56 \mu\text{s}$

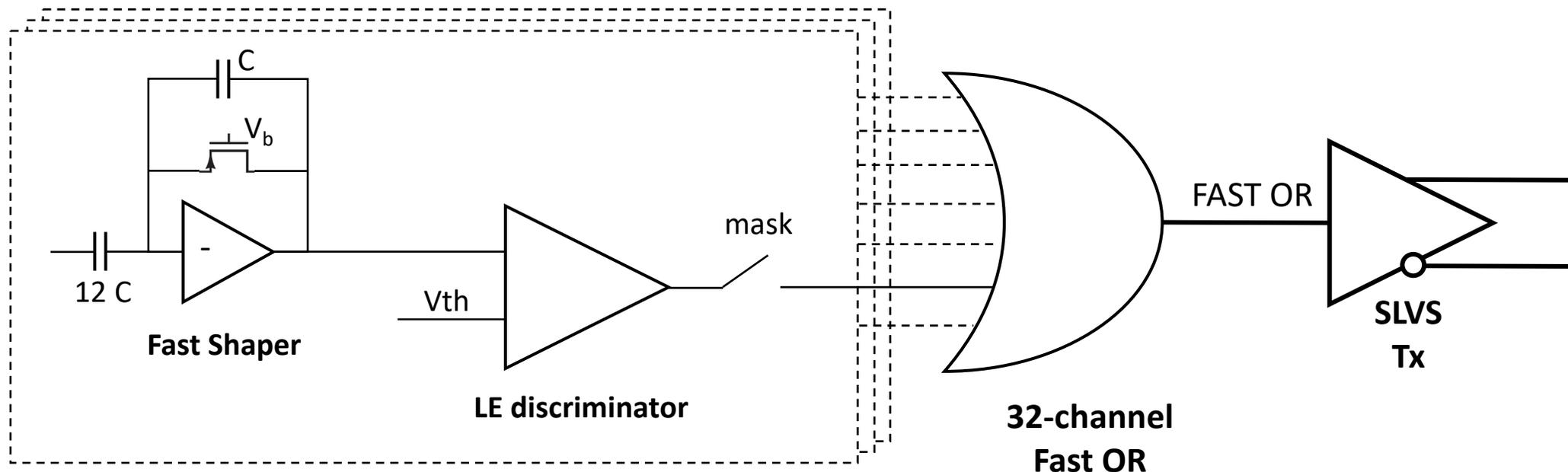
} 100 MHz clock

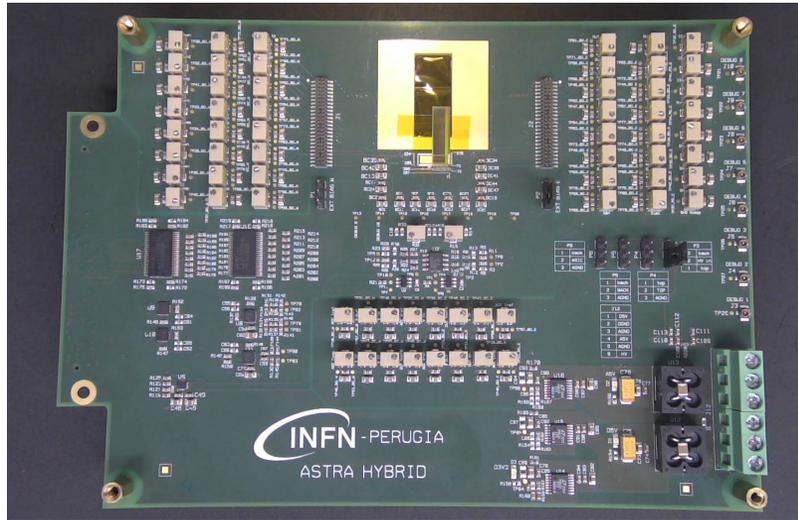
I_{ADC} [nA]	MAX recharge time [μs]	# BITS
70	2.7	8
35	5.4	9
17	11.1	10
9	20.9	11
4.5	41.9	12



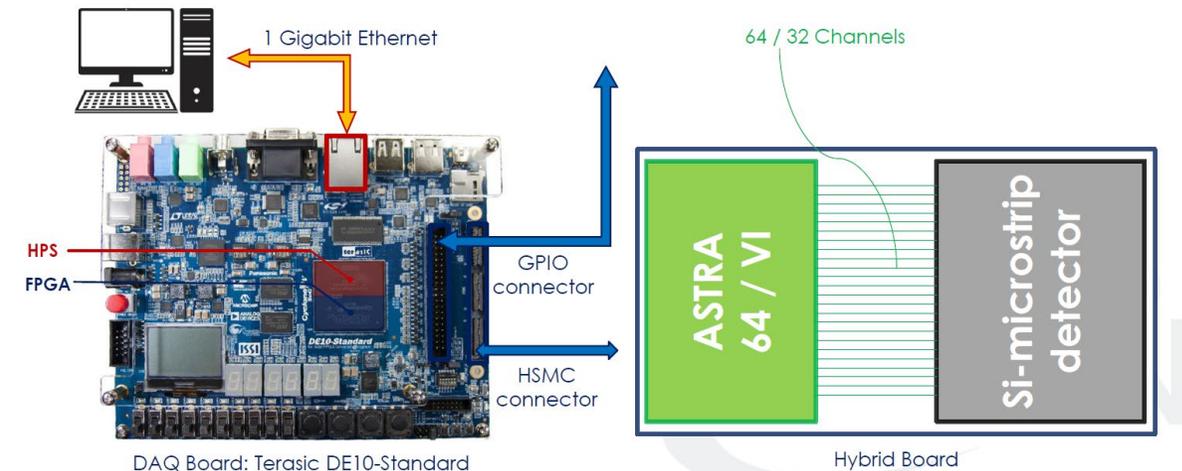
Fast Branch – Trigger Output

- **Fast shaper**
 - 800 ns peaking time, 25 mV/fC
- **LE discriminator** with hysteresis
 - V_{th} generated off-chip and common to all 32 channels
- **Fast OR** logic to generate trigger output
 - Each channel can be masked to remove noisy channels





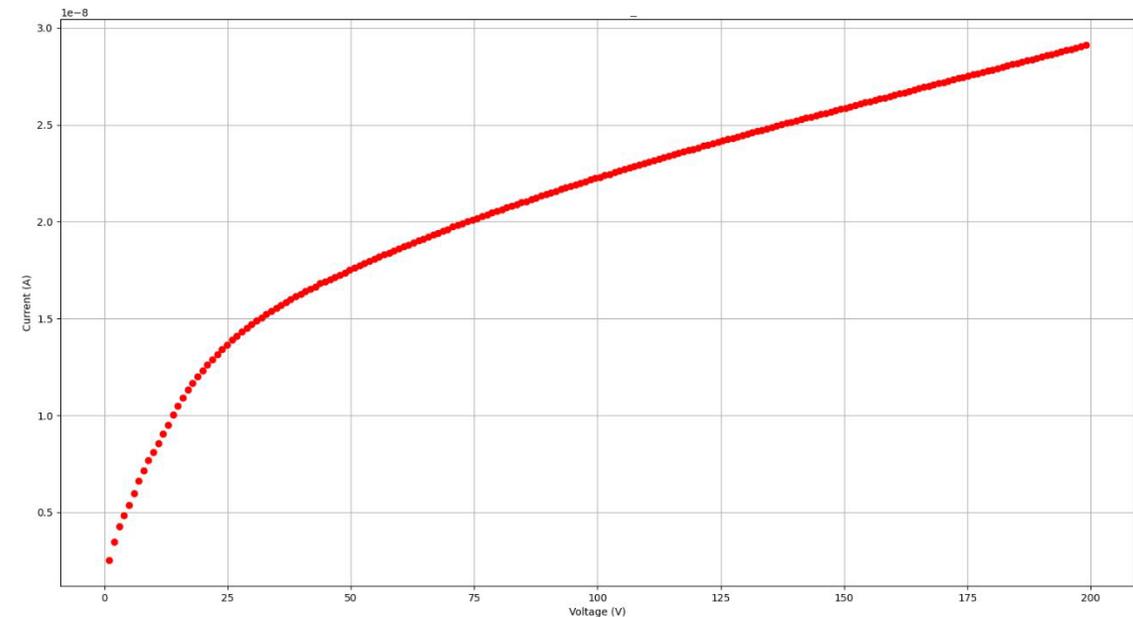
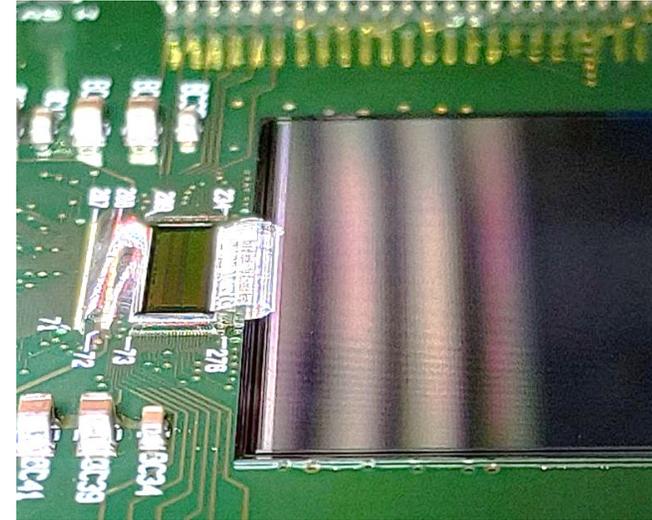
- ADCs for analog output digitization
- Analog/Digital Power Supplies
- Level shifters and SLVS converters
- Can accommodate both ASTRA-VI and ASTRA-64
- Trimmer resistors for external bias
- Sensor HV bias



DAQ

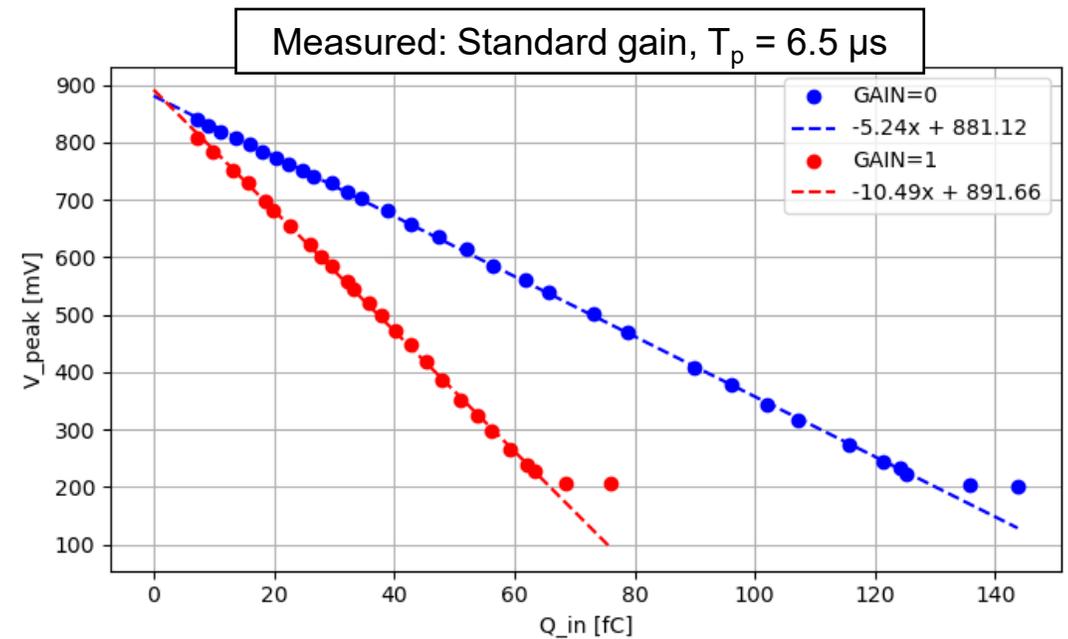
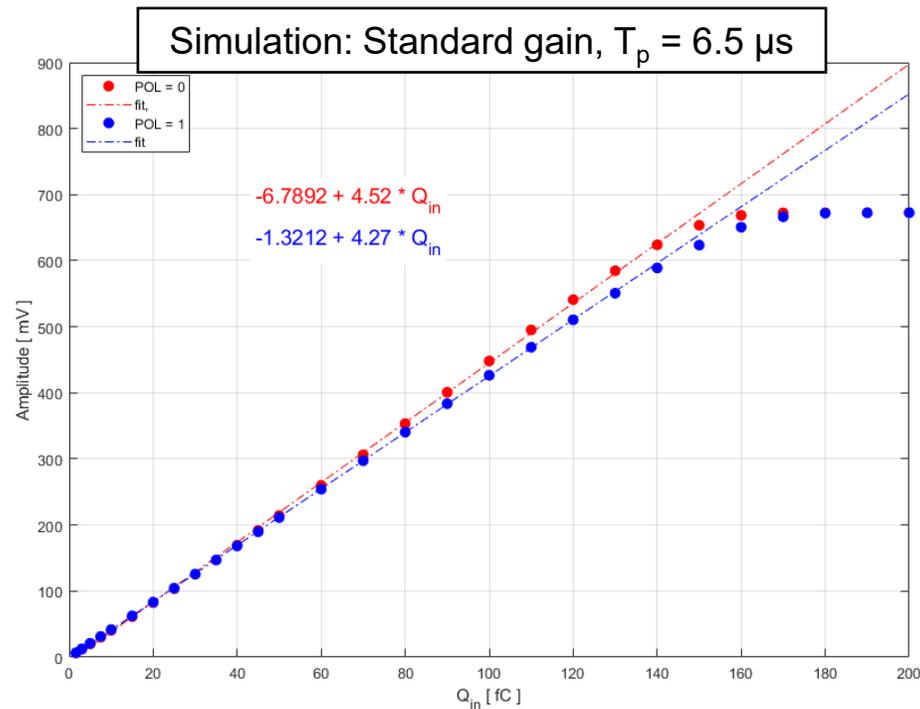
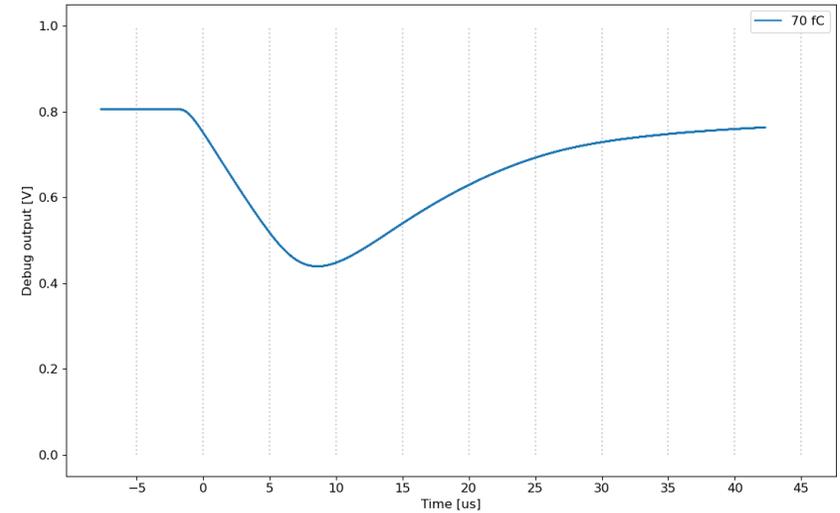
- ASTRA configuration, readout operations, and data acquisition
 - *Terasic DE10-Standard*
 - *Intel Cyclone V FPGA*

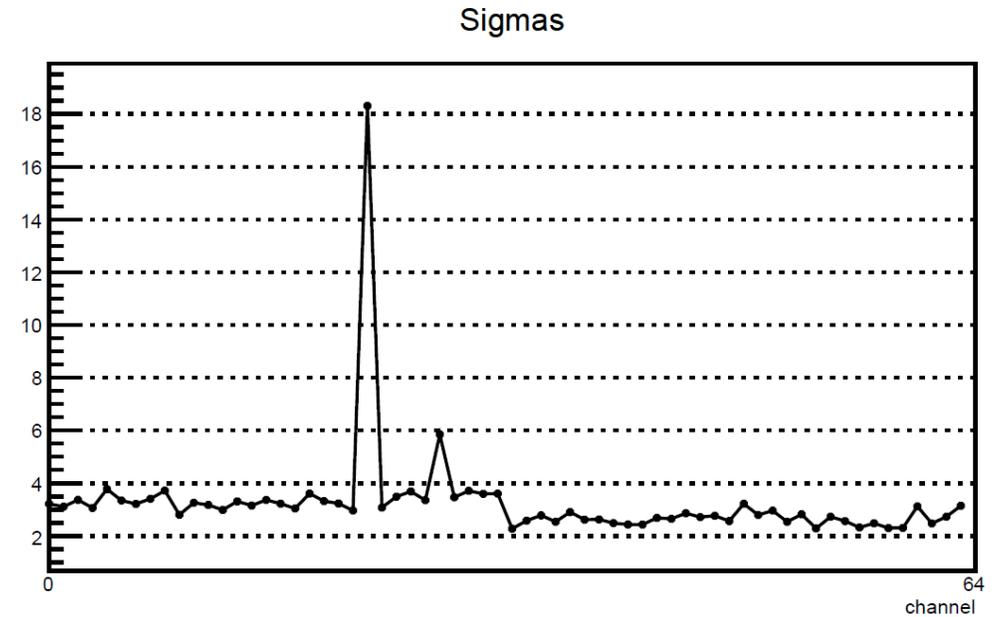
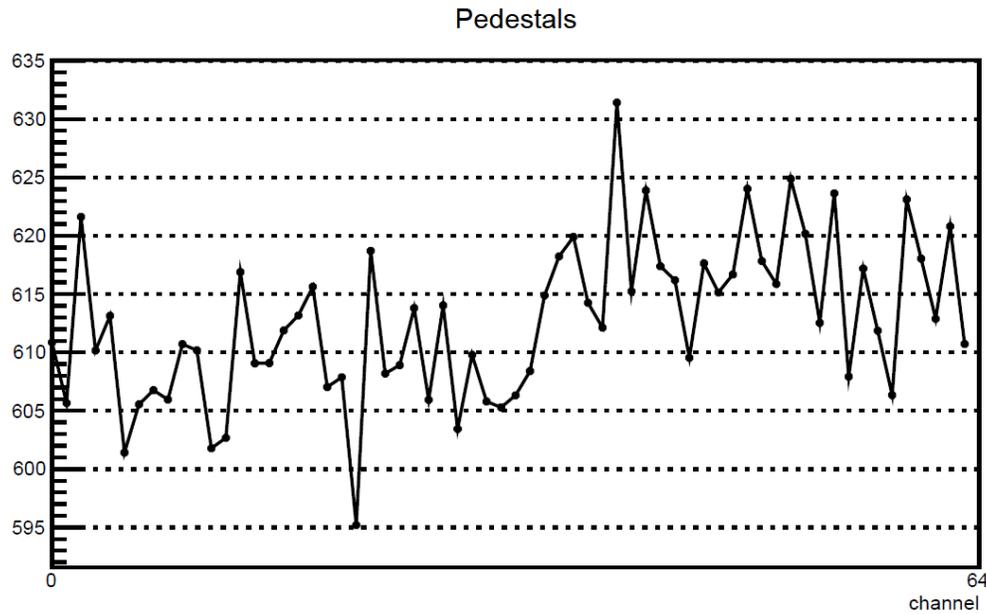
- Used the test board to characterize ASTRA-64
 - For the moment, we only verify the analog read-out
 - Started this month!
 - All the following are preliminary results
- Verification campaign to test all the functionalities
 - FOOT sensors
 - 3x3 mm²
 - 50 μm implantation pitch
 - 150 μm readout pitch
 - Integrated test-pulse injection
 - 1058-nm laser
 - ⁹⁰Sr radioactive source



ASTRA Characterization: Front-End Linearity

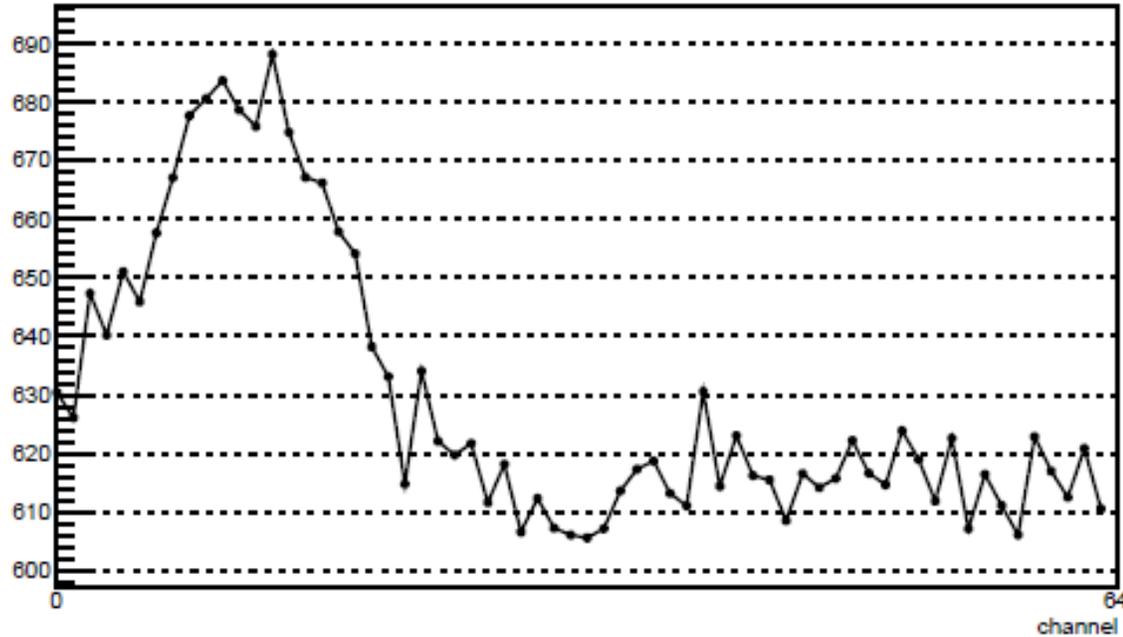
- Slow Shaper peak voltage (from debug output)
 - Integrated test-pulse injection
 - Shaping time settings: 6.5 μs
- Slightly higher gain compared to simulations
 - 5.24 mV/fC, 10.49 mV/fC
 - Compared to 4.3 mV/fC, 8.1 mV/fC



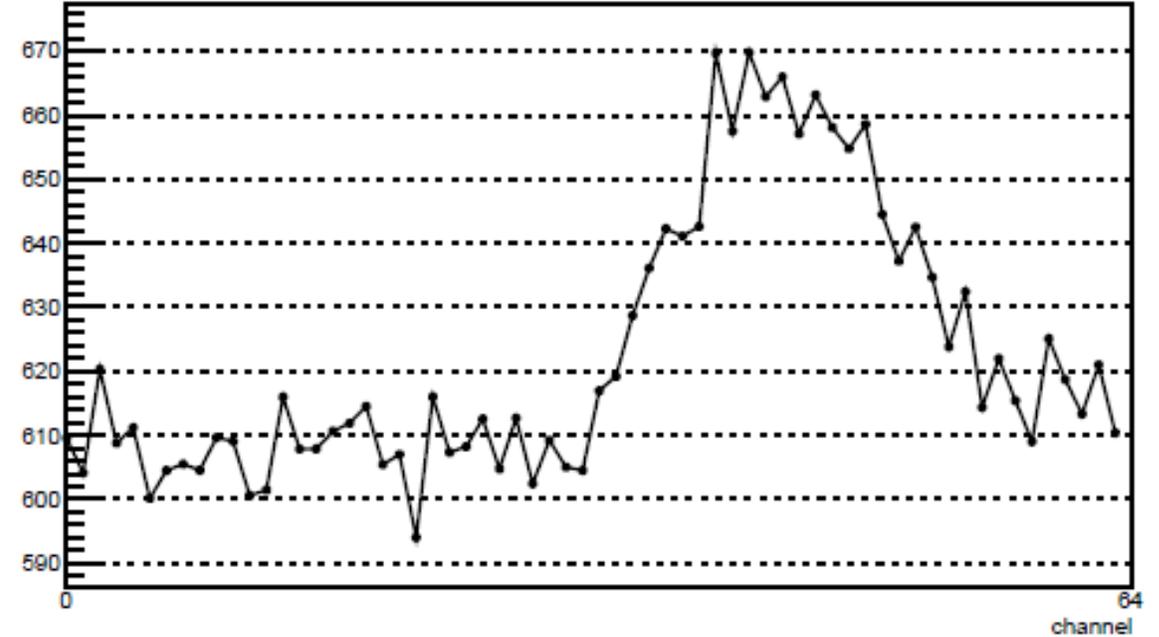


- Tested ASTRA analog output
 - Pedestal: base-line of the strips without crossing particles (average value)
- Same noise figures as in FOOT / POX / HERD hybrid boards

Pedestals



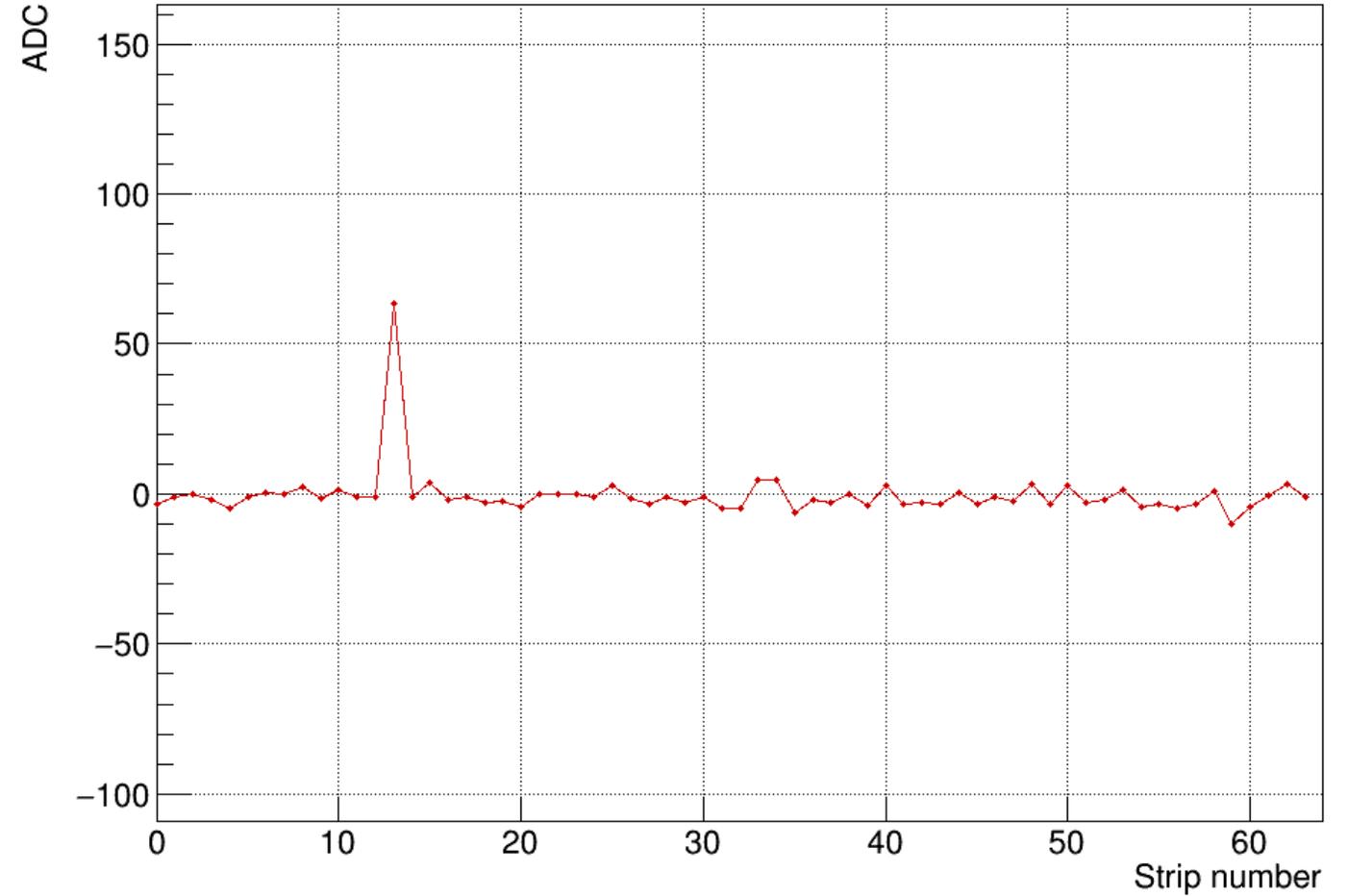
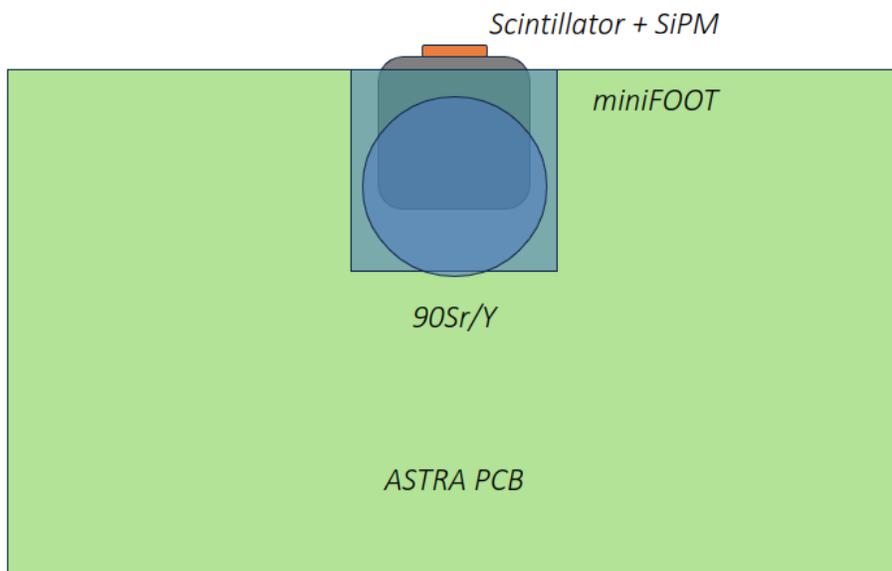
Pedestals



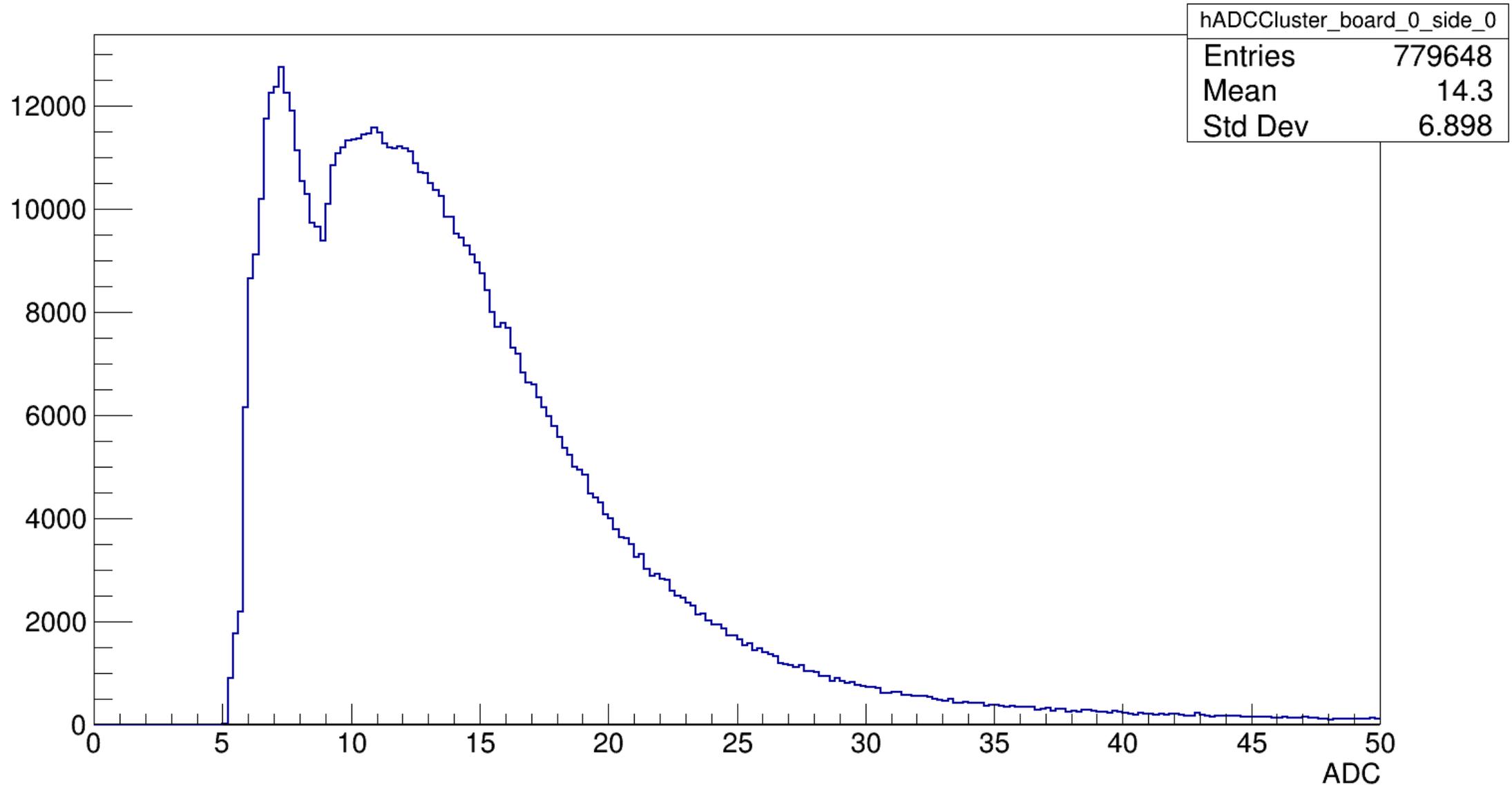
- Illuminated the sensor with 1058-nm laser
- Verified that both ASTRA-64 halves were receptive
 - Laser can only induce big signals onto the detector

ASTRA Characterization: ^{90}Sr Radioactive Source

- Moved to a ^{90}Sr radioactive source
 - Smaller signals w.r.t. laser
 - Can compare results with our existing detectors
- Setup with scintillator + SiPM
 - Supply a trigger signal to ASTRA
 - Source not perfectly centered
 - Empty events collected



ASTRA Characterization: ^{90}Sr Radioactive Source



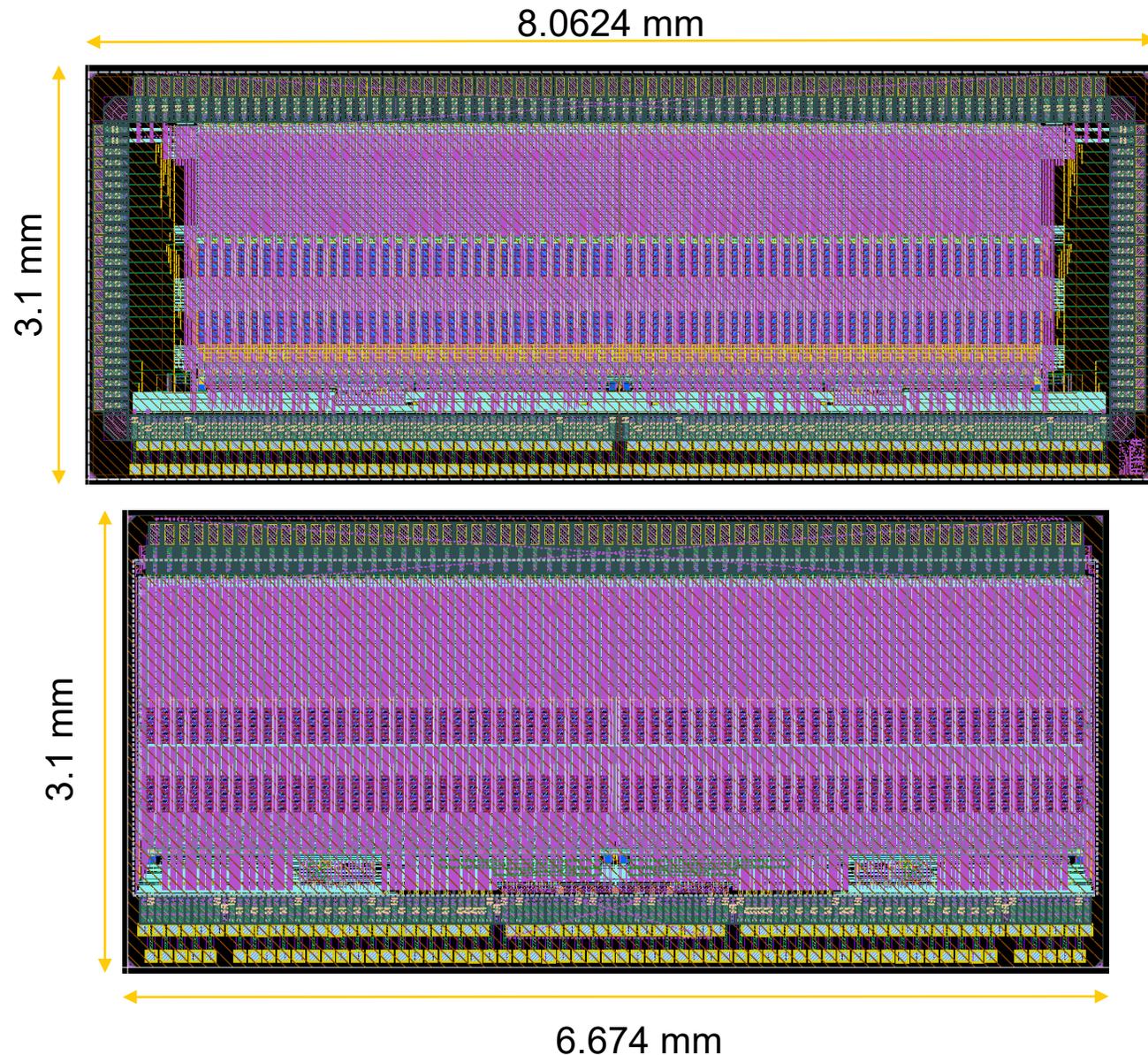
ASTRA Requirements and Specs

	Requirements	Specs (v1)
Channels	64	64
Dynamic Range	± 160 fC	± 160 fC
Linearity Region	± 160 fC	± 160 fC
Shaping Time	Adjustable in $1 \div 10$ μ s	1.5 μ s, 3.5 μ s, 6.5 μ s, 9 μ s
ENC	$< 1000 e^-$ @ C_{in} 100 pF	$< 1000 e^-$
Gain	-	5.2 mV/fC, 10.5 mV/fC
Output	Multiplexed pulse height Digitized pulse height Channels FastOR	Multiplexed pulse height, Digitized pulse height, Channels FastOR
Power supply	Positive (only) supply	1.2 V
Overall power consumption	-	Test board: 1.4 W
Channel power consumption	< 1 mW	< 1 mW 
Production Process	110 nm CMOS	110 nm CMOS
Size	6x6 mm ²	8.06x3.1 mm ²

Stage	Power/ch [μ W]
Preamplifier	300
Inverting stage*	24
Shaper	66
Fast Shaper	32
Discriminator	18
S&H	108
ADC	36
Single-to-Diff. Amp.	8
Output Buffers (2)	37
Counter + Serializer	0.12
SLVS RX (3)	9
SLVS TX (2)***	190

630 μ W/channel for analog readout
830 μ W/channel for digital readout

ASTRA-64 v1 vs v2

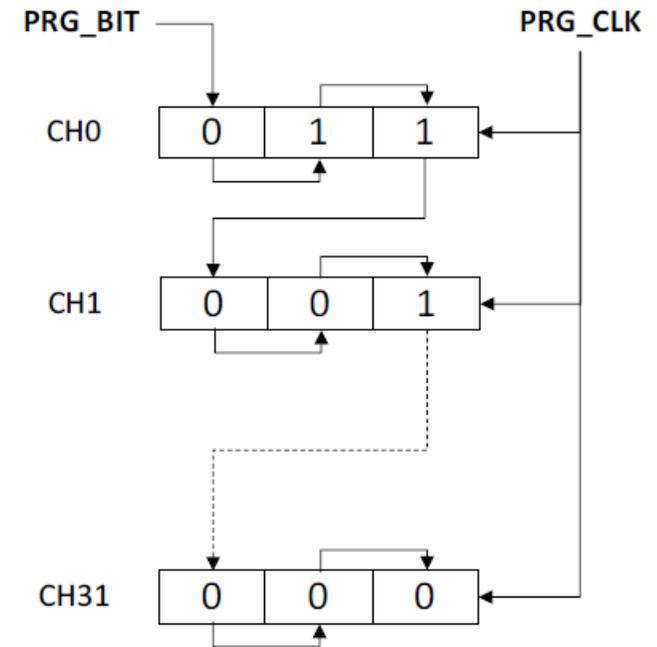


- Removed side pads to be 2-side abutable
- Already available from ARCADIA RUN2
- Design of PCB hosting ~4 ASTRA-64 v2 ASICs starting soon

- ASTRA: 64-channel ASIC readout electronics for Si μ Strips
 - in house design of versatile chip
 - possible application in different space and ground experiments
- Each ASTRA channel performs signal amplification and charge measurement
 - Positive and negative input signal polarities readout capability
 - 2 gain settings providing input dynamic range up to 80 or 160 fC
 - 4 peaking time configurations: 1.5 μ s, 3.5 μ s, 6.5 μ s, 9 μ s
 - Dual-readout mode: analog and digital
 - FastOR trigger output
- ASTRA electrical characterization just started this month!

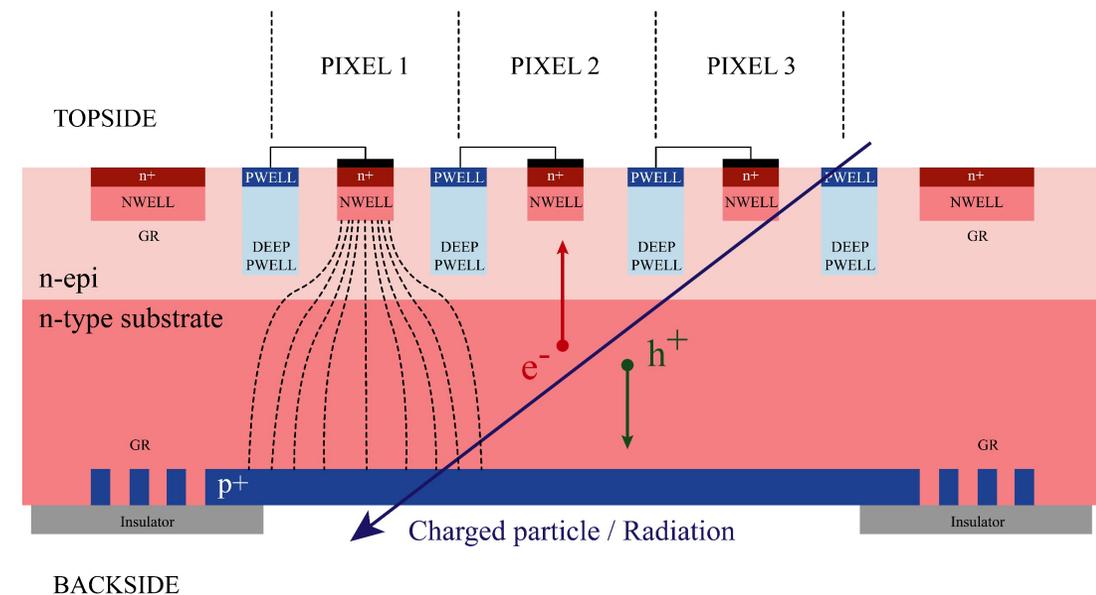
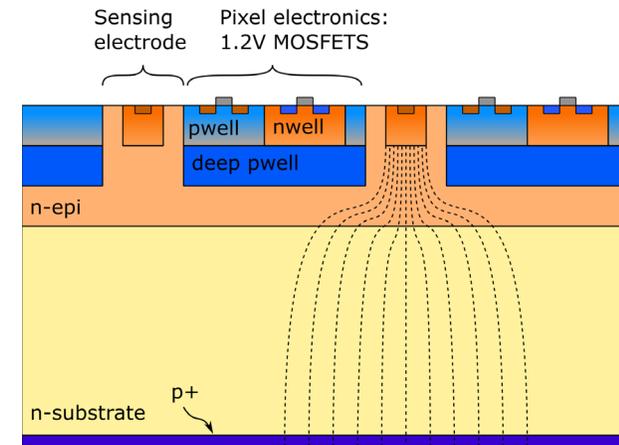


- Each channel has 3-bit configuration
 - `ch_mask`: masks the selected channel in readout
 - Mutes noisy channels
 - `tp_en`: enable the test-pulse injection circuitry
 - `disc_en`: enables the discriminator output
 - Prevent high-rate of triggers when there are noisy channels
- The user can write the configuration as a shift-register



Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

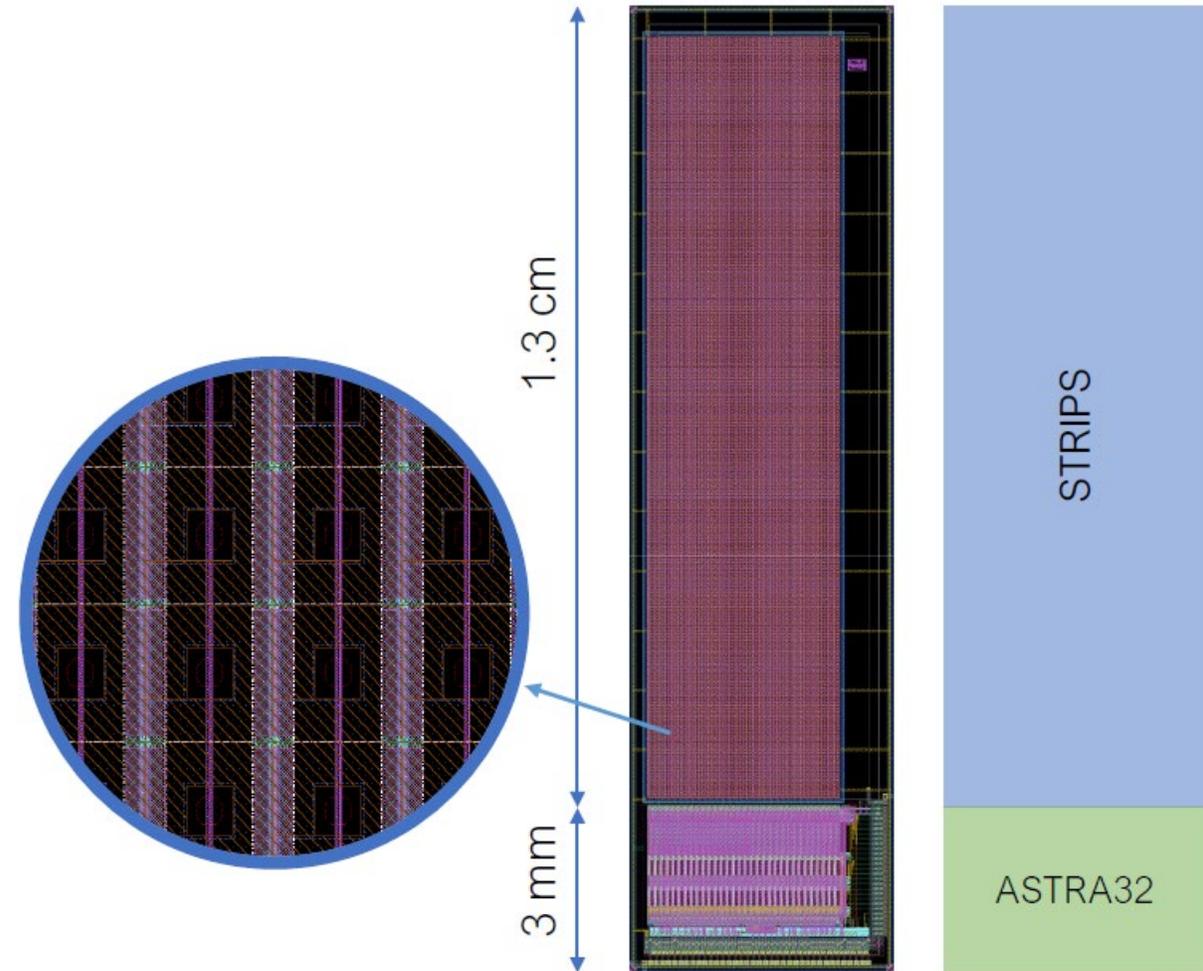
- 110 nm CMOS process (LFoundry)
- n-type high resistivity active region
- Fully depleted substrate: depletion grows from back to top
- Electronics buried in deep p-well
- Sensing electrodes biased at low voltage ($< 1V$)
- CMOS circuitry can be implemented, but no triple well process for deep n-well NMOS isolation
- Only HVT transistors (1.2 V) available



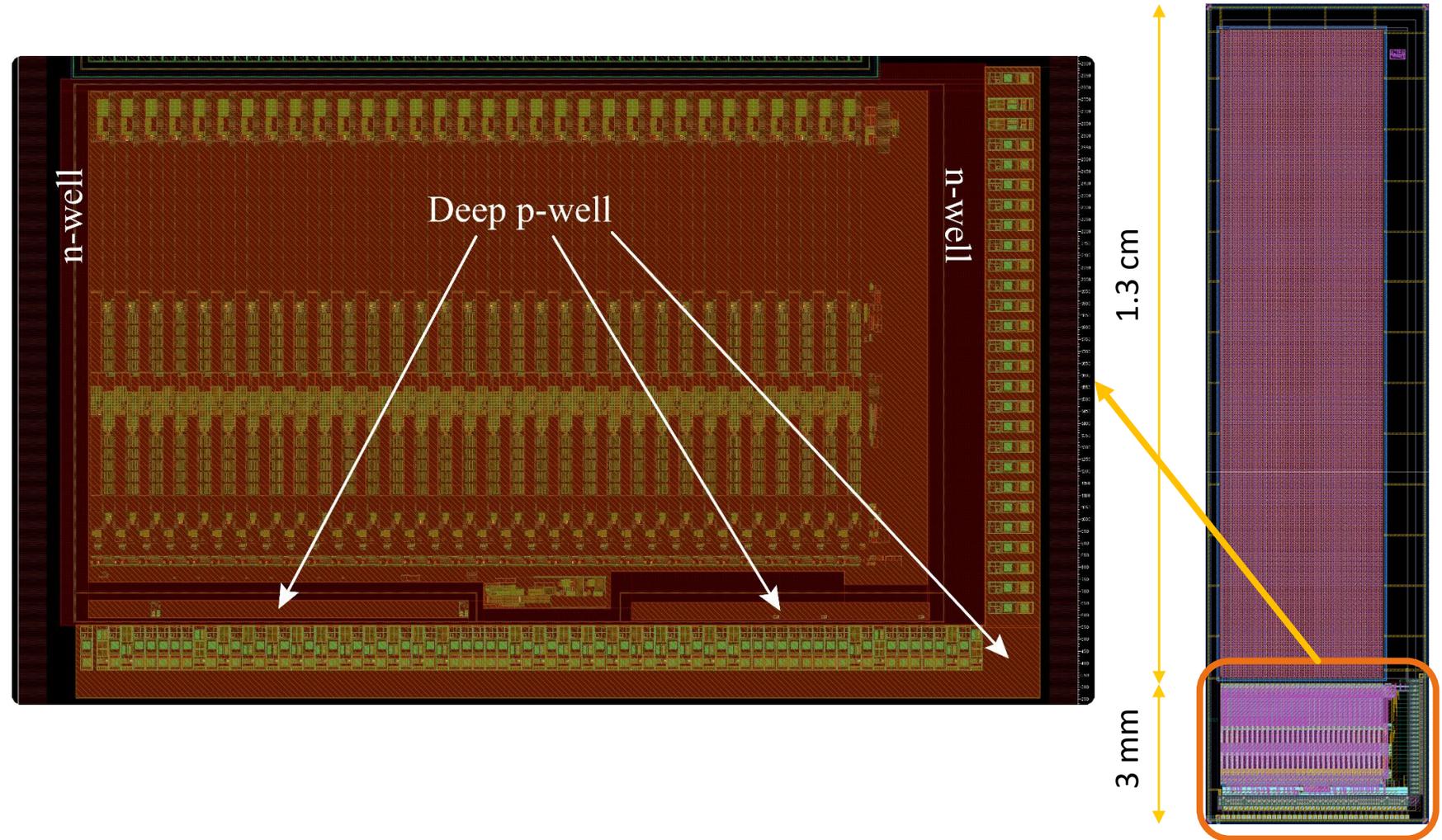
ASTRA-VI with Monolithic Si-Strips

Fully depleted monolithic pixelated strips based on ARCADIA sensor design

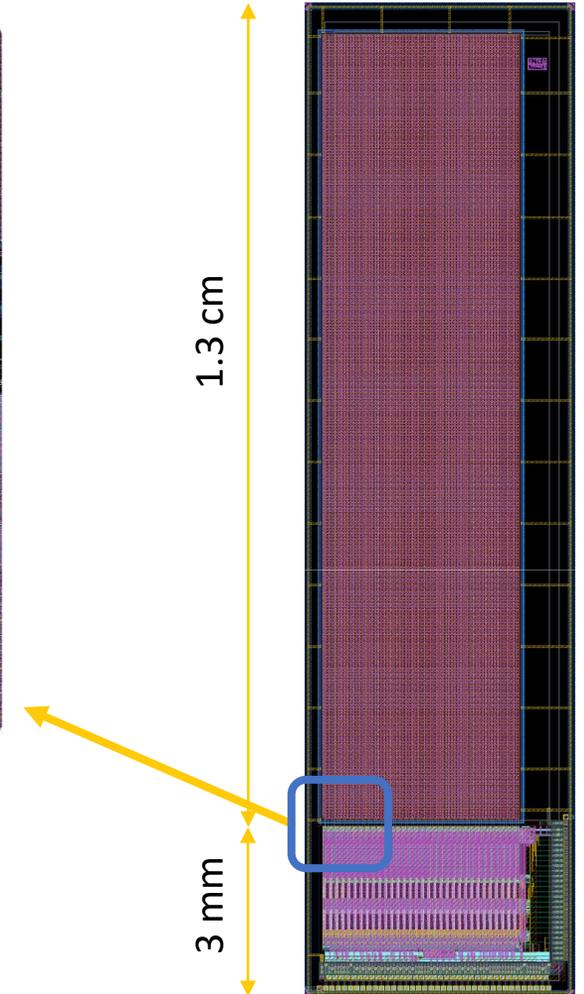
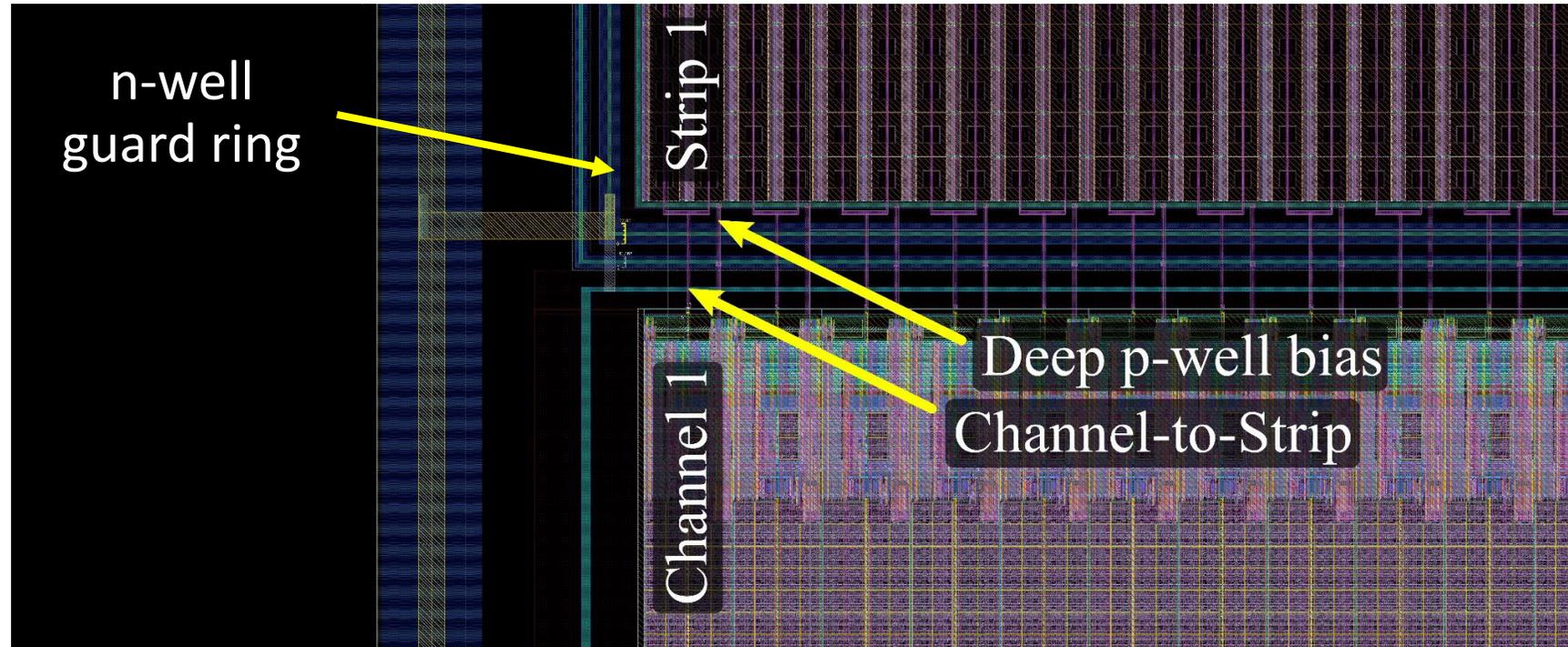
- 32 columns of 2 x 256 pixels connected in parallel
- 50 x 50 μm^2 pixels
- Total strip capacitance between 5 and 10 pF
- The 32 columns are read by an array of 32 readout channels
- Modular layout allows to characterize the electronics independently of the microstrips
- Future versions with the electronics fully included in the deep p-wells in the microstrips allowing wafer-level detector stitching



- Electronics enclosed in a large deep p-well
- Protected by n-well guard rings
- Guard rings are biased at 1.2 V
- They collect stray electrons generated in the substrate directly below the electronics



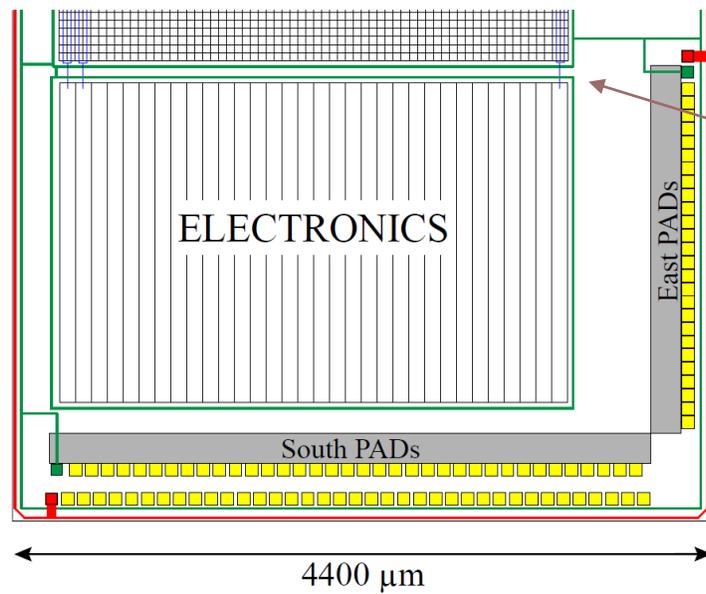
Strips – Electronics Interface



- Two pixel-columns connected to channel FE input using top metal (ME6)
- GND connection to the deep p-wells surrounding the pixels active region
- n-well guard ring also around the microstrips to collect stray electrons generated in the depleted substrate outside the active sensor volume

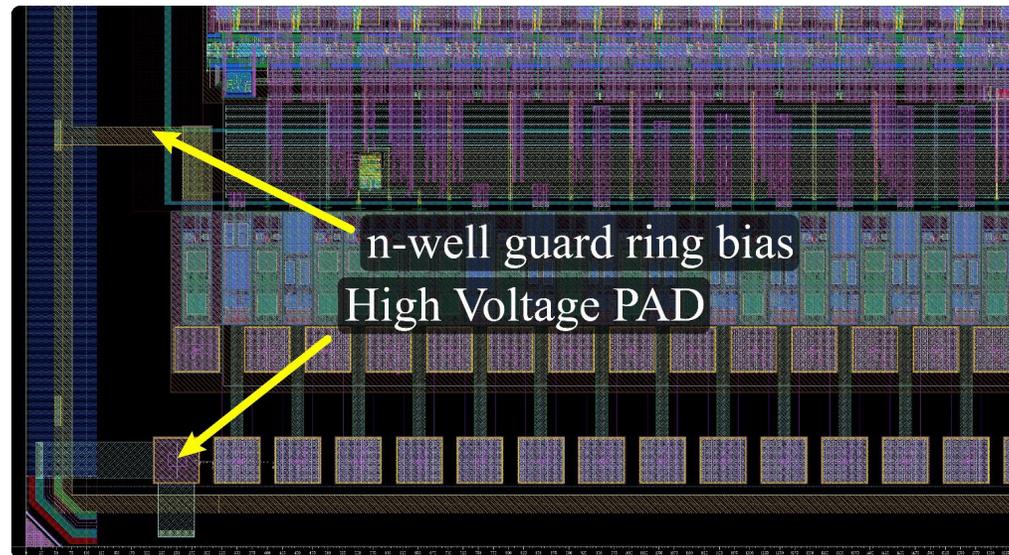
Top-Side Back-Biasing

Substrate bias can be applied also from the top via dedicated pads



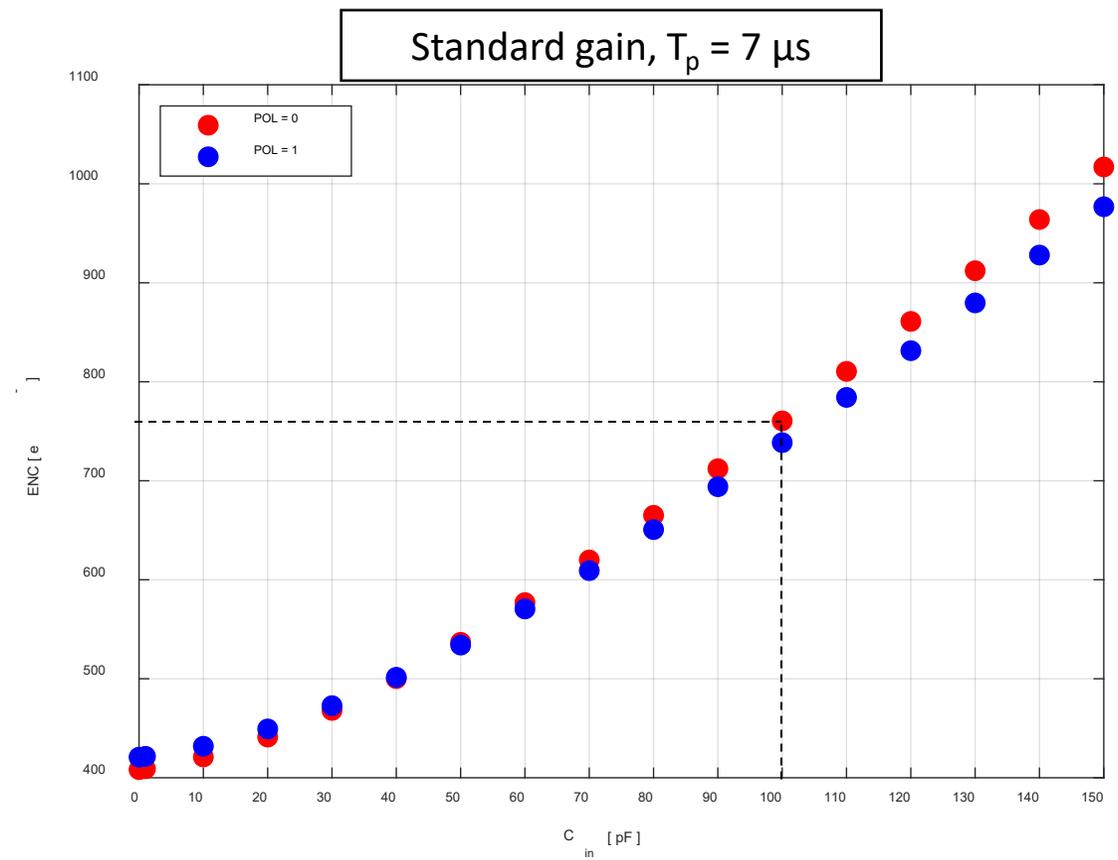
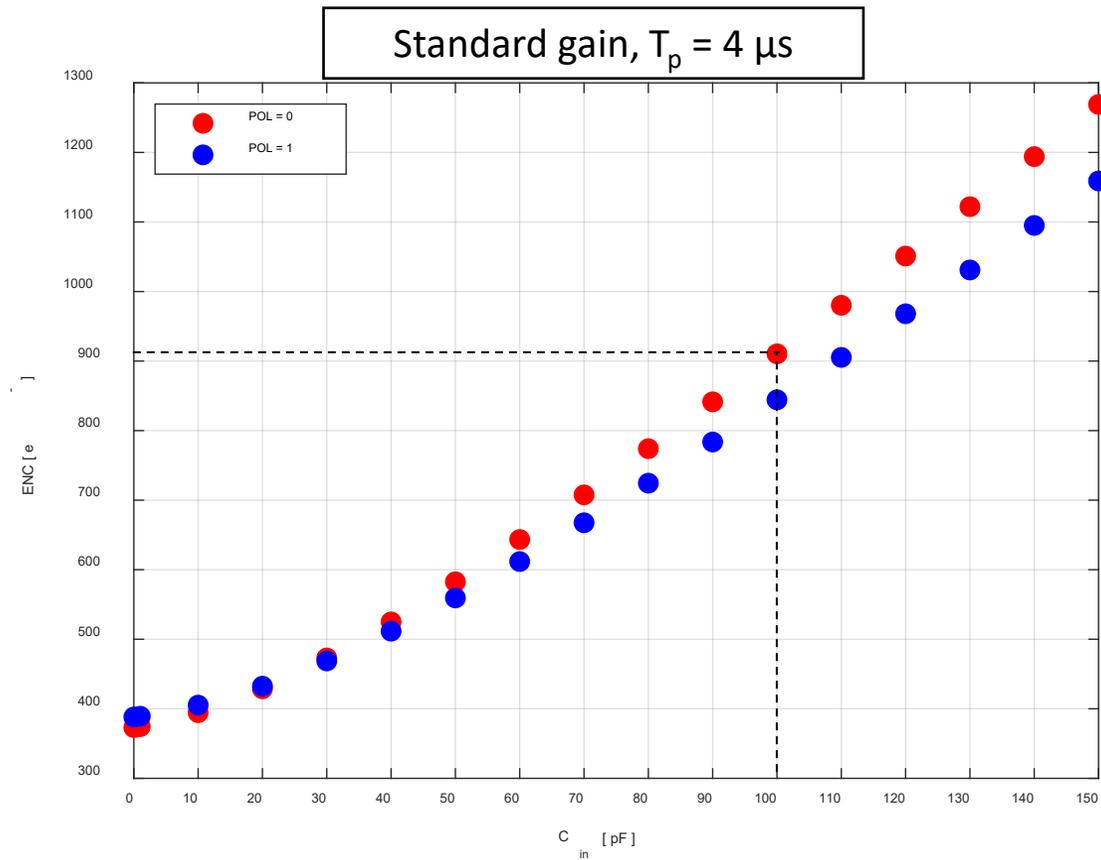
top-side back biasing
p-well structure

n-well 1.2V guard ring

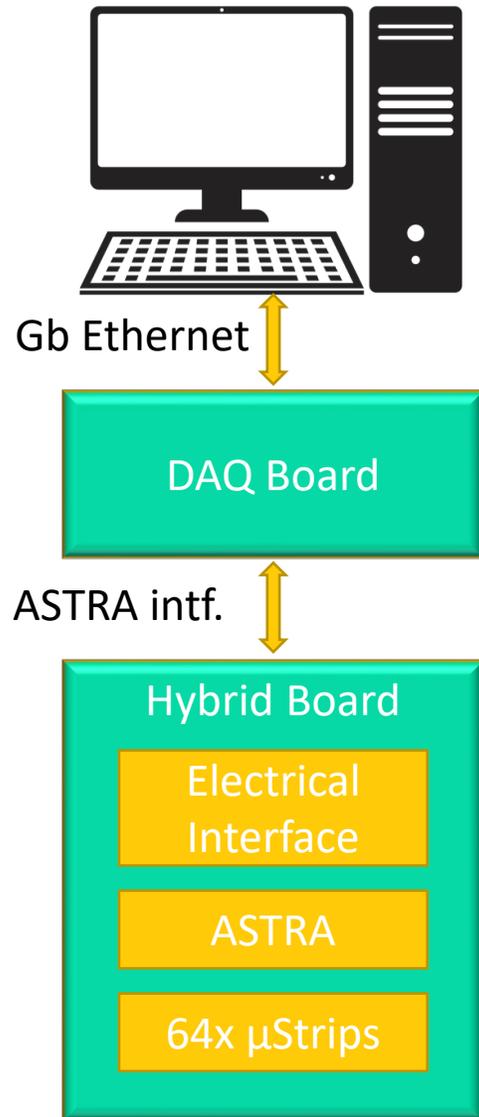


1.3 cm

3 mm



ASTRA64 DAQ Block Diagram



- DAQ Configuration
- DAQ Control

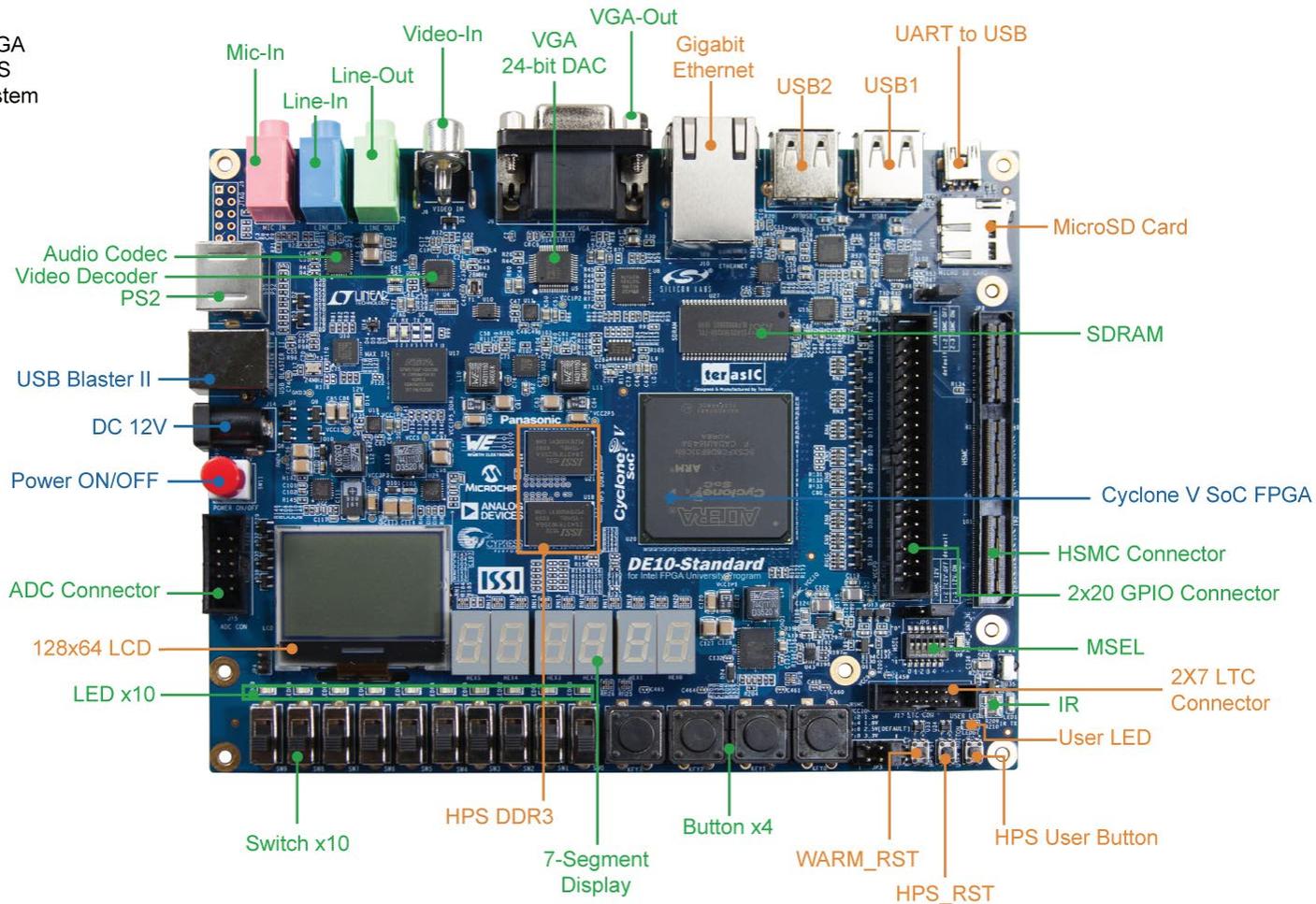
- ASTRA Configuration Parameters
- Long-Term storage

- ASTRA Control
- ASTRA Digital Readout
- ASTRA Analog Readout

- Host ASTRA
- Host 64- μ Strip Detector
- Electrical Adaptation to the DAQ Board

- Digitization Chain for the ASTRA Analog Out

DAQ Board: Terasic DE10-Standard



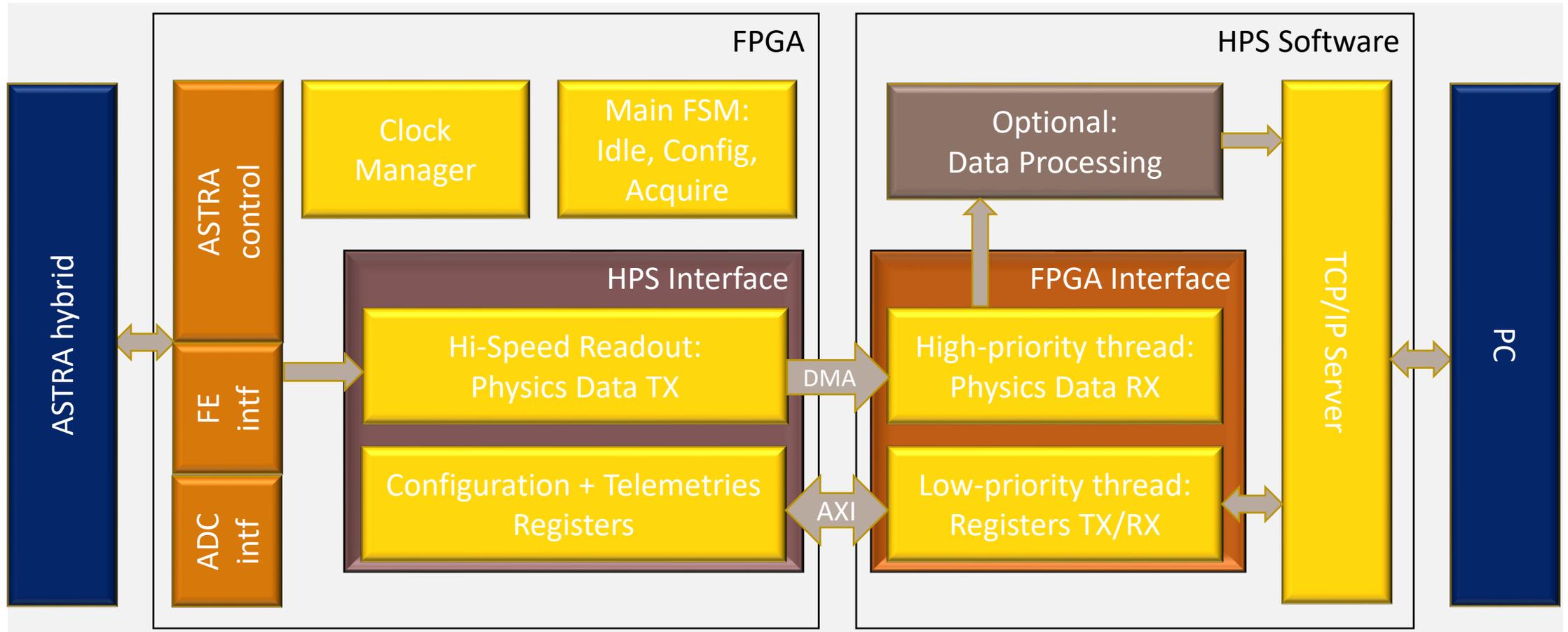
FPGA

- 1x Intel Cyclone V 5CSX
- 1x HSMC with Configurable I/O standard 1.5/1.8/2.5/3.3
- 1x 40-pin expansion header
- 1x USB-Blaster II onboard for programming

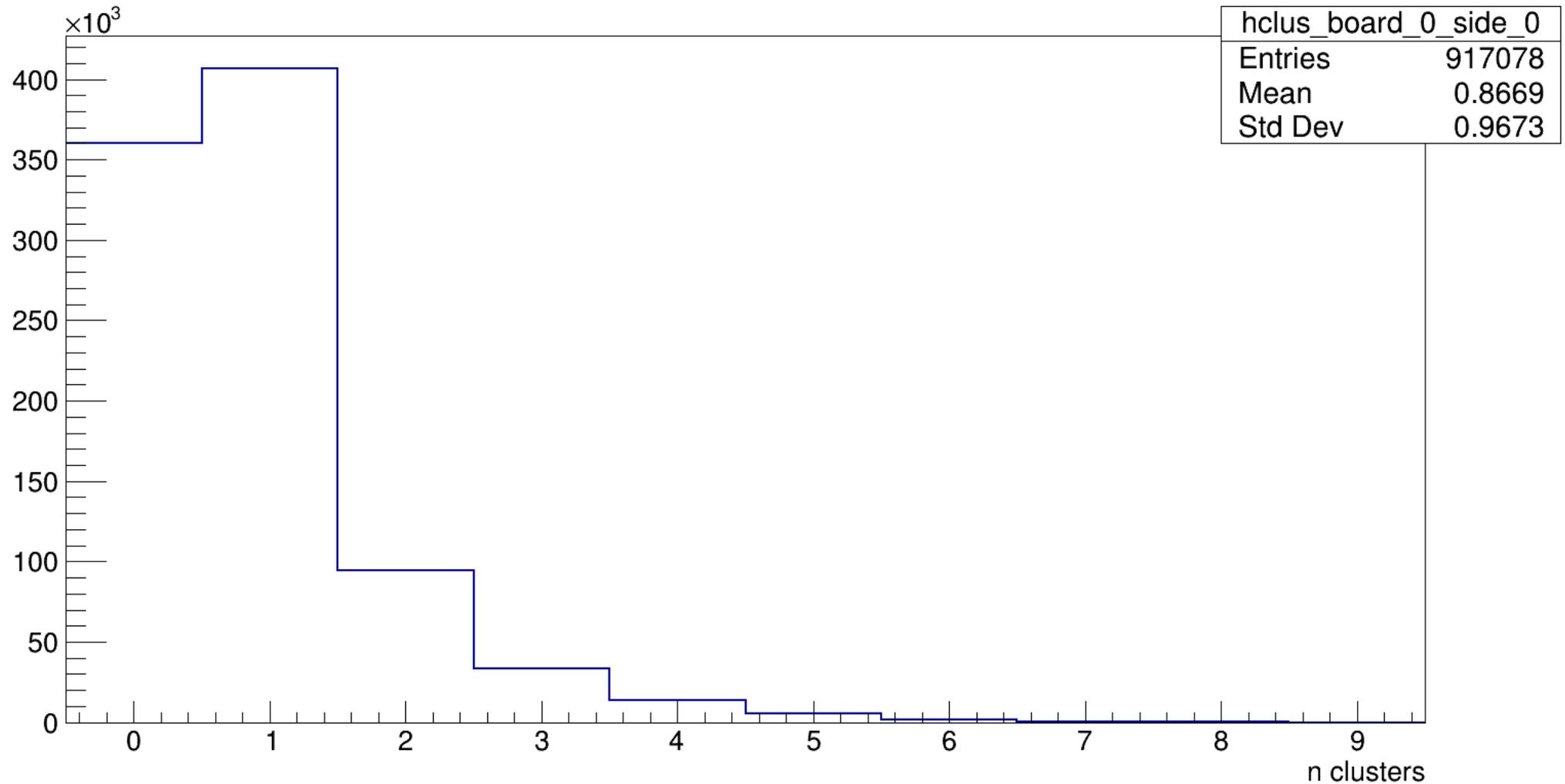
HPS (Hard Processor System)

- 1x 925 MHz Dual-core ARM Cortex-A9 processor
- 1 GB DDR3 SDRAM
- 1 Gigabit Ethernet PHY with RJ45 connector

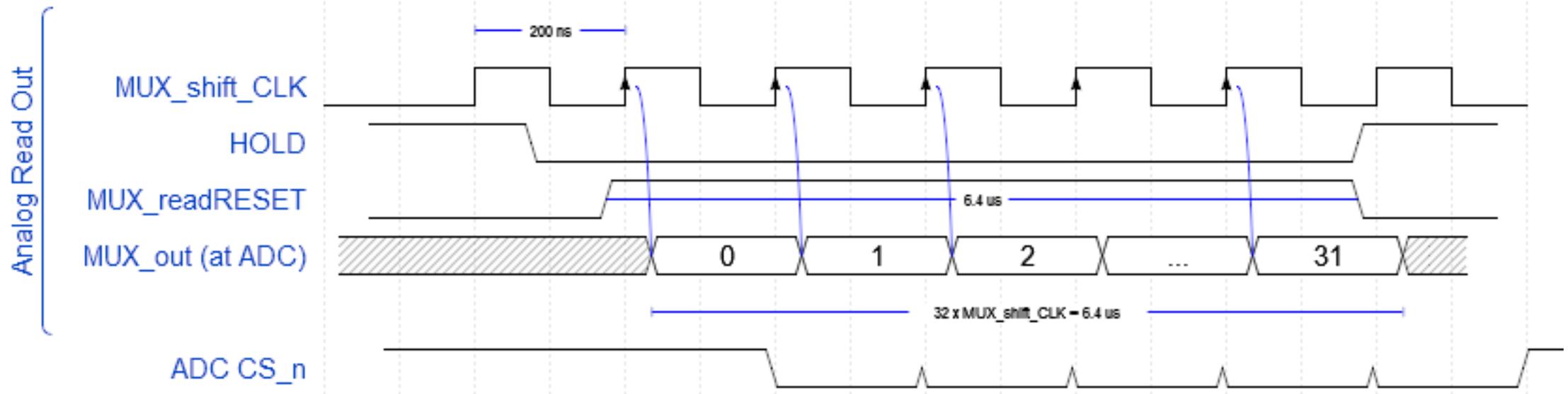
DAQ Board Architecture



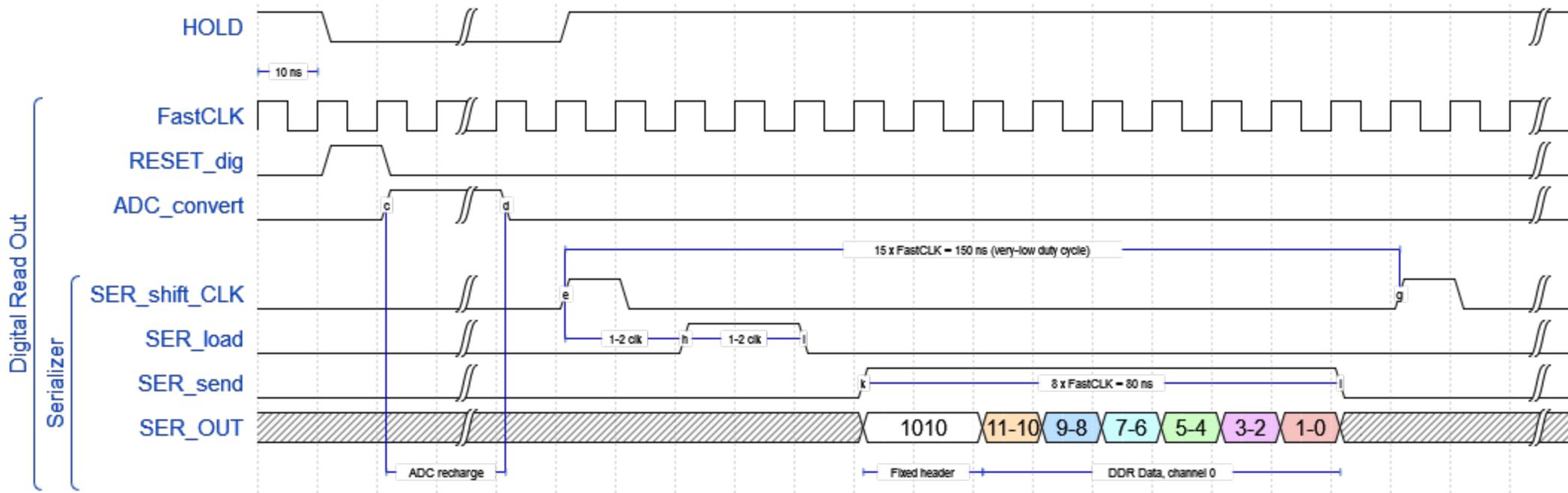
ASTRA Characterization: ^{90}Sr Radioactive Source



ASTRA Readout Operations – Analog Out



ASTRA Readout Operations – Digital Out



- 64 channels
- Charge-Sensitive Amplifier
 - 5.7mV/fC gain
 - ± 200 fC dynamic range
 - Linear in the ± 72 fC region
- 6.5 μ s shaper
- Sample-and-hold circuitry
 - Overall 2.6 μ A/fC gain
- Equivalent Noise Charge: 139 e⁻ +5 e⁻/pF
- Differential output analog multiplexer
- +1.5 V / -2 V power supplies
- 21 mW power consumption
 - 327 μ W per channel

