



Contribution ID: 76

Type: **Oral**

## A mixed-signal read out ASIC for silicon micro-strip detectors

*Friday 23 June 2023 12:15 (20 minutes)*

ASTRA-64 (Adaptable Silicon sTrip Read-out Asic) is a 64-channel mixed-signal ASIC mainly designed to read-out micro-strip silicon detectors. Its first target application is the Silicon Charge Detector of the HERD facility, to be installed onboard the Chinese space station to provide tracking and complementary charge measurement.

ASTRA-64 is designed in 110nm technology and consists of two identical mirrored blocks, each of which has 32 channels. Each channel includes a Charge Sensitive Amplifier, with 2 programmable gain settings suited for both input signal polarities, followed by a shaper with programmable peaking time to optimize the noise performance according to the detector capacitance. The front-end gain has been set to provide a linear charge measurement of up to 160 fC in standard gain configuration and up to 80 fC for high gain configuration.

ASTRA-64 allows for two readout modes. In the analog readout mode, the sampled voltages stored in each channel are sent off-chip using an analog multiplexer coupled with a differential output buffer. In the digital readout mode, each channel employs its Wilkinson ADC to digitize the sampled voltages and a common serializer to send off-chip the digital information using an SLVS driver.

In addition, a fast shaper is coupled with a leading-edge hysteresis discriminator and the outputs of the 32 channels discriminators are combined in a FAST-OR logic to deliver a fast trigger signal off-chip. This signal can be employed by the DAQ system to perform trigger logic operations and eventually send it back to the ASIC as the HOLD signal to perform the charge measurement. The ASIC dissipates less than 600  $\mu$ W per channel to cope with the very strict constraints on power consumption for space applications.

### Eligibility for "Best presentation for young researcher" prize

Yes

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**Session Classification:** Research and Development of novel instrumentation for particle measurements in space

**Track Classification:** Research and Development of novel approaches and instruments for particle and high-energy radiation measurements in space