Access to 65nm Technology through CERN

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Overview of Technologies

- Foundry services & Technology technical support provided by CERN.

CMOS 8RF-LM

Low cost technology for Large Digital designs

CMOS 8RF-DM

Low cost technology for Analog & RF designs

BiCMOS 8WL

Cost effective technology for Low Power RF designs

BiCMOS 8HP

High Performance technology for demanding RF designs

CMOS 9SF LP/RF

High performance technology for dense designs

130nm CMOS

90nm CMOS

CMOS 65 LP

High performance technology for dense designs

65nm CMOS

- Mainstream technology CMOS8RF-DM (130nm)
  - Full support: CERN compiled Mixed-Signal design kit
- Advance technology CMOS9LP/RF (90nm)
  - Limited support: Project specific.
  - Development of a “lightweight” standard cell library is in progress.
- Future technology CMOS10 (65nm)
  - Plans to evaluate 65 nm processes for SLHC applications.
  - Access to Physical Design Kit.
  - No user support yet.

65nm Technology

- The TSMC 65nm technology is a candidate technology.
- Radiation Tolerance Qualification work is in progress
  Test Results are being presented at TWEPP 2011:
  - "Characterization of a commercial 65nm CMOS technology for SLHC applications"
    by Sandro Bonacini, on Thursday 29/9
  - "News on SEU test in 90nm & 65nm technologies"
    by Sandro Bonacini, on SEU MUG session
- Negotiations are in progress with IMEC and the foundry to obtain access to IP libraries
- Development of a Mixed Signal Design Kit integrating foundry IP libraries having the physical layout views available.

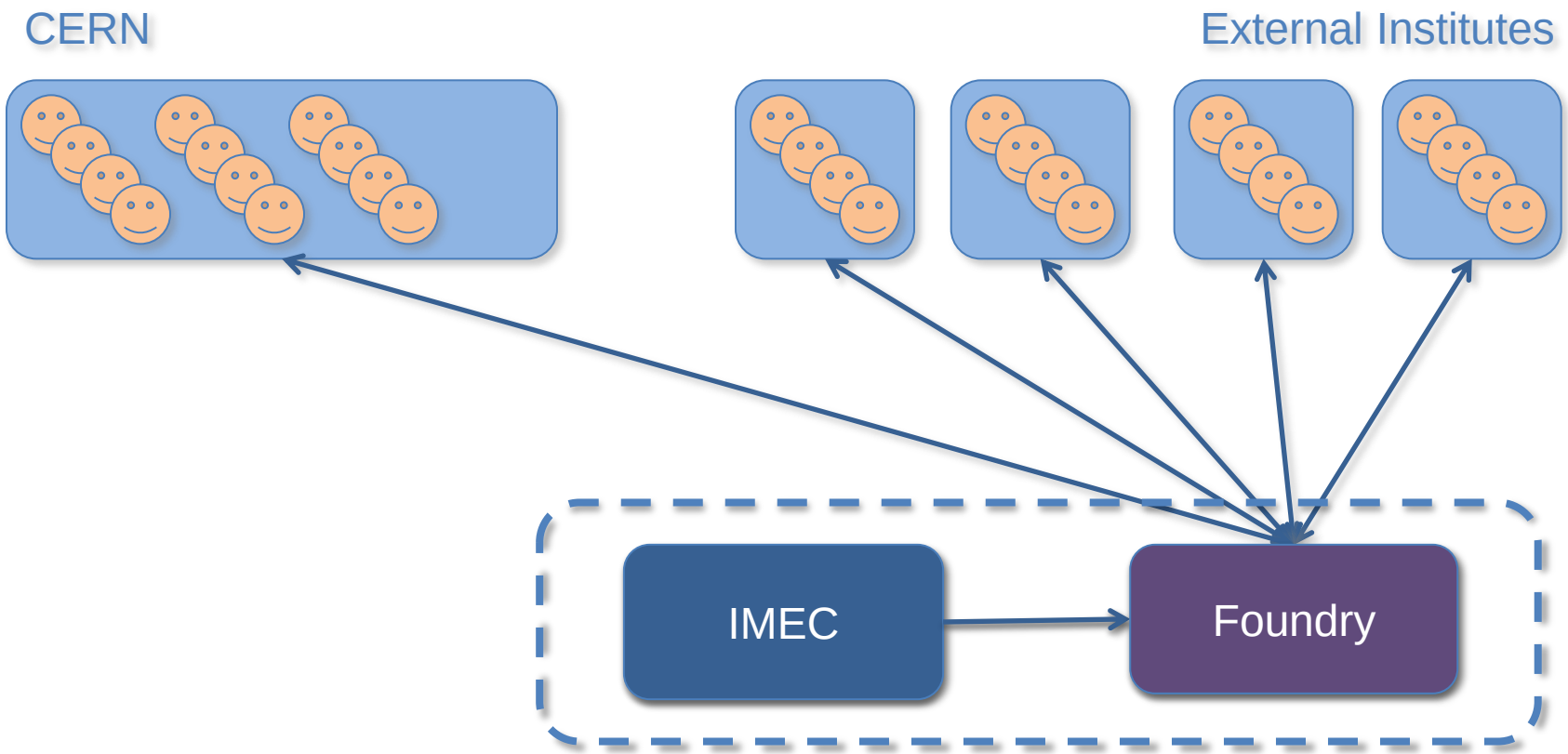
65nm Technology

- We plan to offer:
  - A Mixed Signal Design Kit that supports the same design work flows as the 130nm design Kit.
  - Provide access to memory compiler services.
  - Provide access to foundry services via IMEC.
    - MPWs, Engineering runs, Production runs.

- Decide on a unique set of technology options.
  - Preliminary selection of Technology options:
    - TSMC 65nm LP (Low Power), LO (logic), with 6 metal layers.
    - Core vdd: 1.2V, IO vdd: 2.5V, 3.3V
  - NRE cost is strongly modulated by extra technology options.
  - Very costly to support multiple design kits of different technology options.

Preliminary information

65nm Technology Access (NDAs)



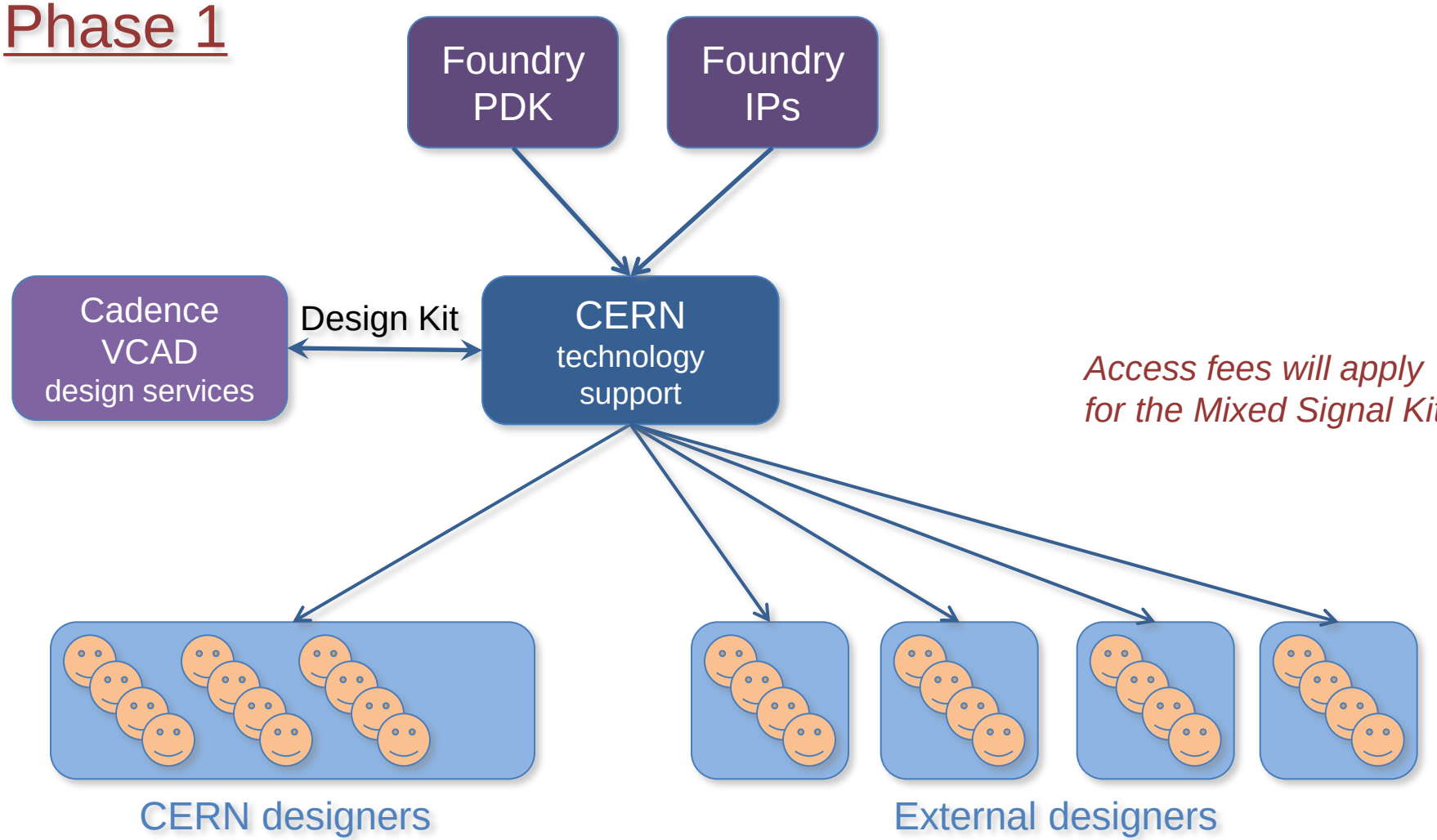
Signing an NDA to access technology data

1. Request access to IMEC
2. IMEC contacts Foundry
3. Sign NDA vis-à-vis with Foundry

Preliminary information

65nm Technology Support Services

Phase 1

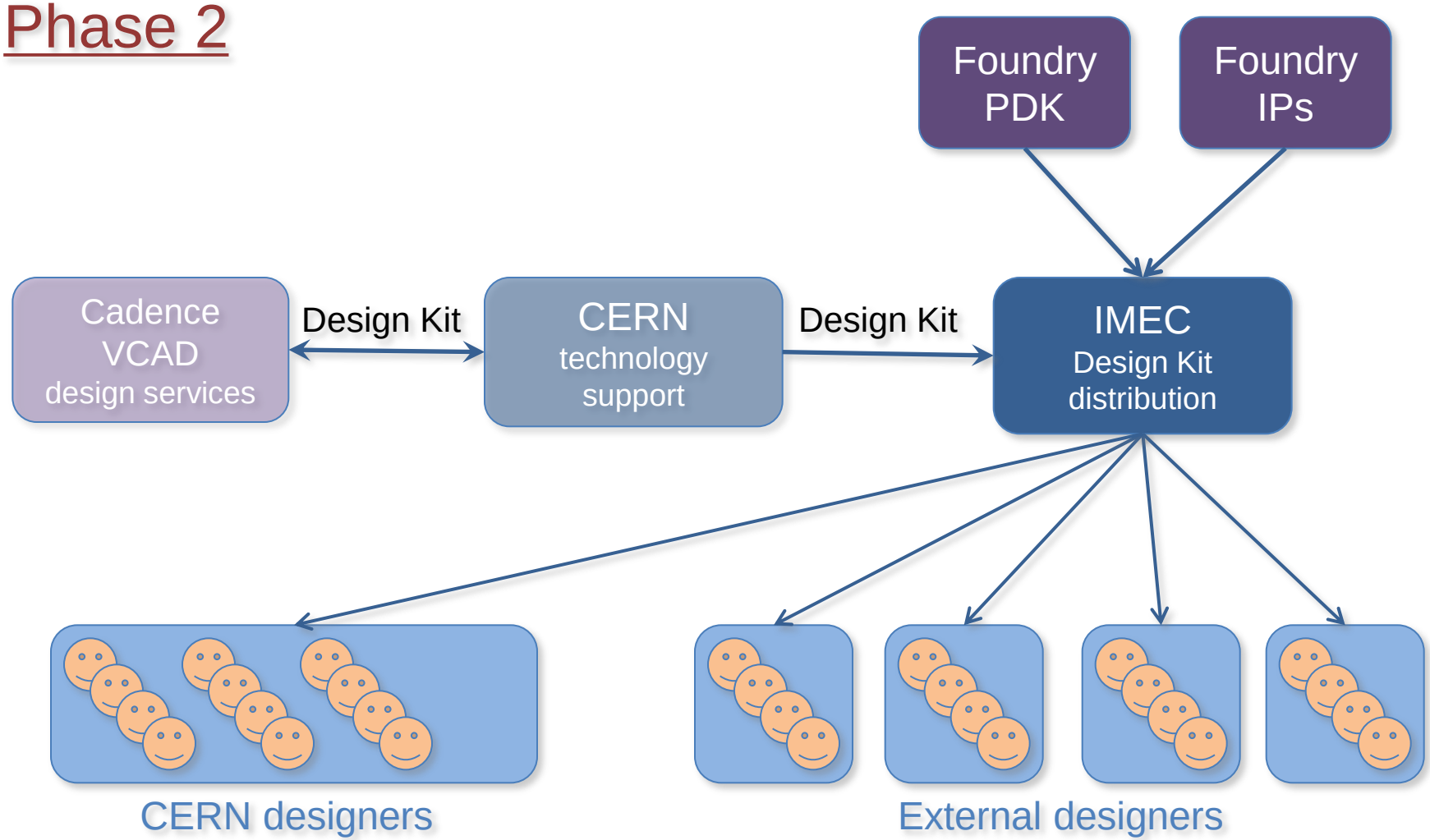


Access fees will apply for the Mixed Signal Kit

Preliminary information

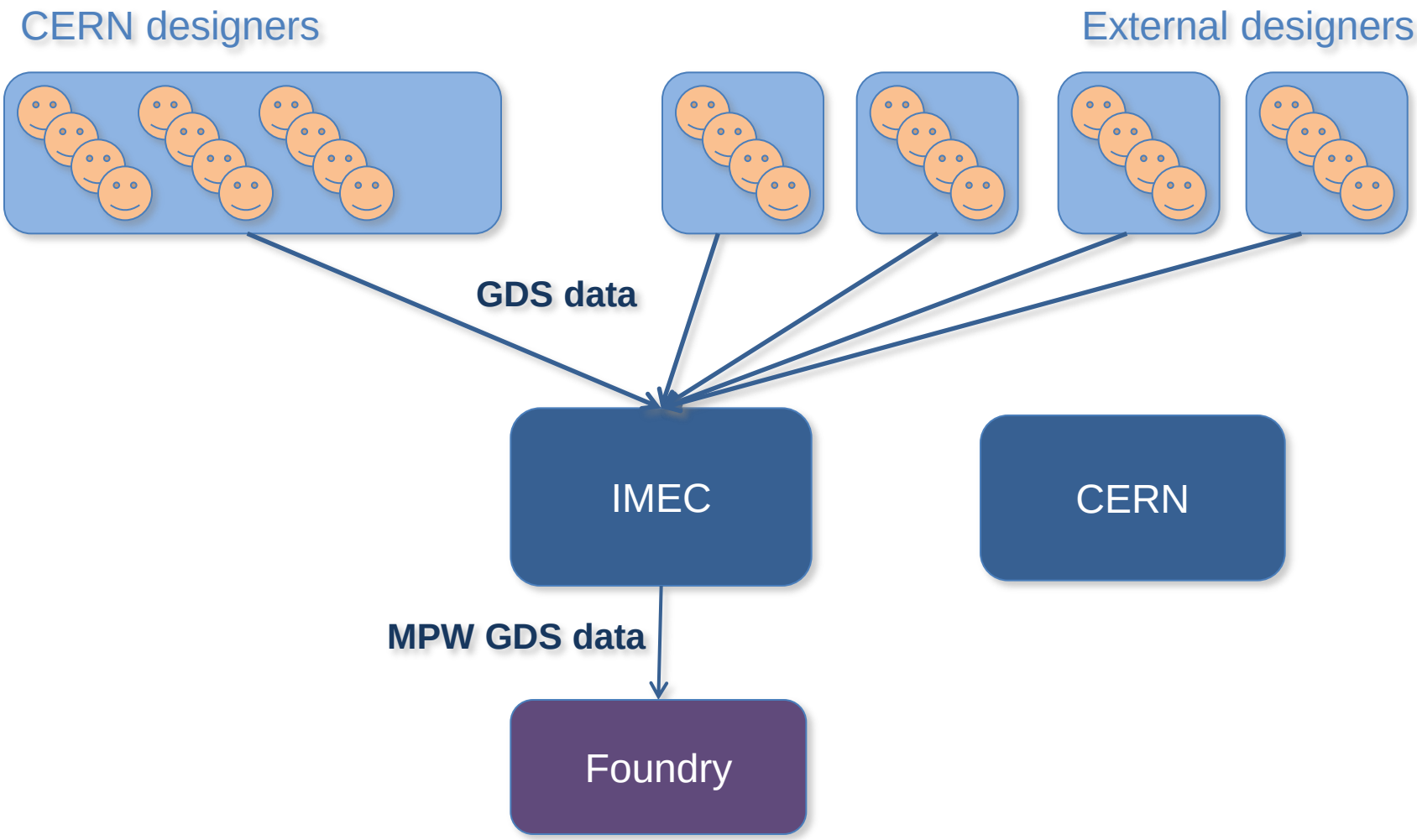
65nm Technology Support Services

Phase 2



Preliminary information

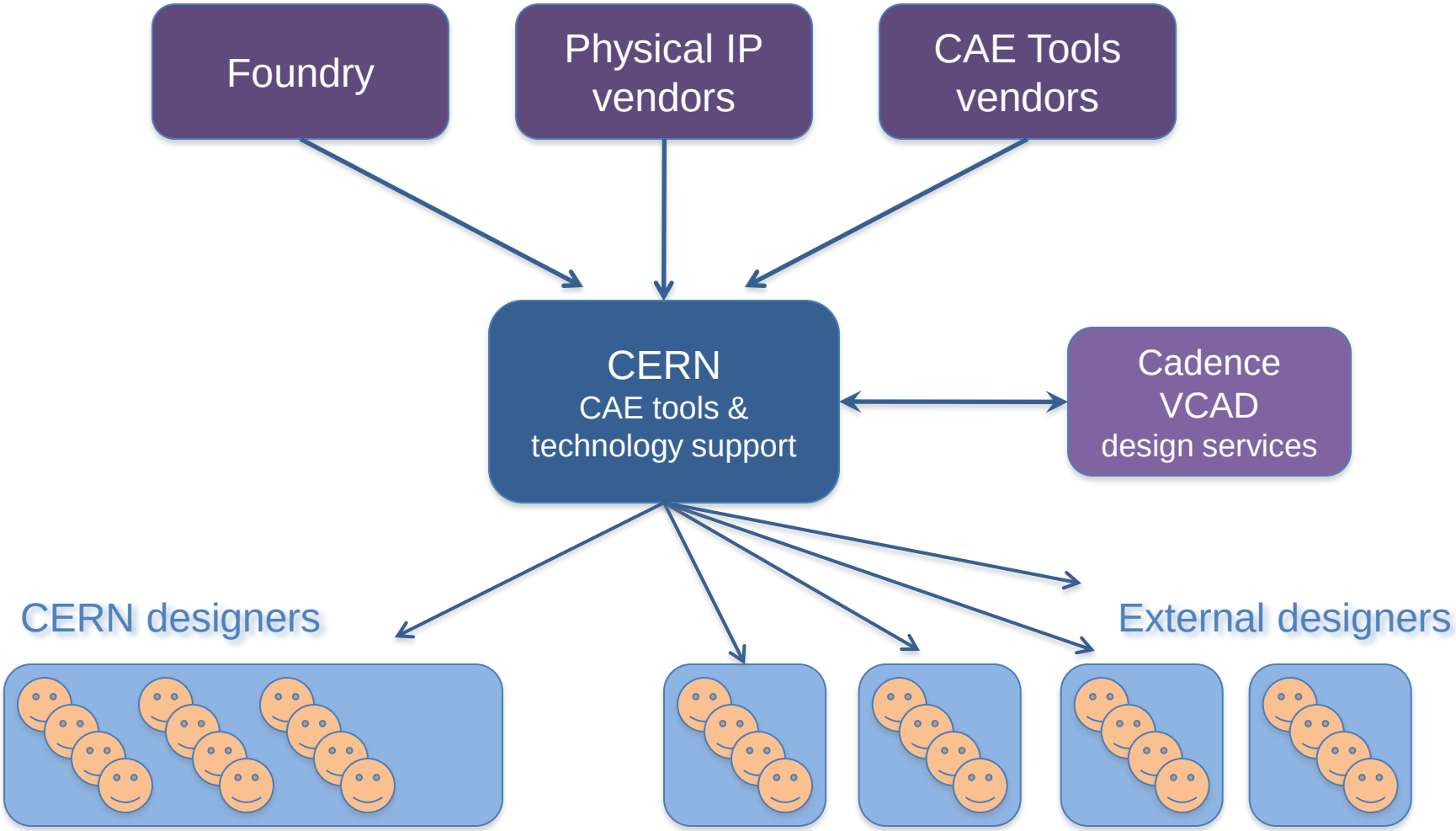
65nm Foundry Access Services



THANK YOU

One more slide →

MPW Call for Interest

- Please contact for participation to:
  - Forthcoming MPW runs:
    - **CMOS8RF (130nm)**
      - CERN MPW, February 2012 (tentative)
      - MOSIS MPW, Nov. 7, 2011
    - **CMOS6 (250nm)**
      - November 2011.
- Keep us informed for your future submission plans.
- Contact: kostas.kloukinas@cern.ch

130nm Technology Support Services