Silicon photonic devices

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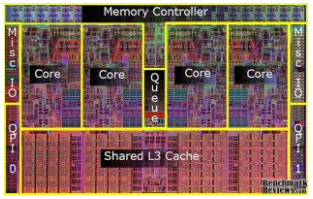
http://silicon-photonics.ief.u-psud.fr/

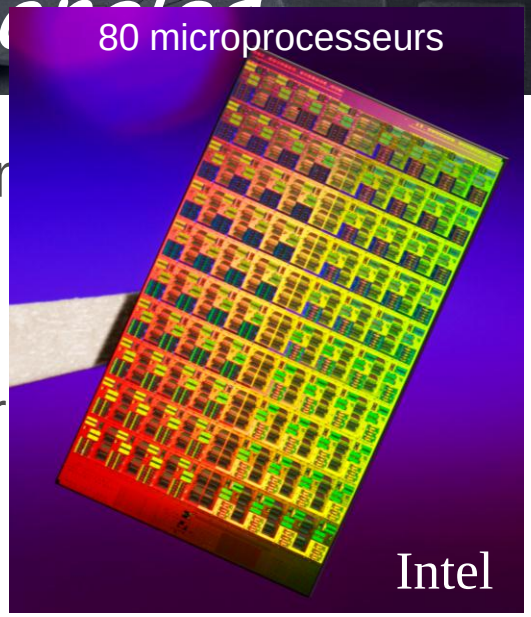
Outline

- Motivations and rationales
- Photonic and opto-electronic building blocks:
  - Passive silicon photonic integrated circuits
    - ✓ Waveguides, 90°-turns, beam splitters, photonic circuits
  - Active devices:
    - ✓ Light sources
    - ✓ Optical modulators
    - ✓ Optical detectors
- Coupling to outside world
- Possible integration schemes of optics with CMOS
- Conclusion and perspectives

Motivations and rati

- Increase of integrated circuit cor
  - Number of transistors
  - Frequency operation
  - Length and density of metallic inter





Metallic interconect limitations

- RC delay
- Signal distortion
- Power consumption

↓

Increase the number of cores

↓

But what's going on for intra and inter core communications?

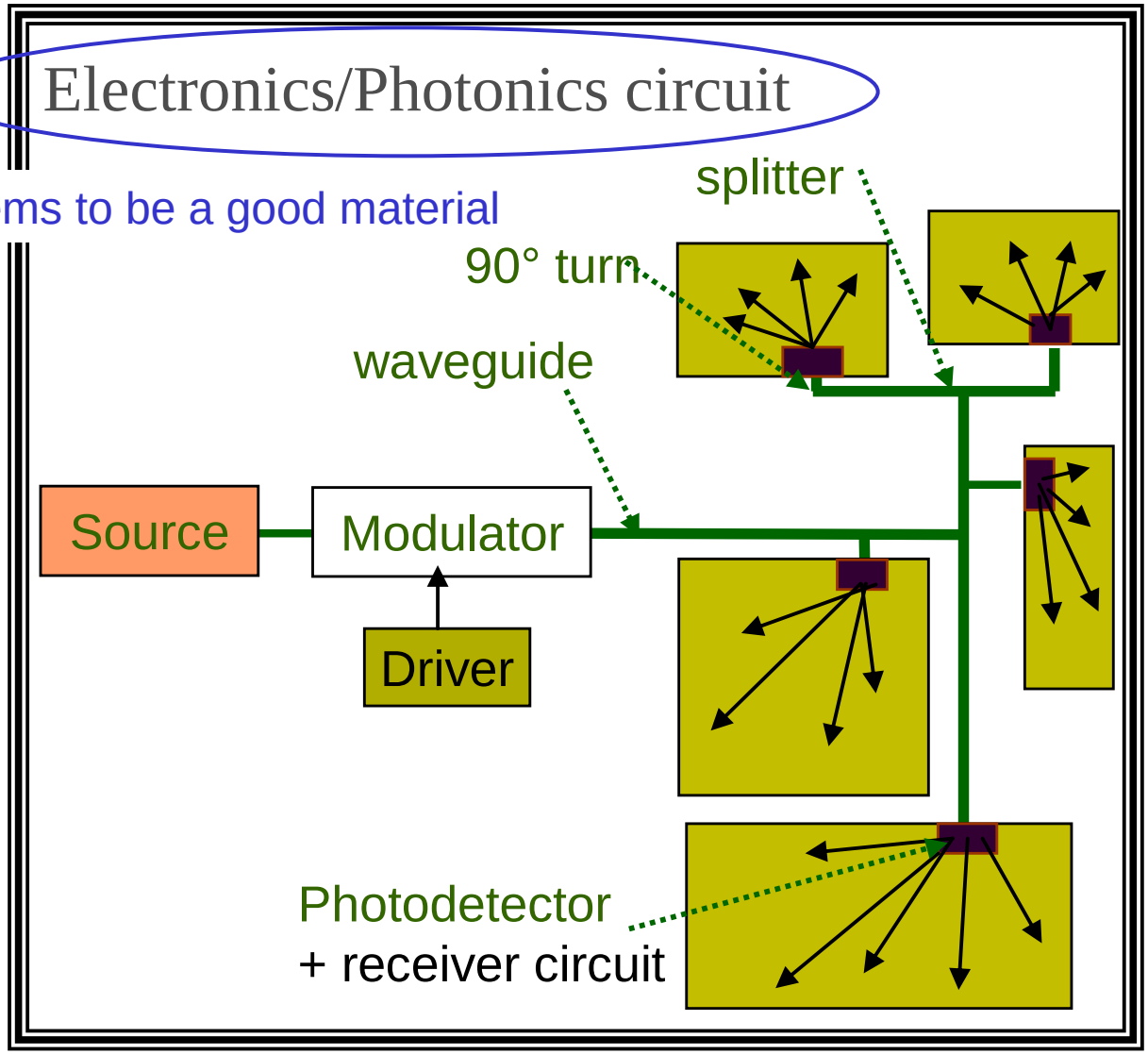
Motivations and rationales

Advantages of optics

- Negligible signal distortion even for high frequencies (>10GHz) and long distances (>1cm)
- Reduced latency, skew, and jitter
  - larger synchronous zones
  - better synchronization
- No repeaters
  - silicon area saving
  - lower power dissipation
  - reduced complexity
- Noise immunity
- Voltage insulation

Motivations and rationales

Optical interconnects

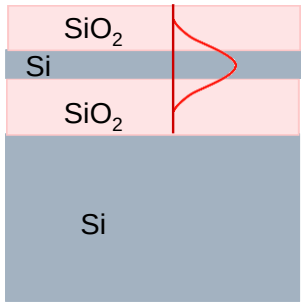


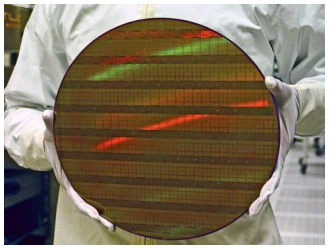
Motivations and rationales

Silicon Pro's and Cons

- Transparent in 1.3-1.6 µm region
- Take advantage of CMOS platform
  - Mature technology
  - High production volume
- Low cost
- Silicon On Insulator (SOI) wafer
  - Natural optical waveguide
- High-index contrast (n_{Si}=3.5 – n_{SiO2}=1.5)
  - Strong light confinement
    - ✓ Small footprint (Sub-micron area)
- Electronic/photonic integration

- Indirect bandgap material
  - No electro-optic effect
  - Lacks efficient light emission
- No detection in 1.3-1.6 µm region
- High-index contrast for coupling

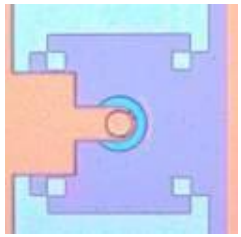


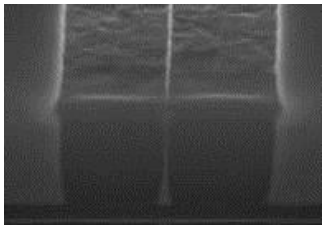


Strong interest for silicon photonics in the recent years

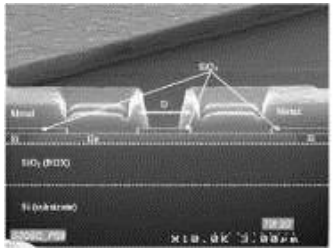
Motivations and rationales

Hybrid CMOS chip merging optics and electronics??



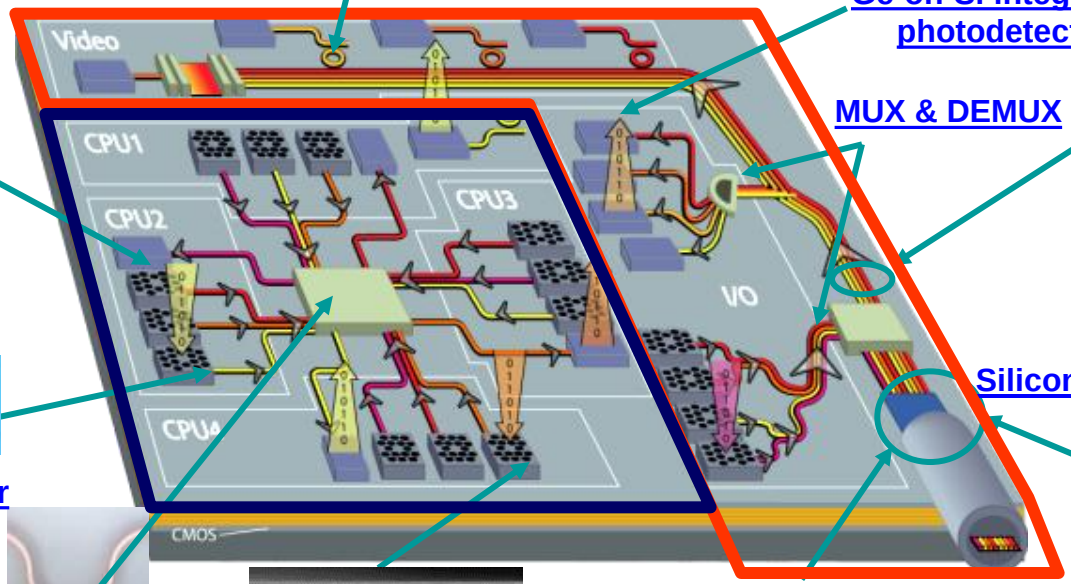


Slot waveguide for NL operation

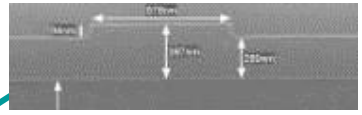


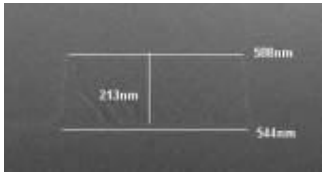
Ge-on-Si integrated photodetector

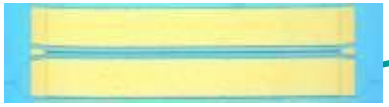
InP-on-Si integrated laser



MUX & DEMUX



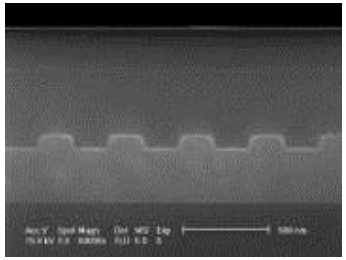




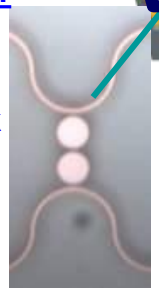
Silicon optical modulator

Silicon-On-Insulator waveguide

Grating coupler



ONoC
Optical Network On Chip



Inverted taper

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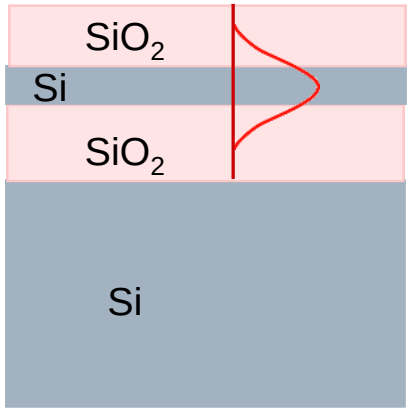
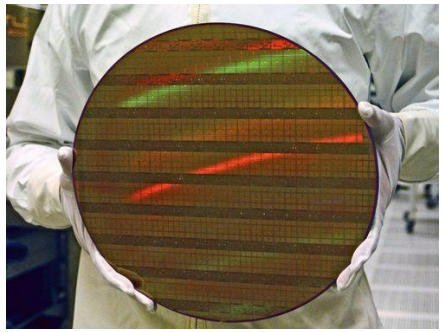
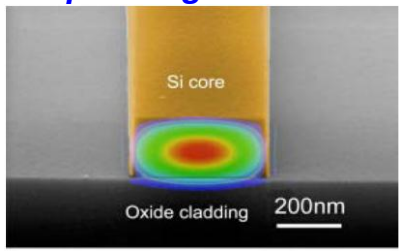
SOI microwaveguides: the basic device





SOI wafer = Optical planar waveguide

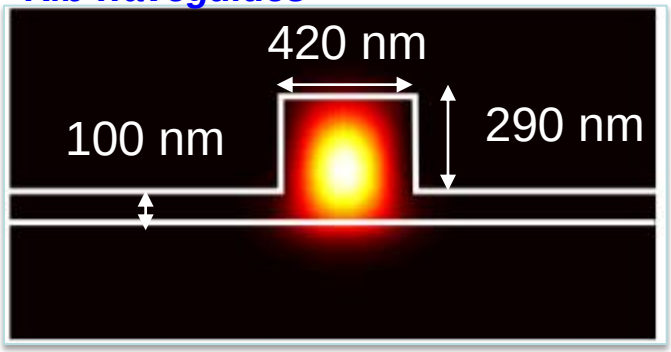
Strip waveguides



Mode size ~0.1µm²

Propagation loss ~1dB/cm

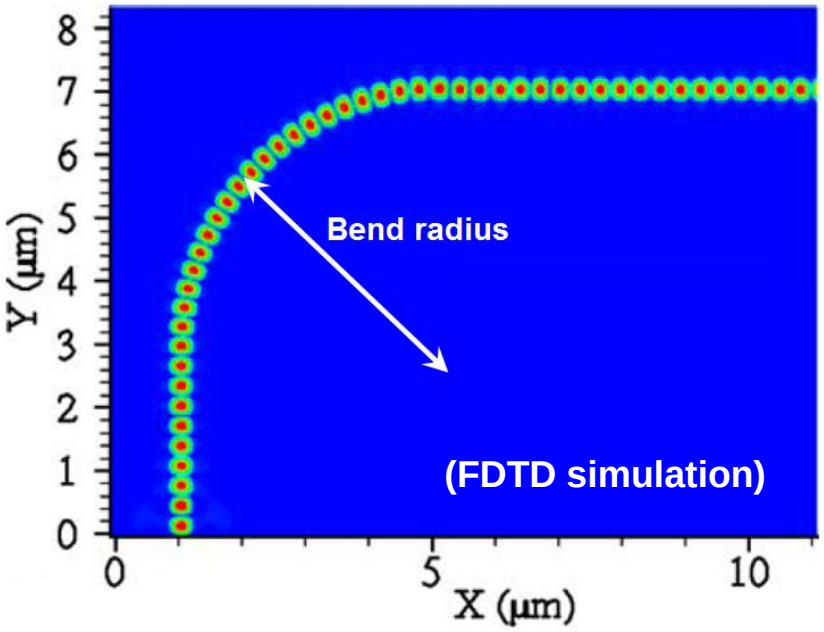
Rib waveguides



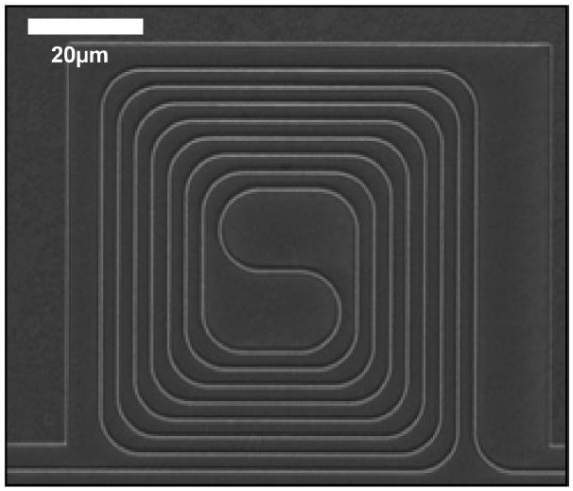
Mode size ~0.2µm²
Propagation loss ~0.2dB/cm

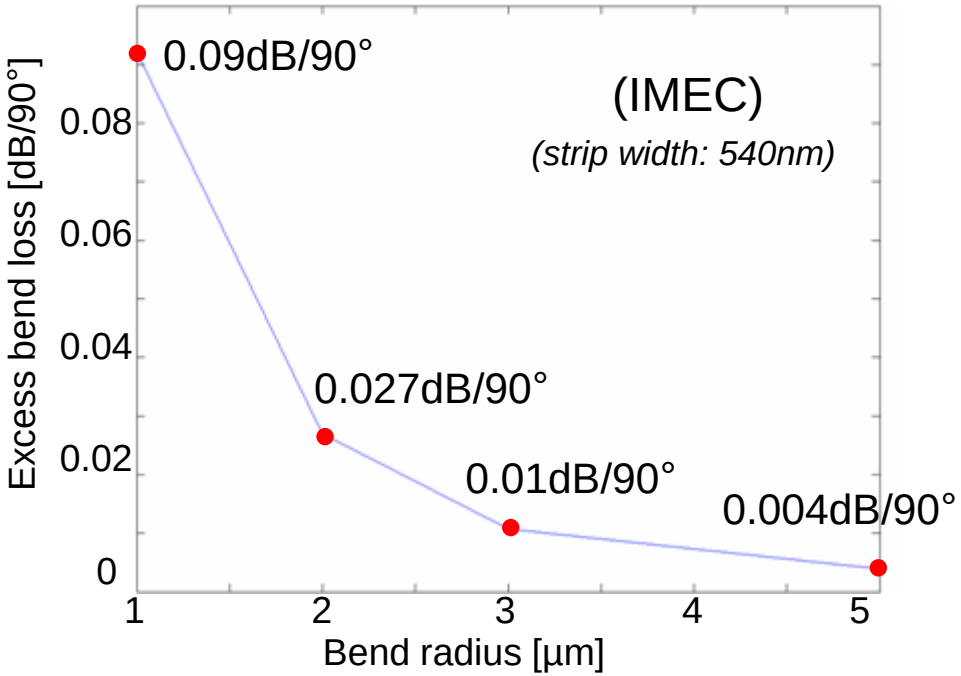
λ=1.55µm

Light bending using strip wgs



Testing device:

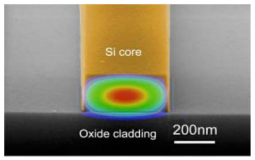




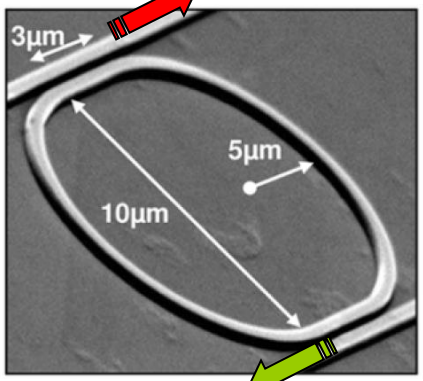
- Increase for narrower waveguides:
  - Weaker confinement: bend radiation
  - More sensitive to roughness
- Increase for smaller bend radii

Other devices for light distribution:

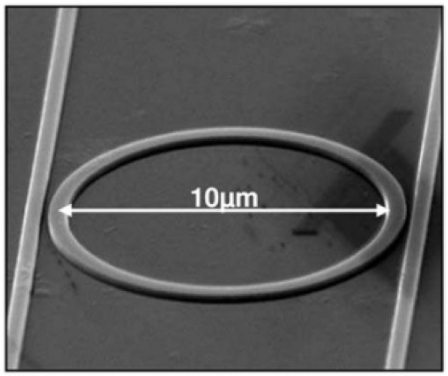
Strip waveguides



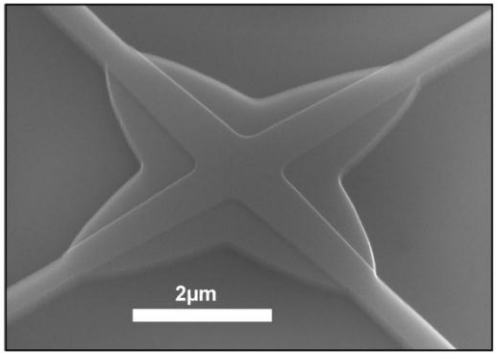
Off-resonance



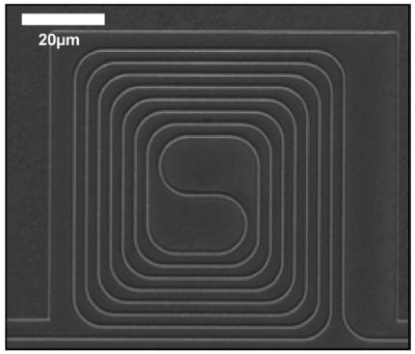
On-resonance



Integrated wavelength filter

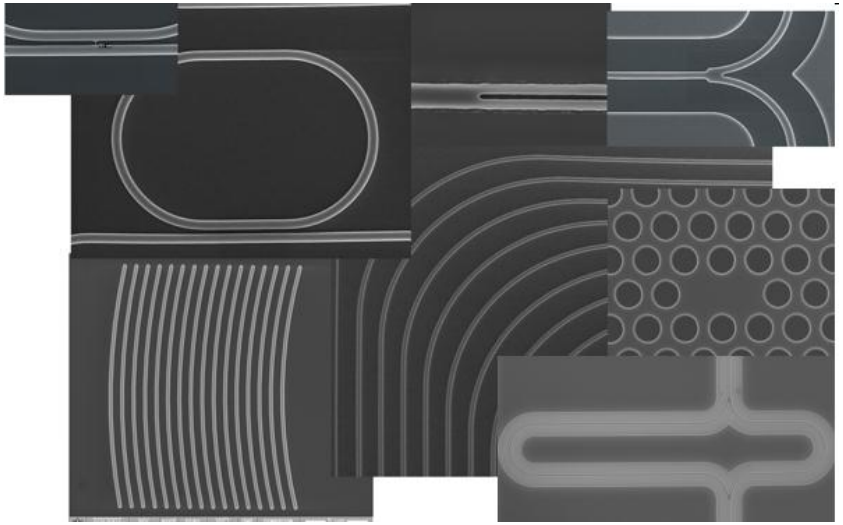


Low-loss crossing



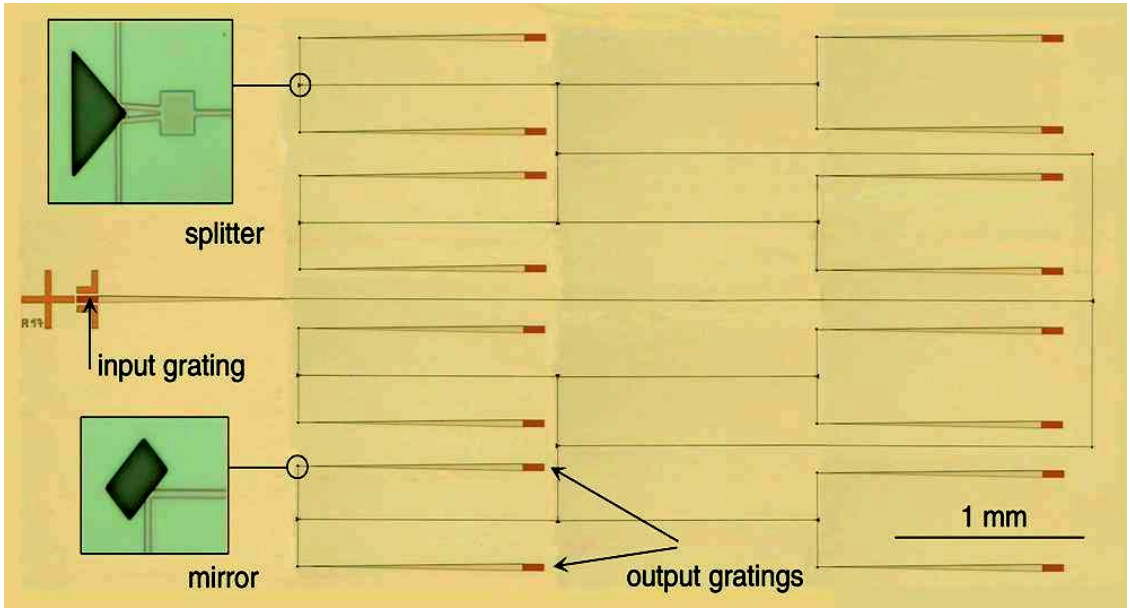
Spiral waveguide

and so on …

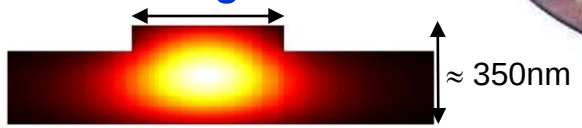


Results from Ghent Univ. (Belgium)

Other devices for light distribution:

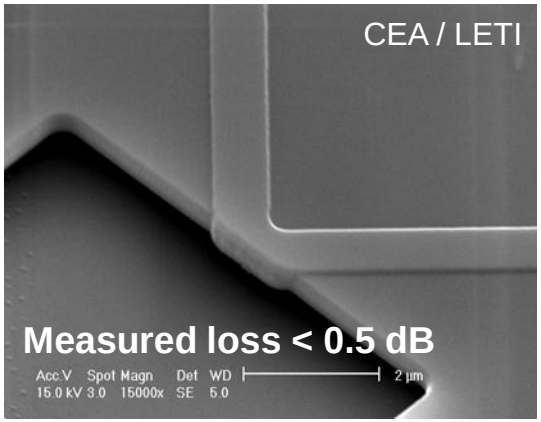


Rib waveguides

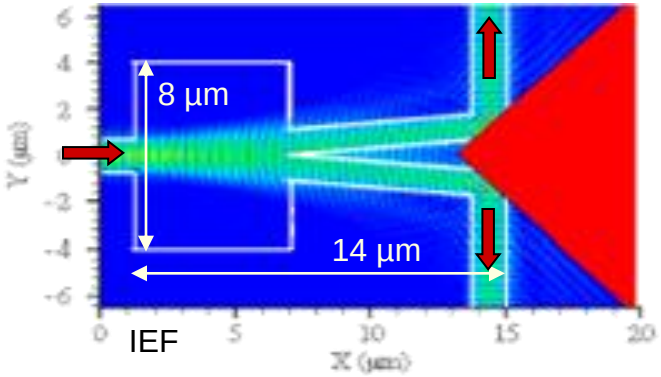


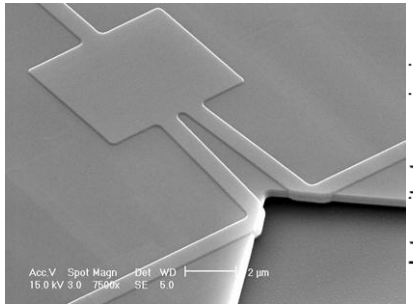
S. Lardenois et al. Optics Letters 28, 1150-1152 (2003)

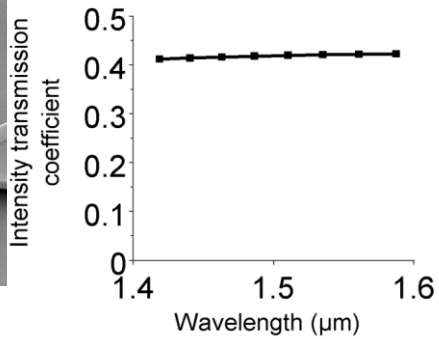
90°-turns:



Compact star couplers:

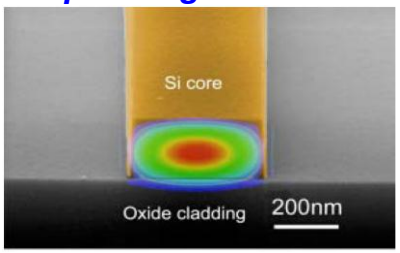






Other devices for light distribution: conclusion

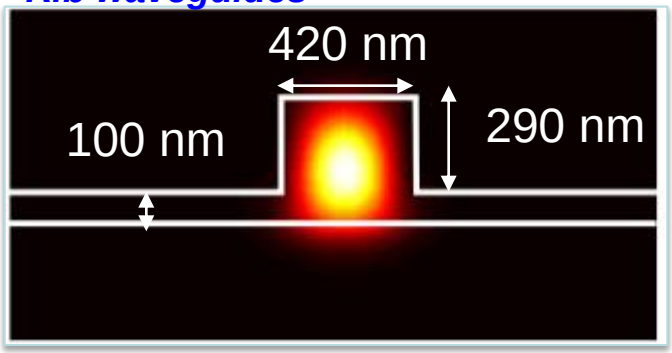
Strip waveguides



Mode size ~0.1µm²

Propagation loss ~1dB/cm

Rib waveguides



Mode size ~0.2µm²
Propagation loss ~0.2dB/cm

Almost arbitrary optical paths and passive functions within SOI photonics

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Overview of the optical source issue

Indirect bandgap of silicon make the source issue difficult!

Two main strategies:

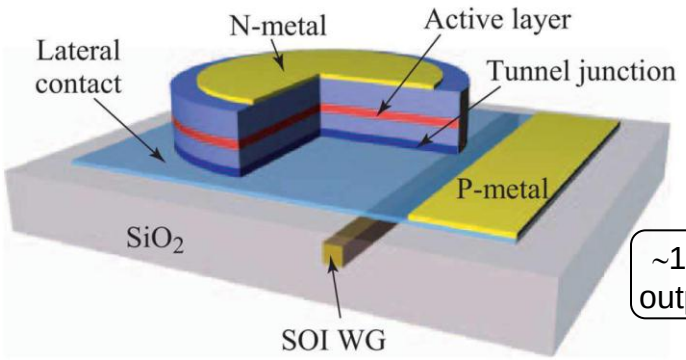
- use **III/V laser diodes on silicon**
- develop **silicon compatible optical sources using group-IV materials** (e.g. Ge rich materials)

Questions to be adressed:

- **Integration of optical sources on silicon**: device bonding, wafer bonding, heteroepitaxial groth, heterogenous integration, …:
  - ➢ several possible strategies with advantages and drawbacks: easiness, cost, thermal budget management
  - ➢ injection optical waveguides: coupling issue (tolerances and misalignments, efficiency due to compatibility between optical modes)

Some proposed strategies for III/V source on Si:

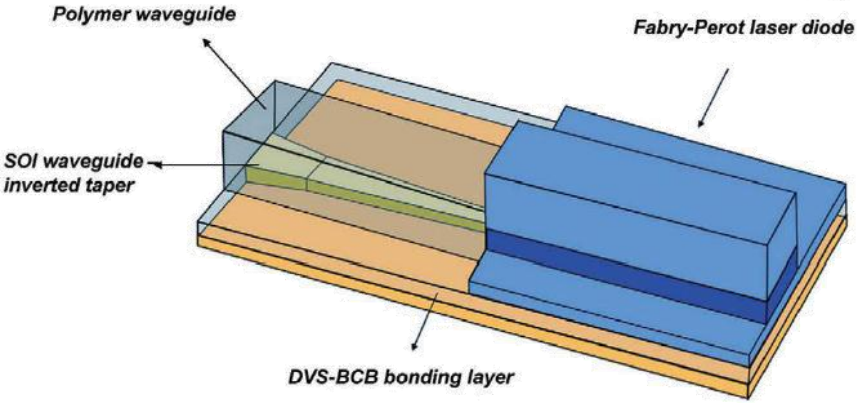
Micro-disk lasers



~10-100 µW output powers

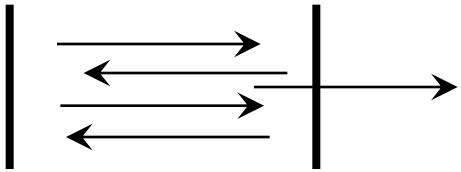
- InP-based micro-disk lasers
- Die-to-wafer molecular bonding

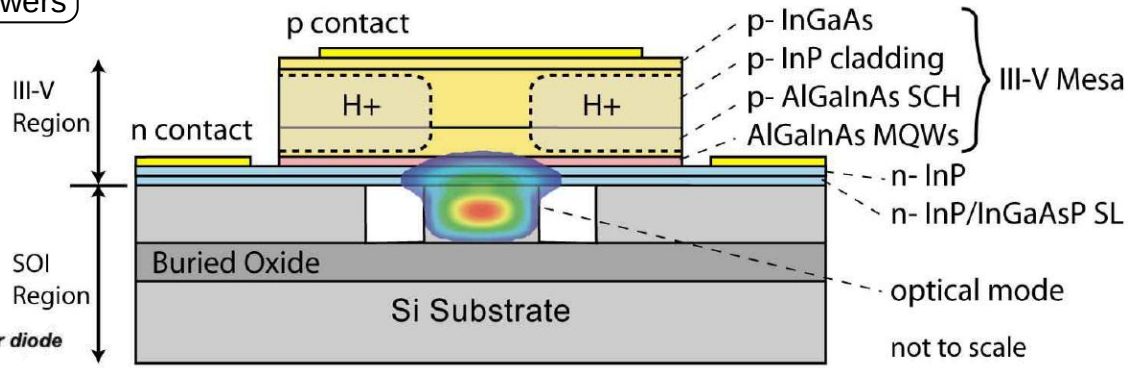
J. V. Campenhout et al. IEEE Photonics Techn. Letters **20**, 1345-1347 (2008).



Tapering stage to match the wg mode profiles

Fabry-Perot lasers





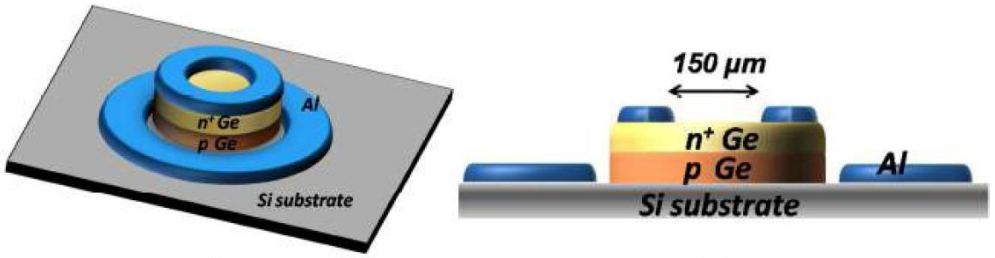
D. Liang et al., Optics Express 17, 20355-20364 (2009).

~1-10 mW output powers

- strong confinement of SOI waveguides
- optical amplification in the III/V layer

Electroluminescence properties of Germanim-rich materials (Ge/Si, GeSi quantum wells)

Aim: monolithic integration of optical source within CMOS



J. Liu et al., « Direct-gap optical gain of Ge on Si at room temperature », Optics Letters **34**, 1738-1740 (2009).

J. Liu et al., « Ge-on-Si laser operating at room temperature », Optics Letters **35**, 679-681 (2010).

can be exploited

Rapid progress in this field
=> Ge-on-Si optical source likely to appear in a near future

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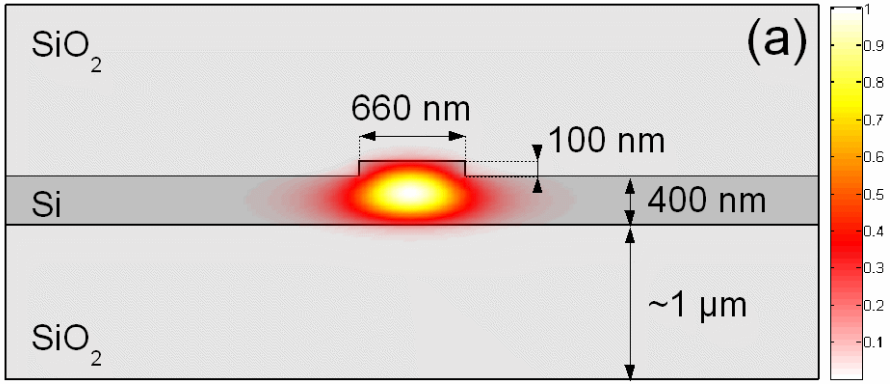
Optical modulation within CMOS photonics?

Modulating the free carrier concentrations:

$$\Delta n = -8{,}8.10^{-22}\,\Delta N - 8{,}5.10^{-18}\,\Delta P^{0,8}$$

$$\Delta \alpha = 8{,}5.10^{-18}\,\Delta N + 6{,}0.10^{-18}\,\Delta P$$

at λ=1.55µm



example:

Electro-refraction by free carrier concentration variations in silicon:

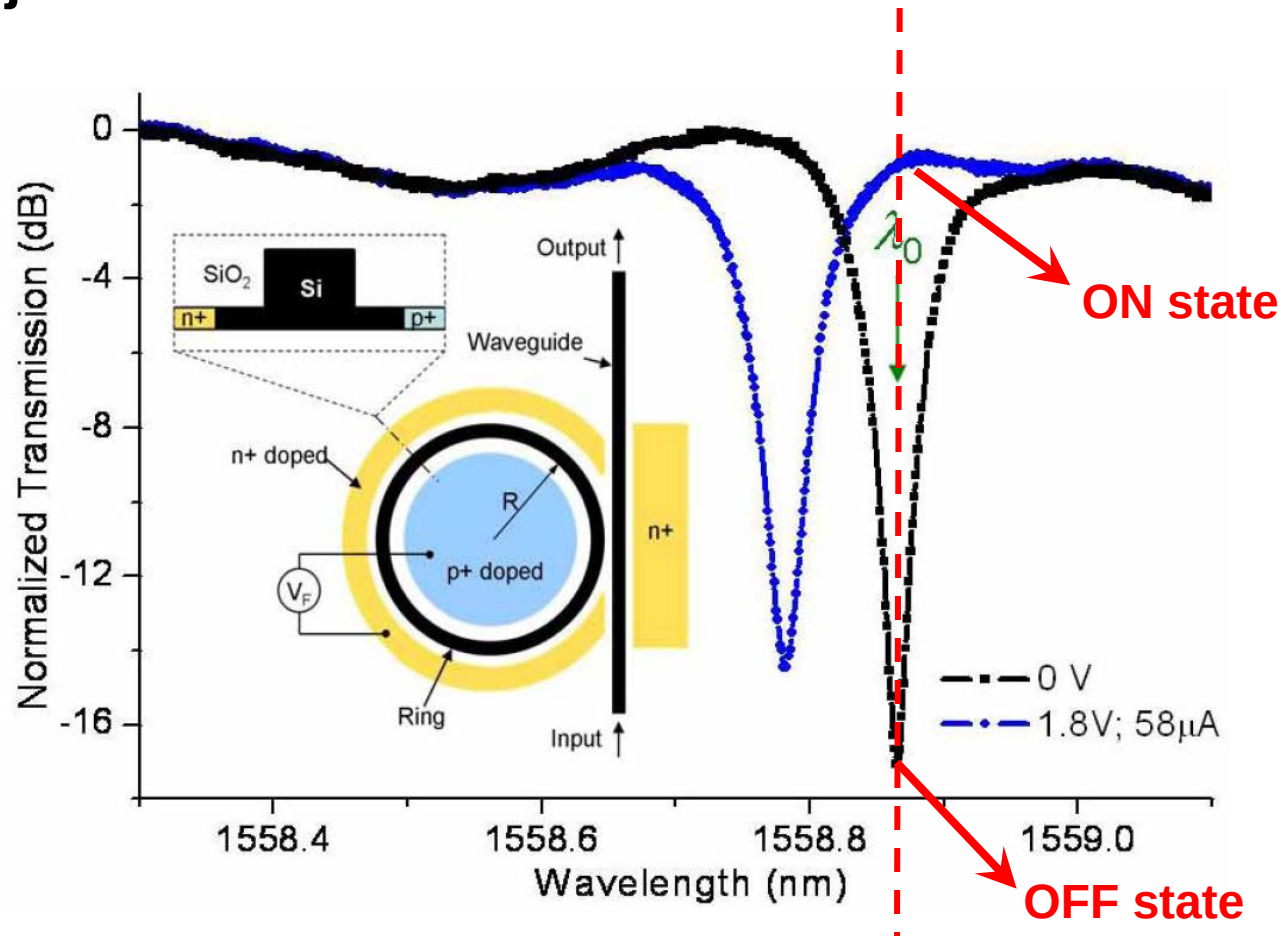
- Accumulation
- Injection
- Depletion

MOS capacitances

PN, PIN, PIPIN junctions

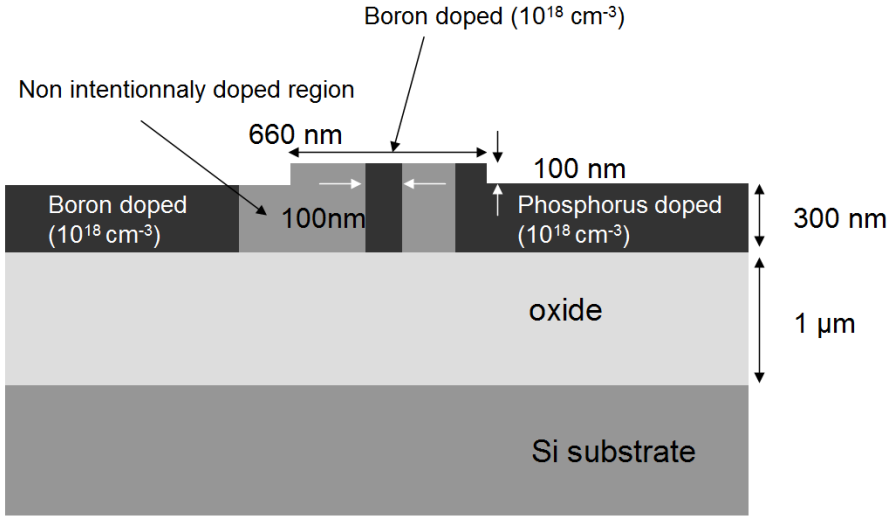
Active devices: optical modulators

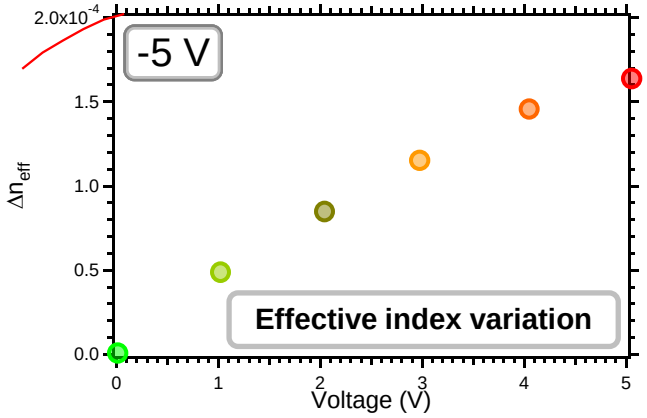
Carrier injection

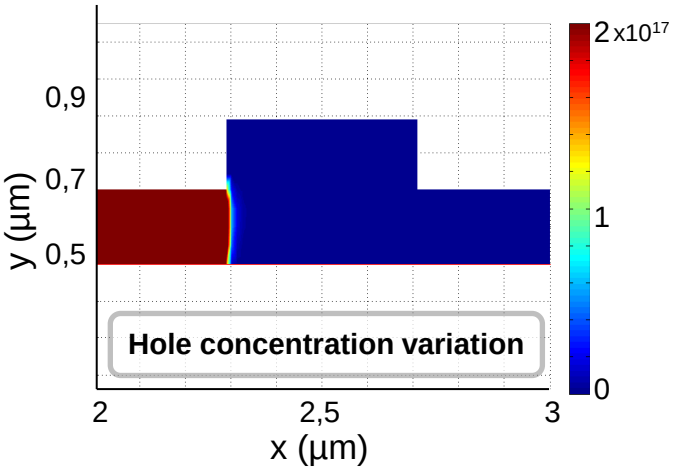


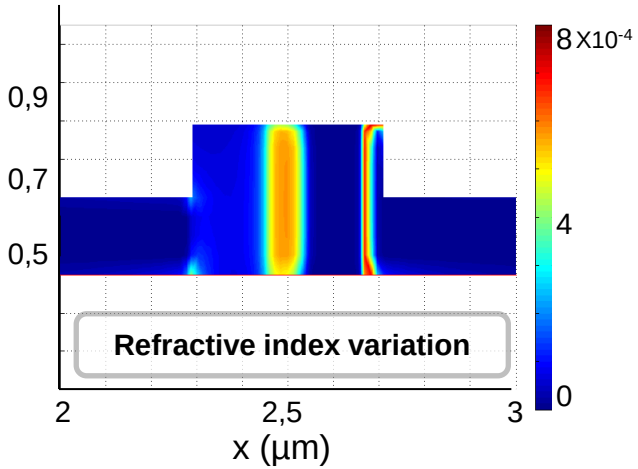
Q. Xu et al., Optics Express **15**, 430-436 (2007).

Carrier depletion

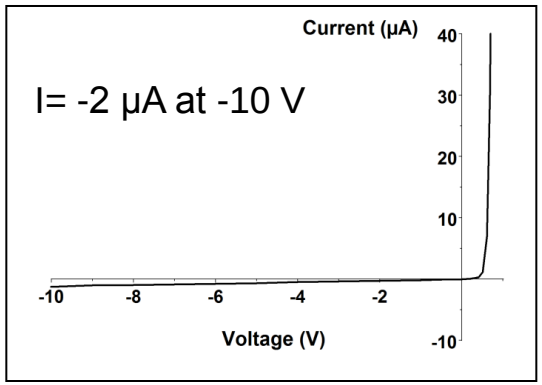


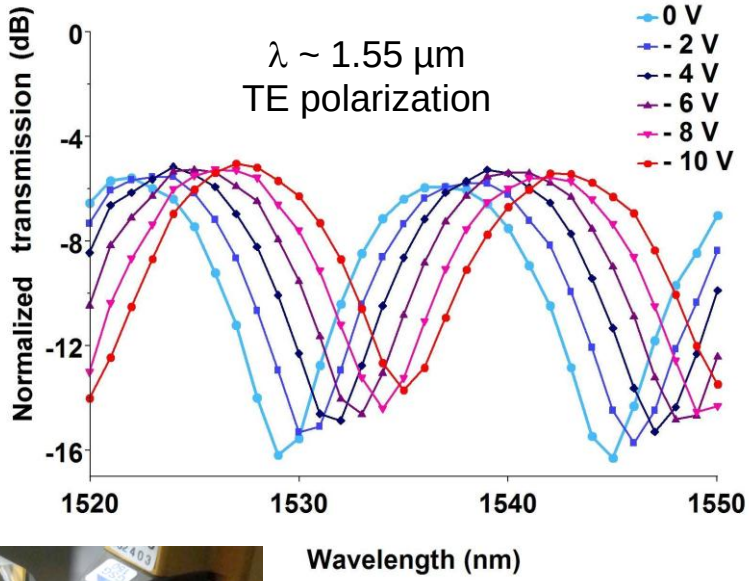






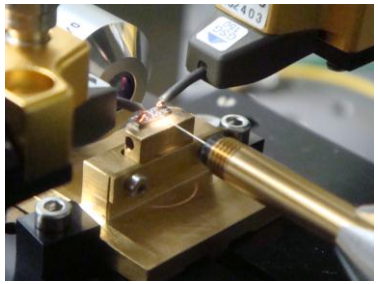
Carrier depletion

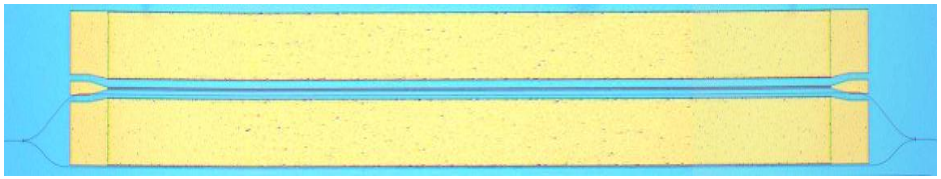




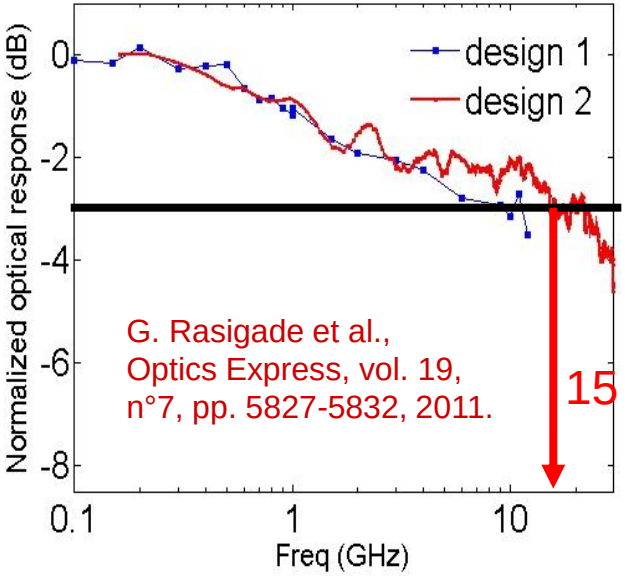
DC experimental results :

- ❑ Insertion loss = 5 dB
- ❑ Contrast ratio up to 14 dB
- ❑ $V_\pi L_\pi$ = 5 V.cm

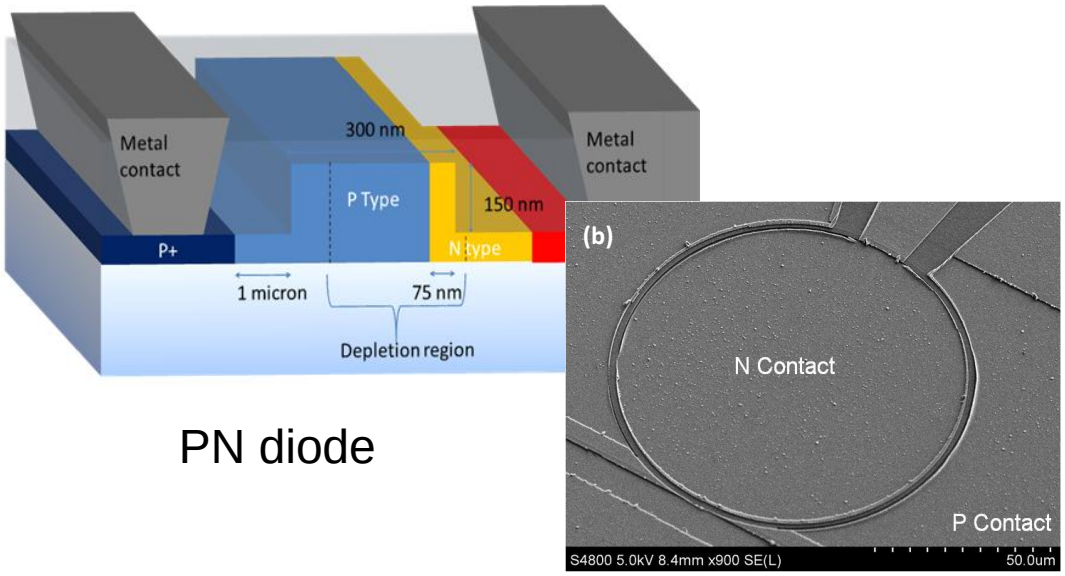




Mach-Zehnder interferometer



Carrier depletion



PN diode

F. Gardes et al, Optics Express, 17 (24) (2009).

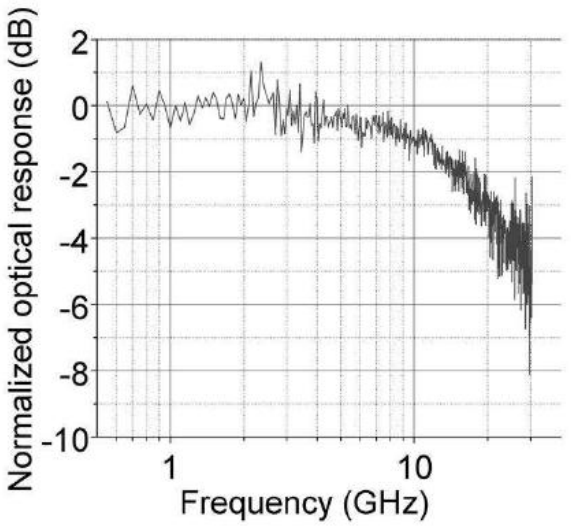


Fig. 4. Normalized optical response as a function of frequency.

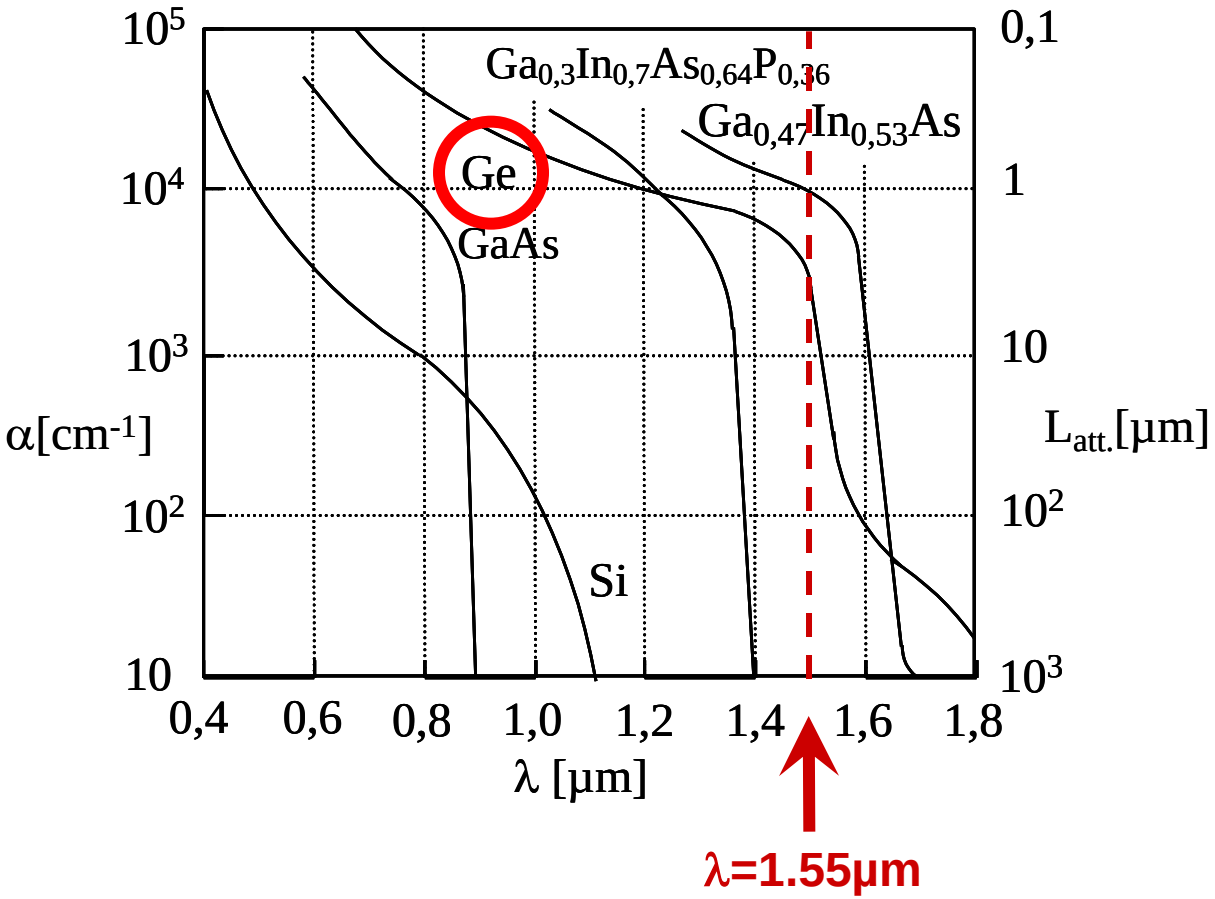
19 GHz small-signal bandwidth

Outline

- Motivations and rationales
- Photonic and opto-electronic building blocks:
  - Passive silicon photonic integrated circuits
    - ✓ Waveguides, 90°-turns, beam splitters, photonic circuits
  - Active devices:
    - ✓ Light sources
    - ✓ Optical modulators
    - ✓ Optical detectors
- Coupling to outside world
- Possible integration schemes of optics with CMOS
- Conclusion and perspectives

Active devices: detectors

A material is needed for light absorption around λ=1.55µm



Active devices: detectors

- Strong absorption:

  √ $\alpha \approx 9000\ cm^{-1}$ at λ=1.3 µm
  ⇒ $L_{ABS}^{95\%} \approx 3.3$ µm
  ⇒ Low capacitance devices
  ⇒ High frequency operation

- High carrier mobilities

- Lattice misfit with Si of about 4.2%

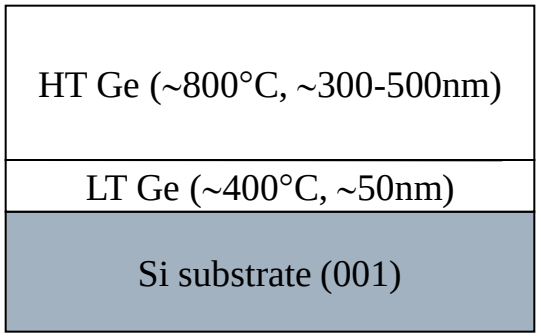
  ⇒ Specific growth strategies required

- 2-step Ge growth on Si
  ⇒ annealing to reduce threading dislocations

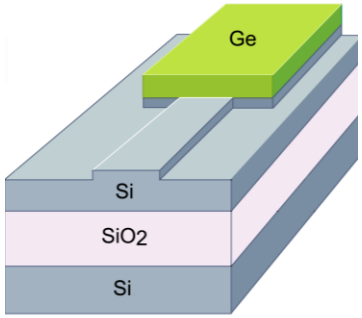
Germanium photodetectors

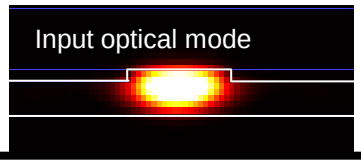
UHV-CVD (IEF) *RP-CVD (LETI)*

M. Halbwax & al., Optical Materials **27**, 822-826 (2005)
J. M. Hartmann & al., J. Appl. Phys. **95**, 5905-5907 (2004)



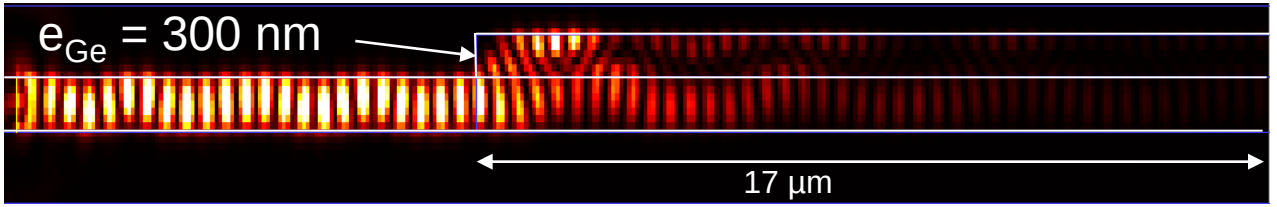
Active devices: detectors



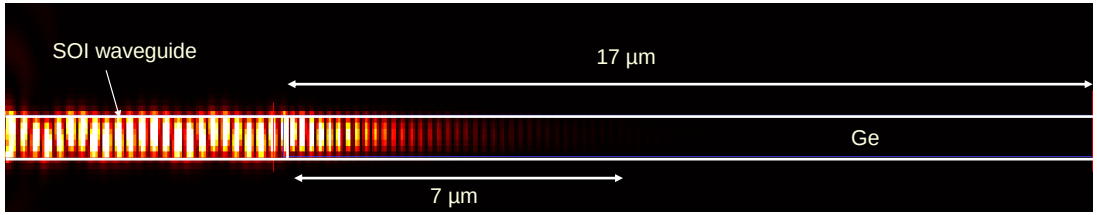


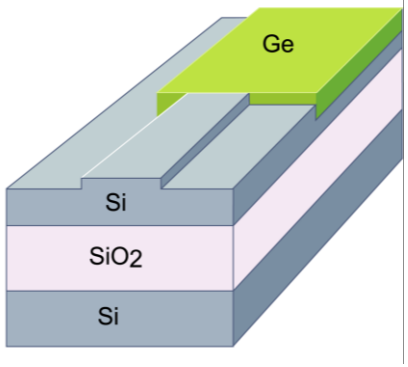
Waveguide height: 380 nm
Waveguide width: 700 nm
Etching depth: 110 nm

Vertical coupling



Butt coupling

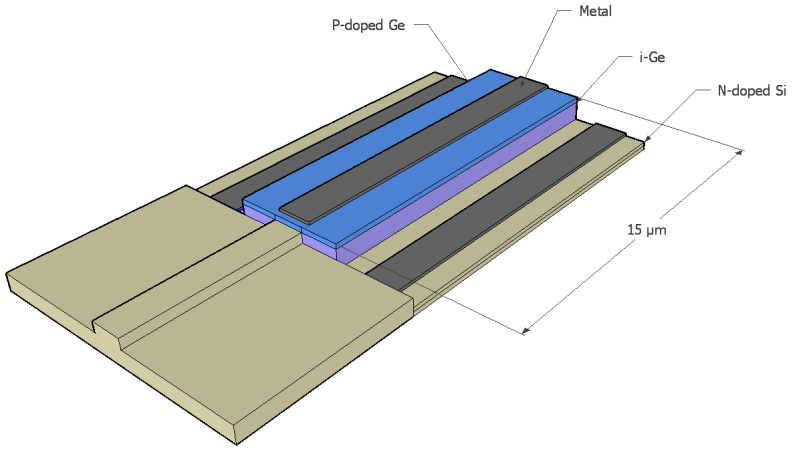




⇨ Shorter absorption length (few microns)
⇨ Light absorption is independent of Ge film thickness
(if Ge layer is thick enough: >350 nm)

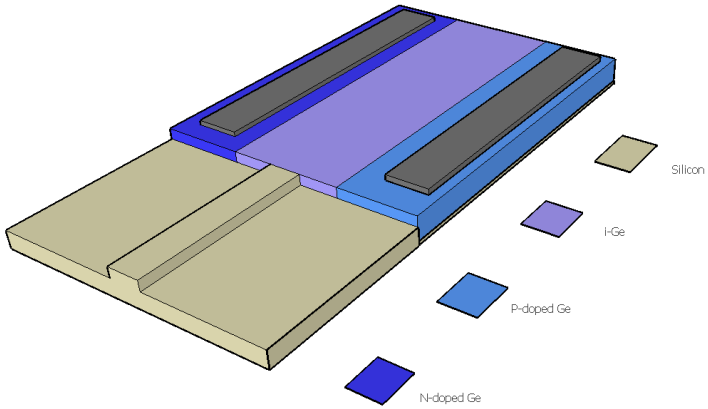
Active devices: detectors

Vertical diode



- √ 3 µm wide mesa
- √ **i-Ge thickness:** ~300 nm
- √ **Ge length:** 15 µm

Lateral diode

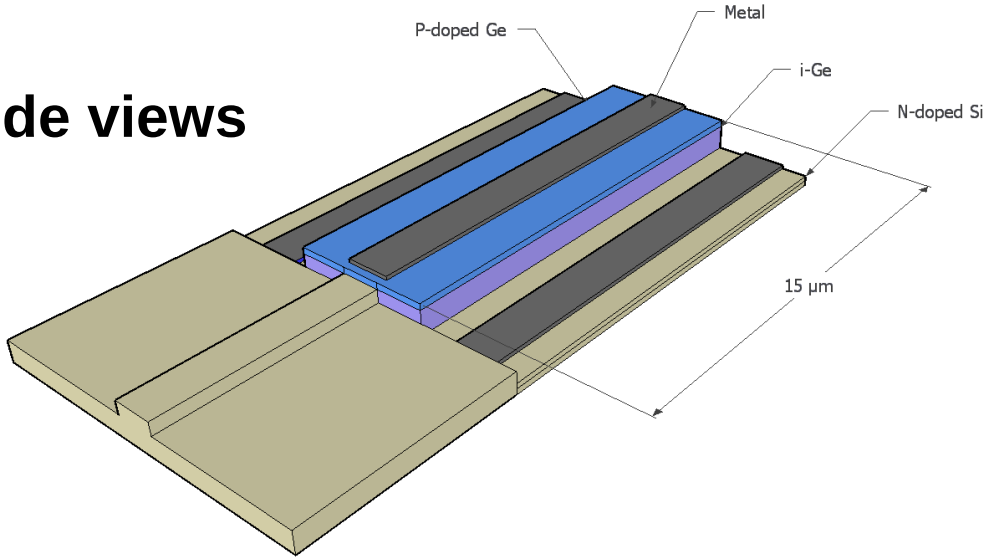


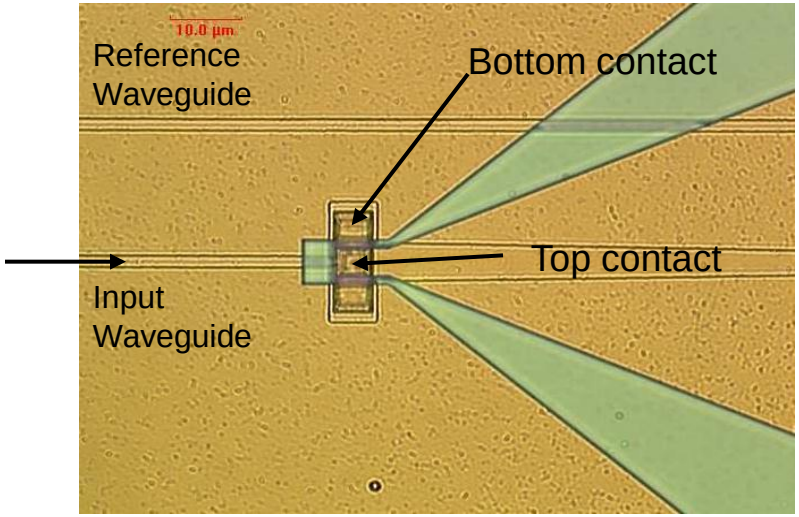
- √ **i-Ge width:** from 1 µm to 0.5 µm
- √ **Ge length:** 10 µm

Both Ge PIN diodes theoretically lead to
low dark current, high responsivity and high bandwidth

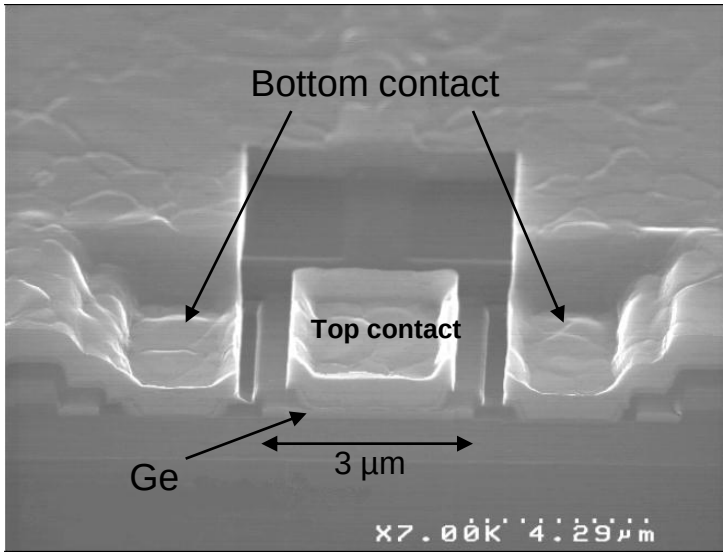
Active devices: detectors

Vertical pin diode views





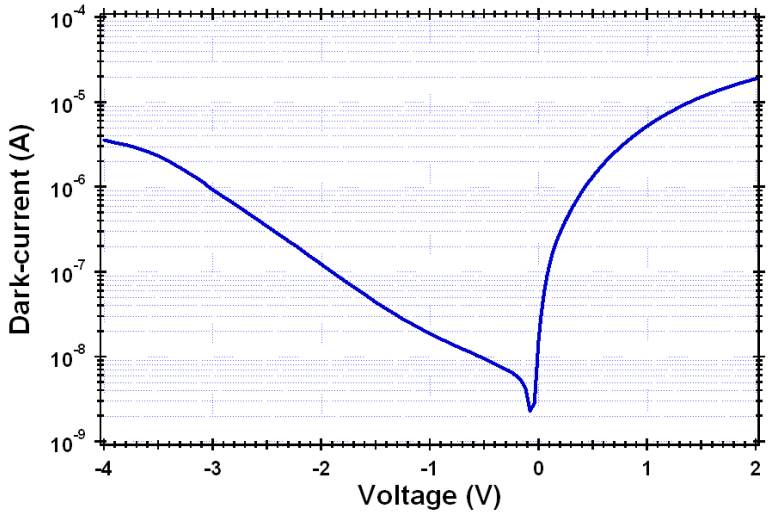
Top view



Side view

Active devices: detectors

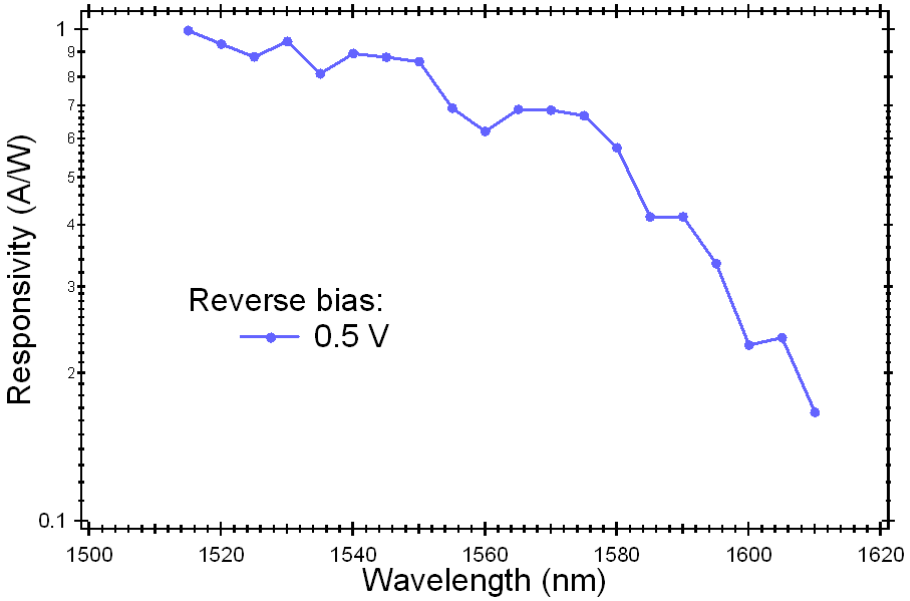
Vertical diode: DC characteristics



- 18 nA dark current at 1V reverse bias

⇒ Dark current density: 60 mA/cm²

- $C_{measured}$ ~ 12 fF



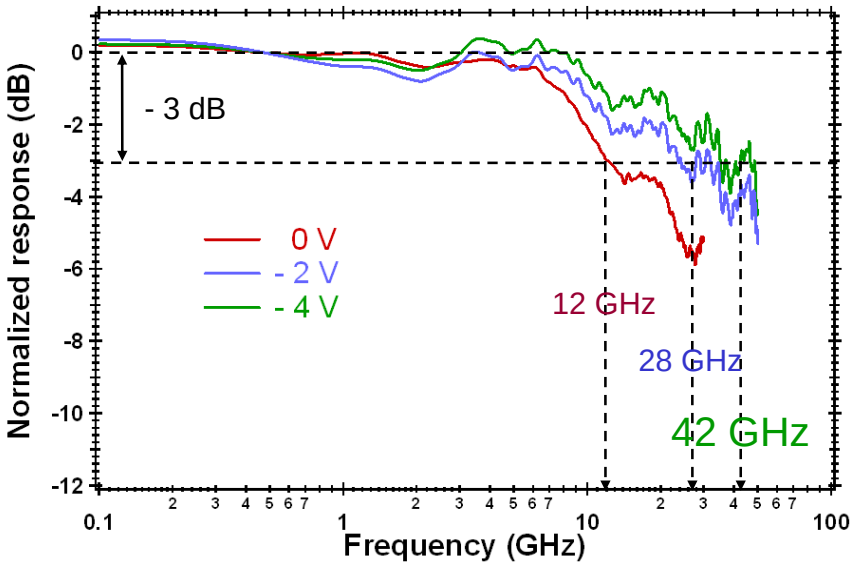
- **Under -0.5 V:**

  ⇒ **~ 1 A/W at 1520 nm**

  ⇒ ~ 0.2 A/W at 1600 nm

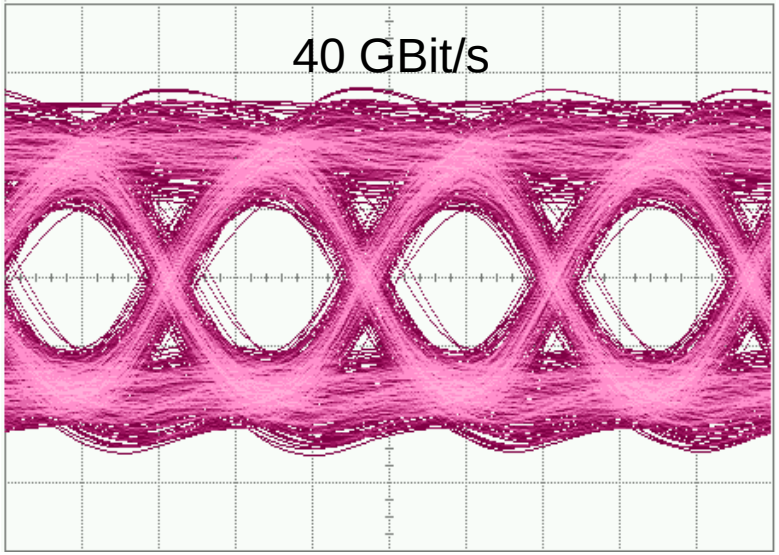
Active devices: detectors

Vertical diode: RF characteristics



- -3 dB bandwidth:
  - √ 12 GHz at 0 V
  - √ ~30 GHZ at -2 V
  - √ > 40 GHz at -4 V

- Data transmission:
  - √ 40 GBit/s at -4 V



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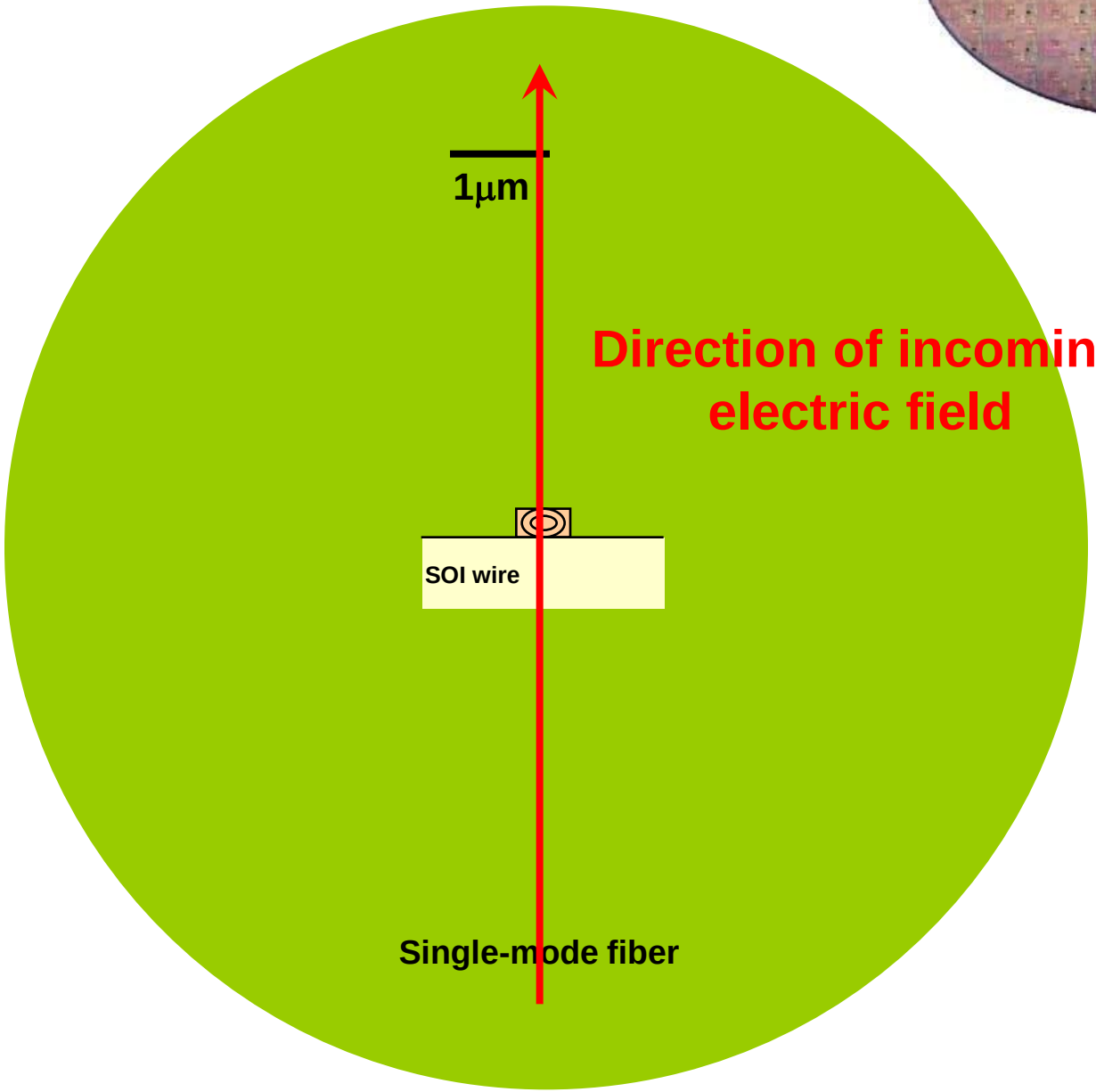
    - ➢ Optical detectors
- Coupling to outside world
- Possible integration schemes of optics with CMOS
- Conclusion and perspectives

Coupling to outside world

The waveguide mode mismatch

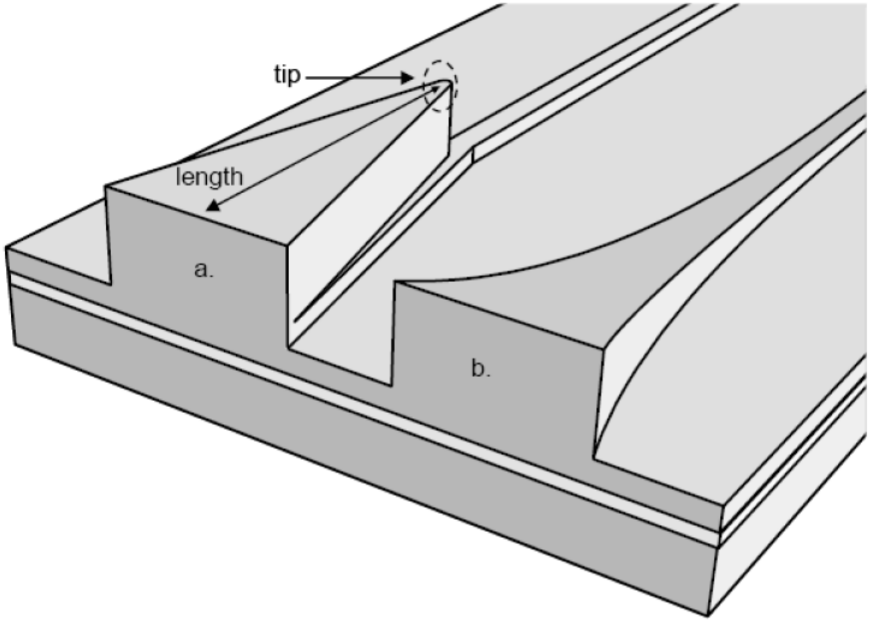
…

… and the light polarization issue.



Coupling to outside world

3D adiabatic taper

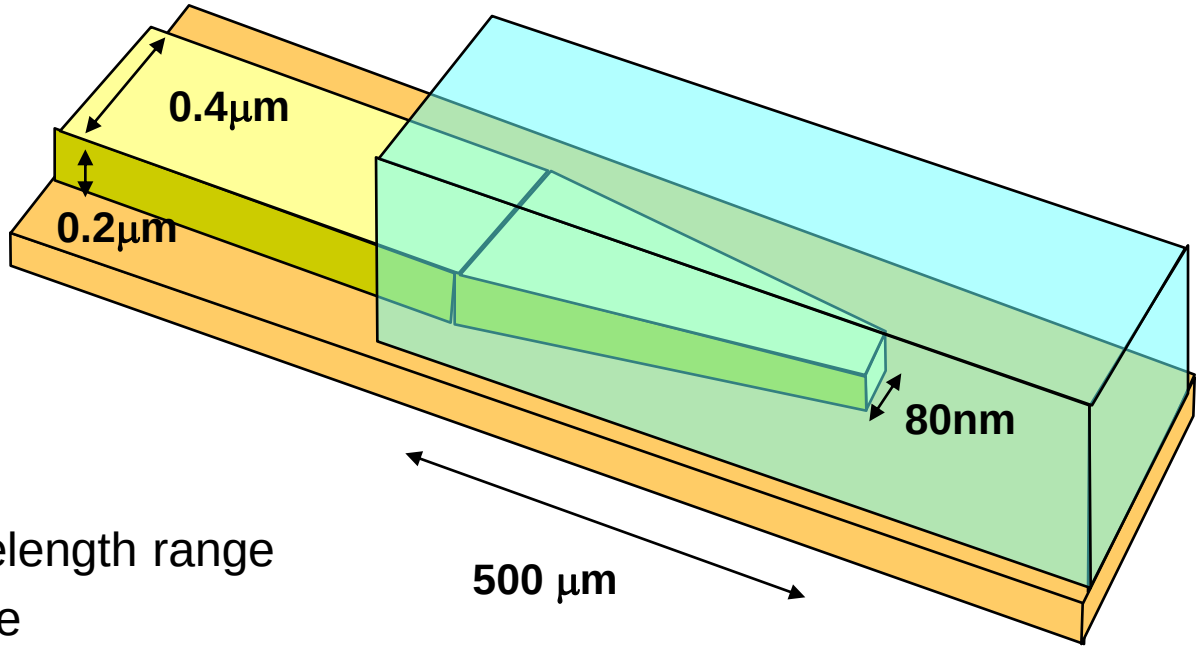


- Thick silicon layer required (~10µm)
- Multilevel grey scale lithography required
- Manual polishinh a the edge
- Antireflection coating is necessary

The most obvious idea is not the best one.

Coupling to outside world

Inverse taper



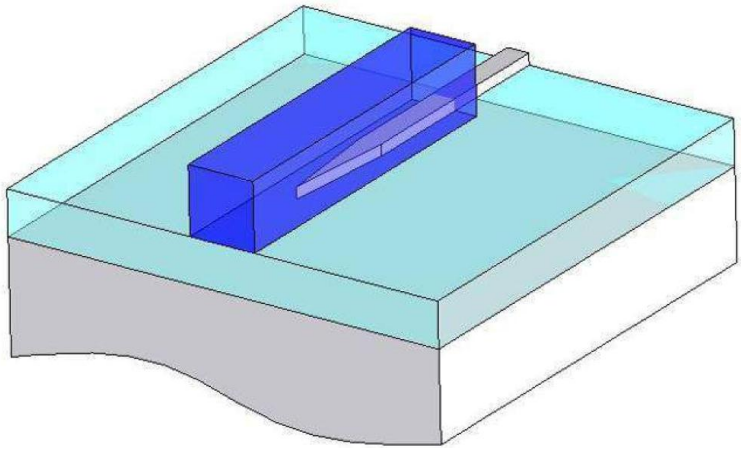
polished facet

- Broad wavelength range
- Single mode
- Easy to fabricate (if you can do the tips)
- Low facet reflections

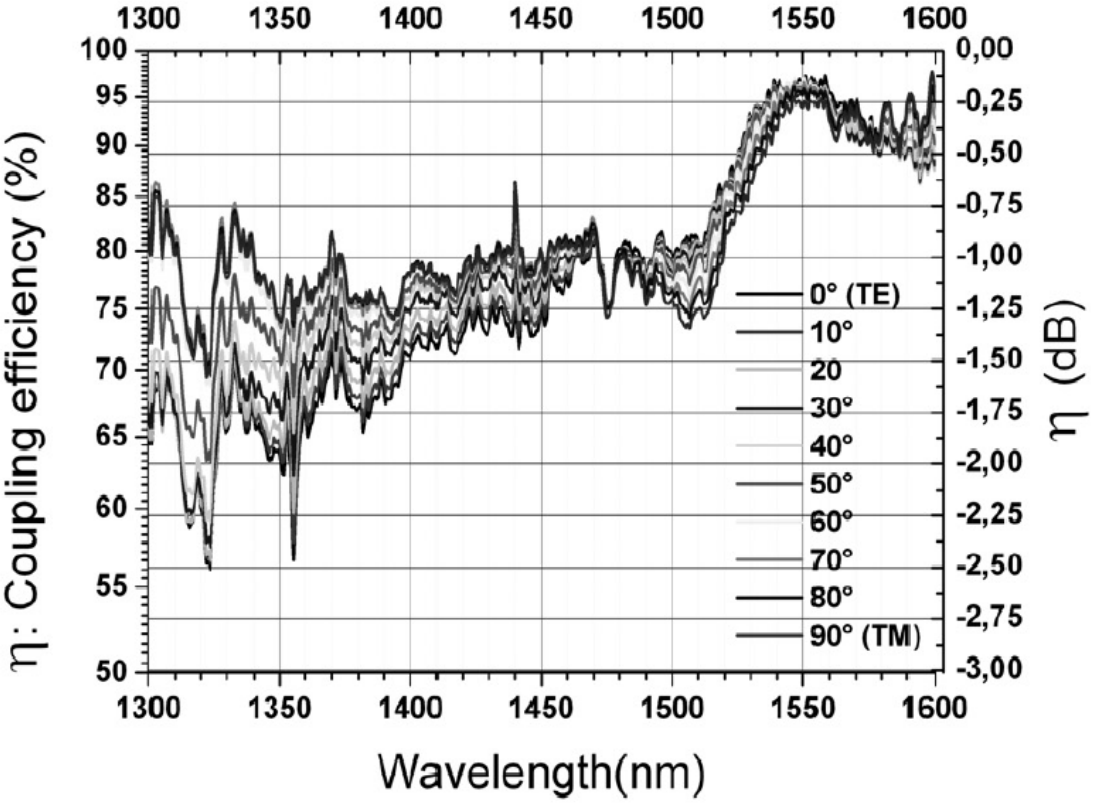
Group	h [nm]	W [nm]	L [um]	tip width [nm]	Cladding Material	Cladding Size	Loss
IBM	**220**	**445**	**150.0**	**75.0**	**Polymer**	**2x2**	**< 1dB**
Cornell	**270**	**470**	**40.0**	**100.0**	**SiO_2**	**2x00**	**< 4dB**
NTT	**300**	**300**	**200.0**	**60.0**	**Polymer/ Si_3N_4**	**3x3**	**0.8**

Coupling to outside world

Improved design allows the fabrication of high-efficiency and polarization-insensitive inversed tapers:



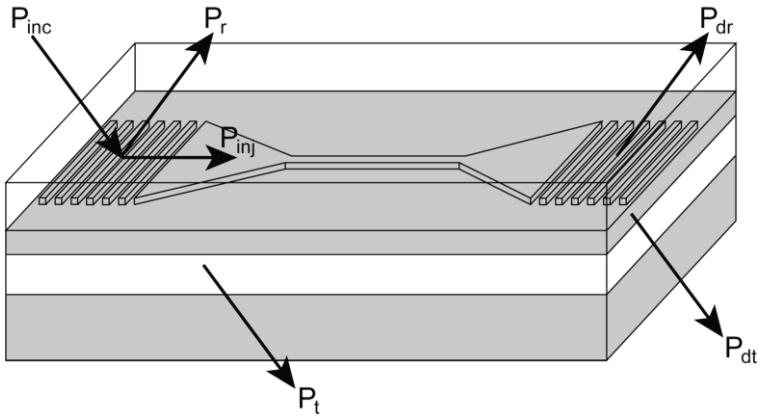
CEA-LETI

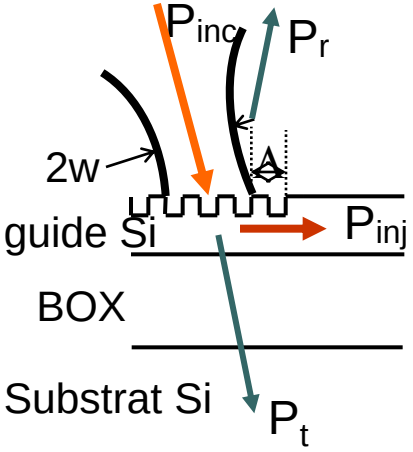


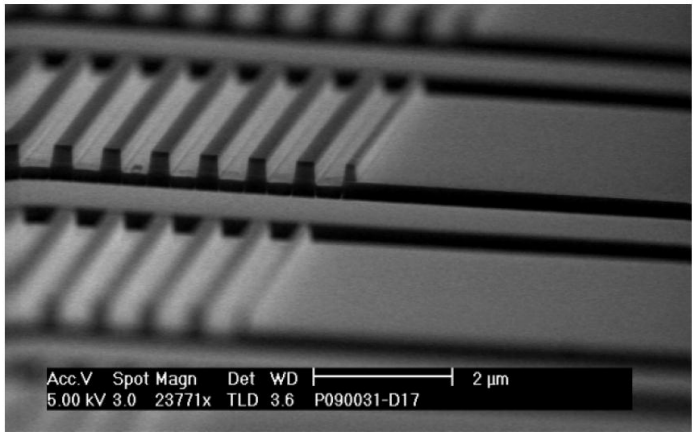
B. Bakir et al., IEEE Techn. Letters 22 (11), 739-741 (2010).

1D grating coupler

Injecting light anywhere on the surface



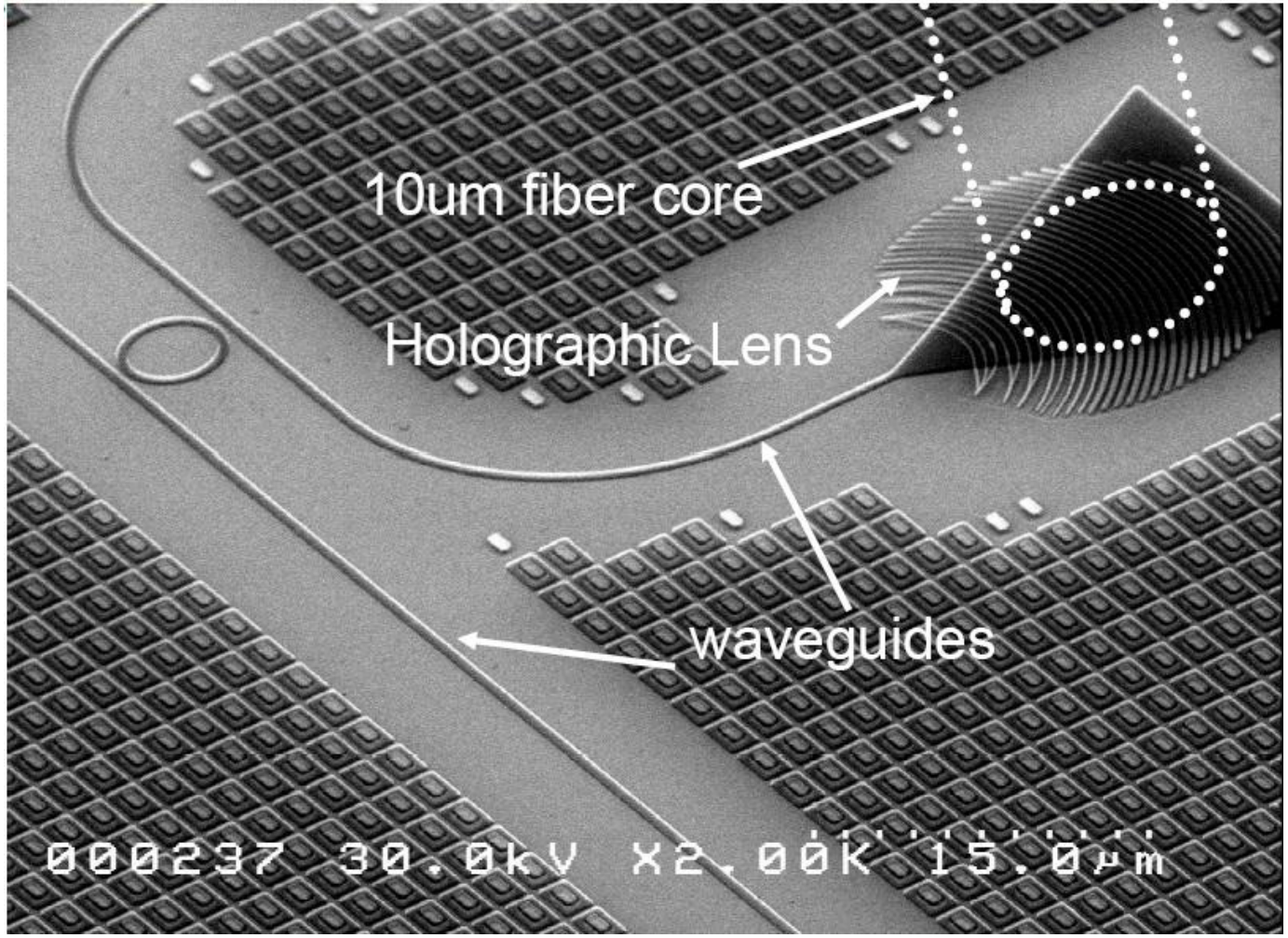




$\eta_{injection}$=68% at λ=1.55µm

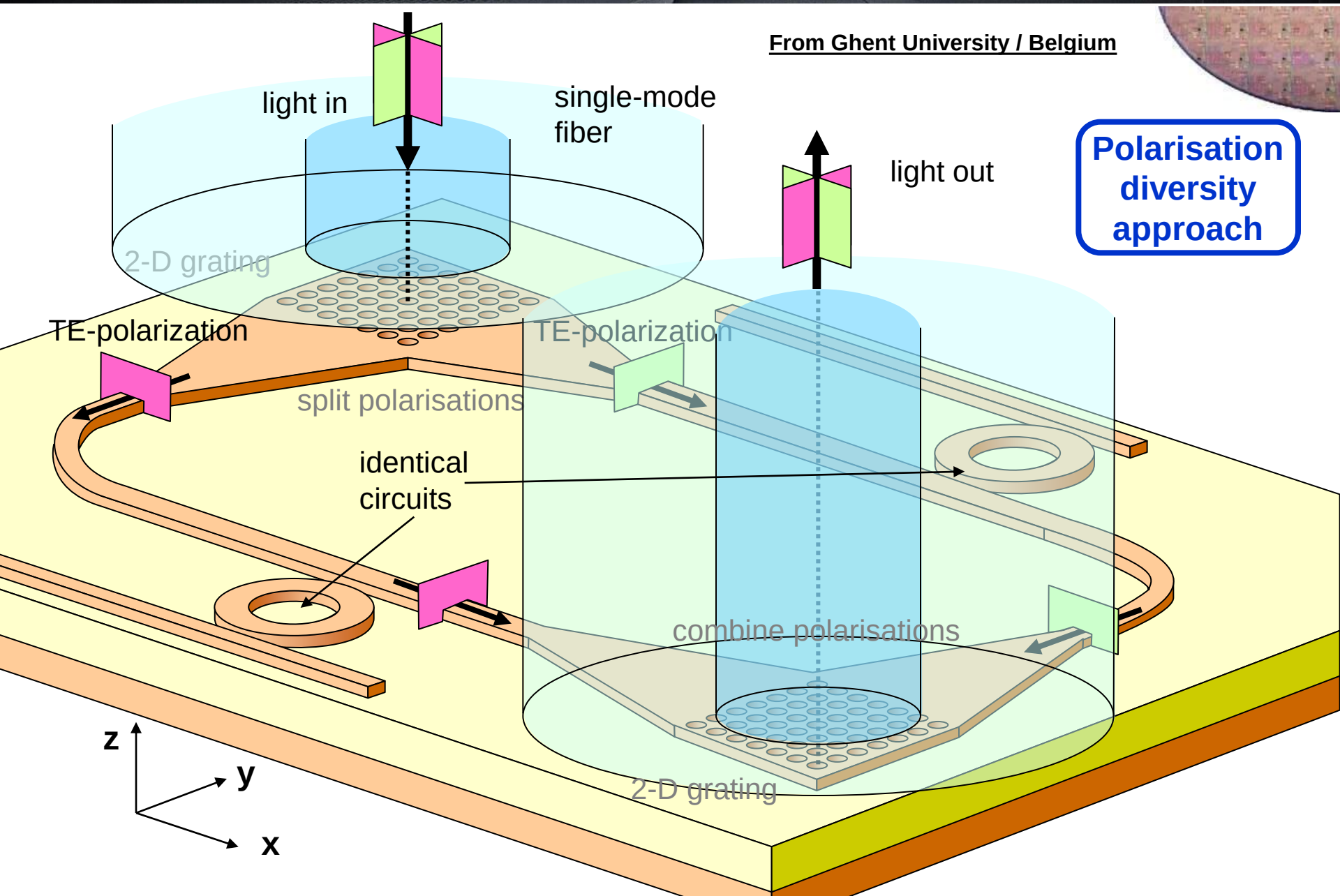
D. Vermeulen et al., The 22nd Annual Meeting of the IEEE Photonics Society, USA, p. FPd1 (2009).

Coupling to outside world

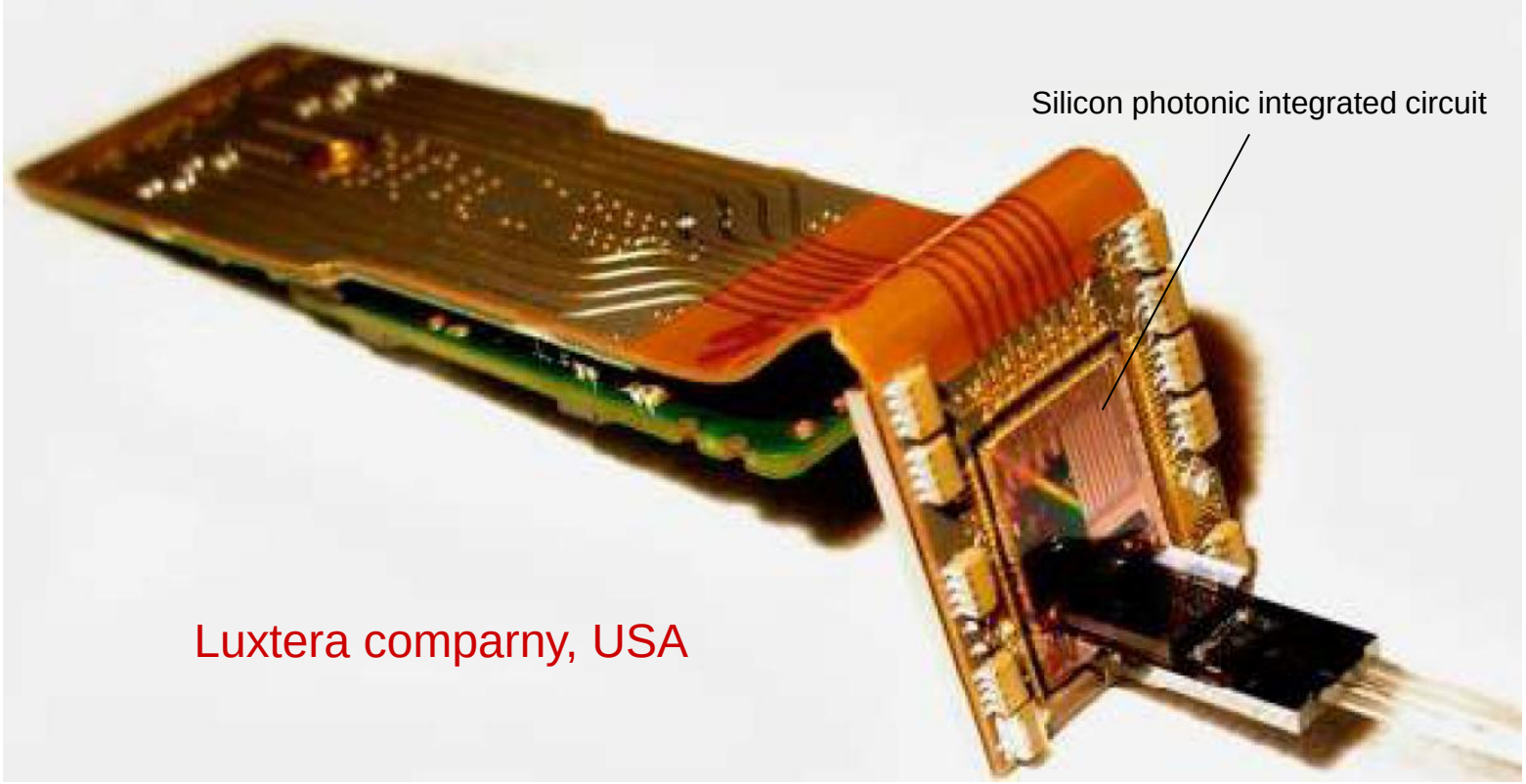


Luxtera company, USA

Coupling to outside world



Next step: fiber pigtailing



… already at the commercial stage in some companies

Outline

- Motivations and rationales
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    - ✓ Waveguides, 90°-turns, beam splitters, photonic circuits
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    - ✓ Light sources
    - ✓ Optical modulators
    - ✓ Optical detectors
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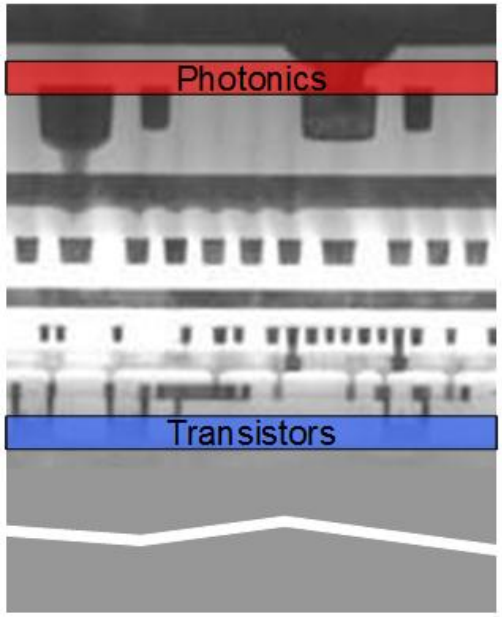
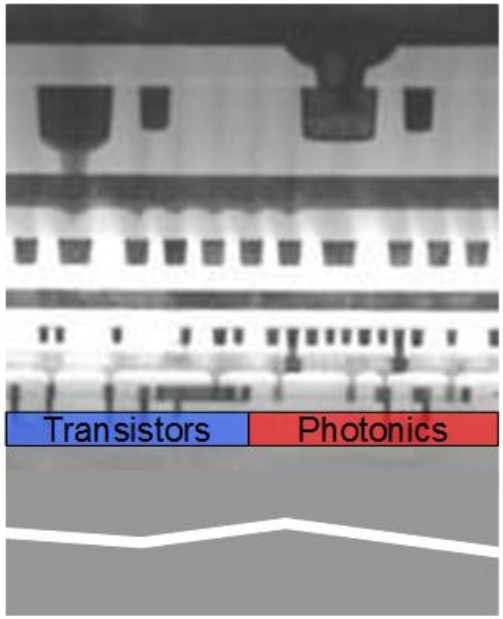
- Conclusion and perspectives

Possible integration schemes

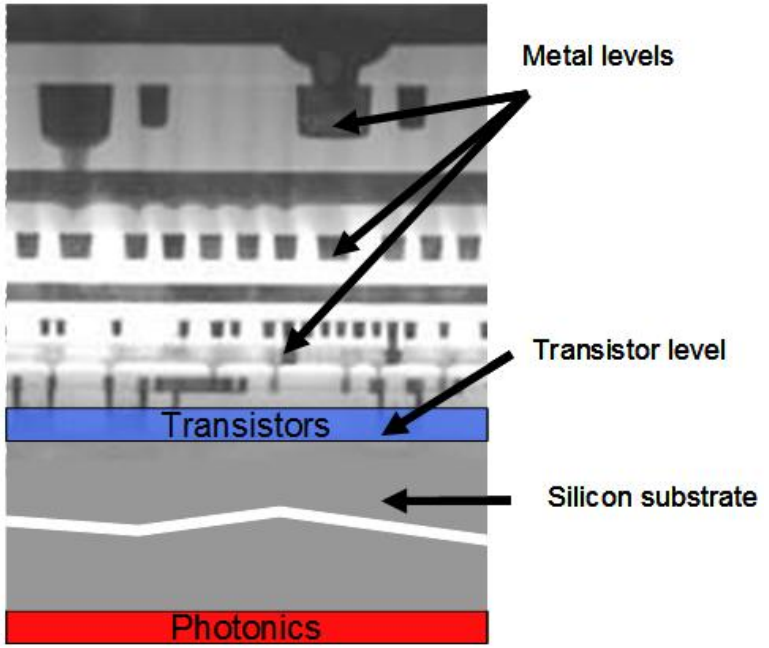
The integration of photonic devices in a CMOS chip can be envisioned by at least three means:



Option 1
Photonic layer at the last levels of metallizations with back-end fabrication



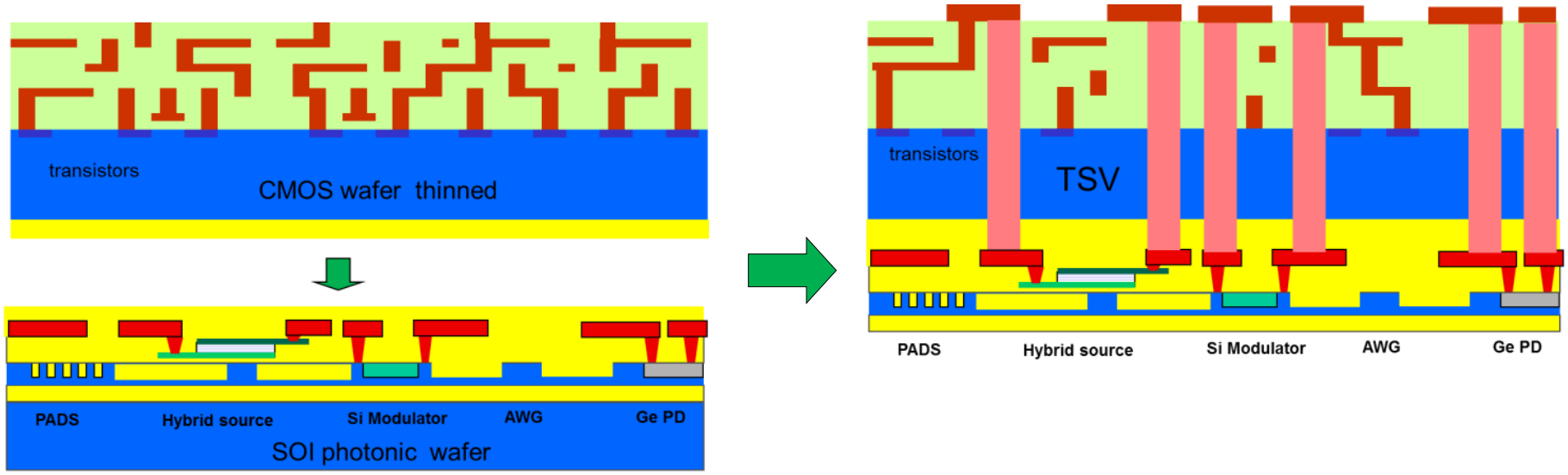
Option 2
Combined front-end fabrication



Option 3
Backside fabrication

Possible integration schemes

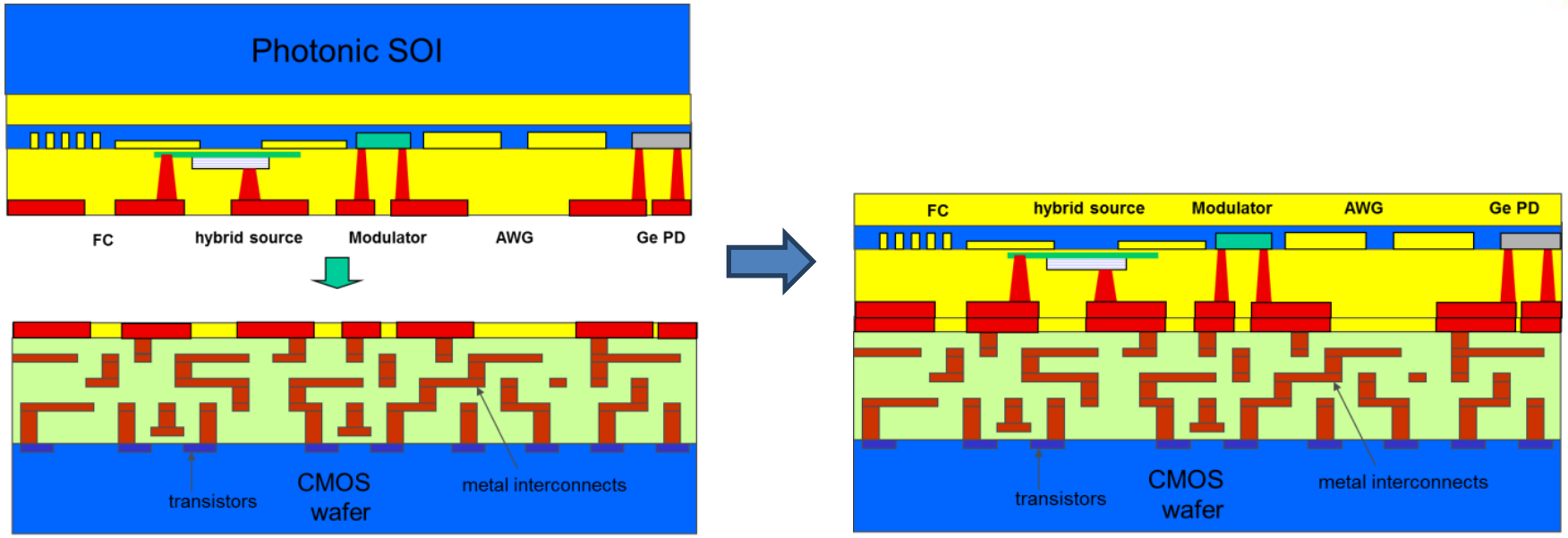
Option 3:



- Independance of the fabrication of the two electronic and photonic circuits.
- <u>But</u> : limitation in bandwidth due to long metallic vias

Possible integration schemes

Option 1: « Back-end integration of photonics with electronics »

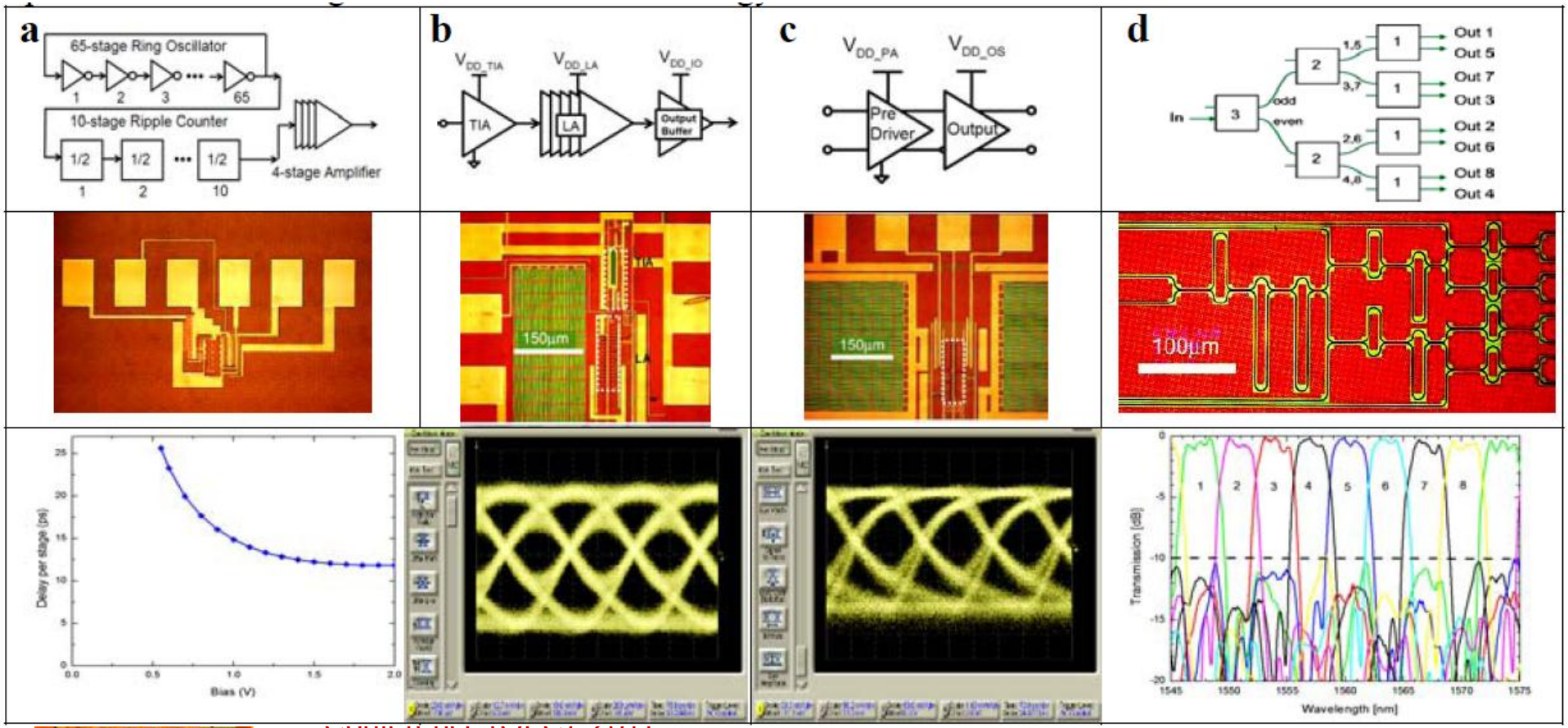


- Fabrication of electronic and photonic wafers separately
- Test of each of them
- Aligned and bonding of the photonic wafer on the electronic one (accuracy<2µm)
- Removal of the photonic substrate down to the SOI buried oxide layer

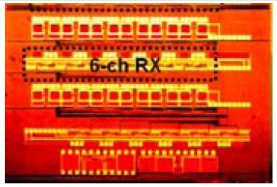
The wire bonding technology is the most flexible way to connect two chips in a package.

Possible integration schemes

Option 2: « Front-end integration of CMOS photonics with electronics »

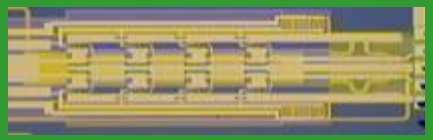


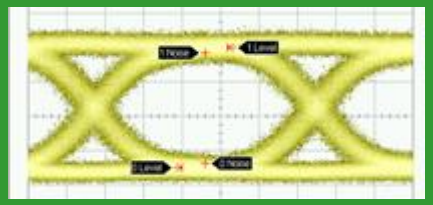
Conference (OFC), 2011.



Possible integration schemes

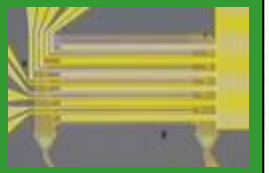
Silicon 10G Modulators
driven with on-chip circuitry
highest quality signal
low loss, low power consumption

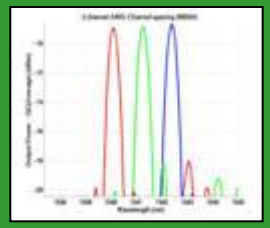




Flip-chip bonded lasers
wavelength 1550nm
passive alignment
non-modulated = low cost/reliable

Silicon Optical Filters - DWDM
electrically tunable
integrated w/ control circuitry
enables >100Gb in single mode fiber





Complete 10G Receive Path
Ge photodetectors
trans-impedance amplifiers
output driver circuitry

Fiber cable plugs here

Ceramic Package

The Toolkit is Complete
✓10Gb modulators and receivers
✓Integration with CMOS electronics
✓Cost effective, reliable light source
✓Standard packaging technology

LUXTERA

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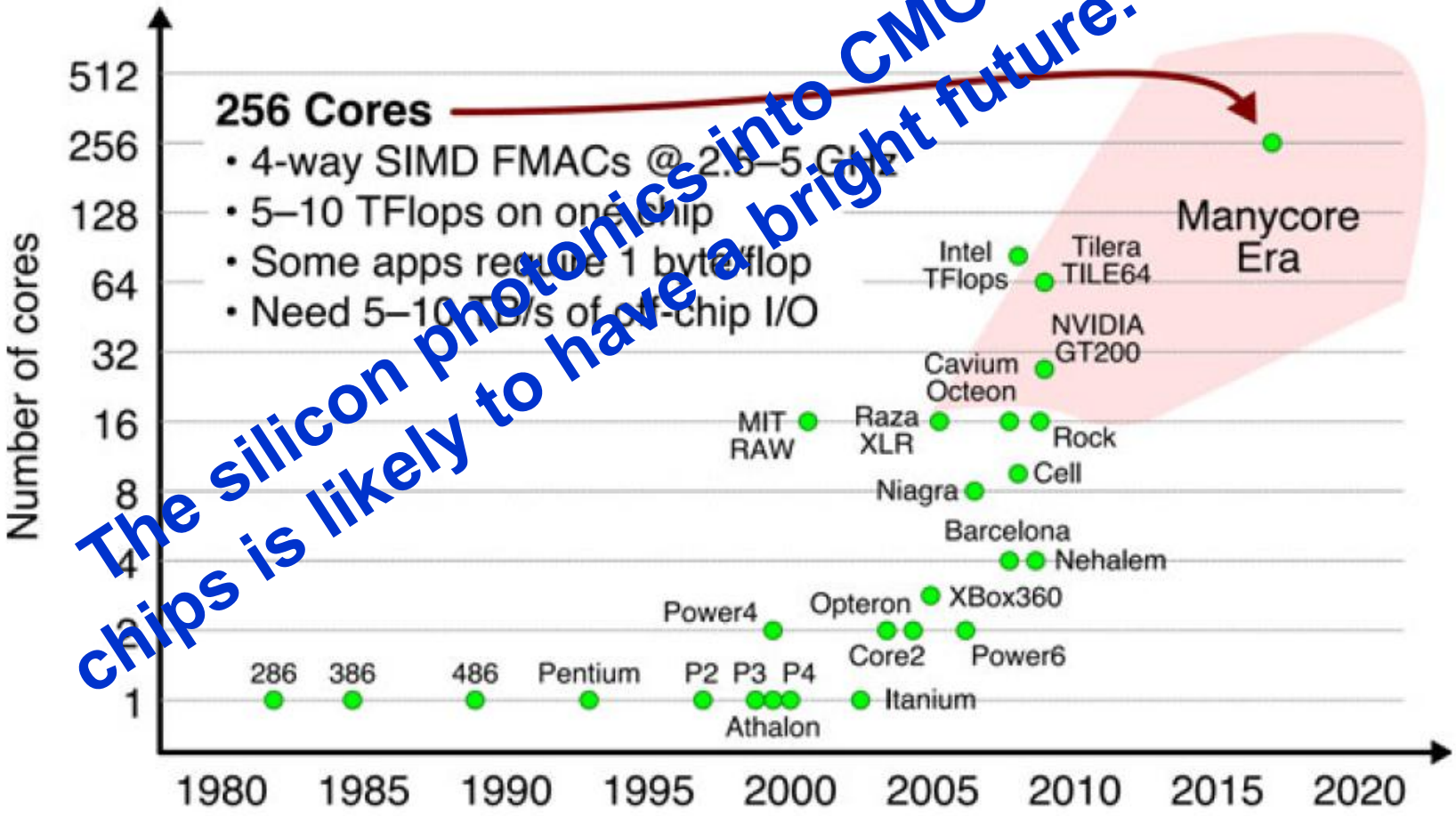
Conclusion and perspectives

- Silicon photonics has received a growing interest in the last years, and most of the basic building functionalities are now available, excepted the optical source
- Integration of optics within CMOS has not yet reached a mature stage
=> several options are still possible for on-chip optical interconnects

	Interr Area
	
Distance	multi-
Number of lines	1
Use of optics	Since the e



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pHotonics ELectronics functional Integration on CMOS - 2008-2012

ANR

SILVER

Thank you for questions

Silicon photonics group

IEF laboratory, Paris-Sud laboratory

http://silicon-photonics.ief.u-psud.fr

Agence Nationale de la Recherche ANR

heliOs

European Community's Seventh Framework Programme (FP7)

“pHotonics ELectronics functional Integration on CMOS”

Basic information about HELIOS

pHotonics ELectronics functional Integration on CMOS

www.helios-project.eu

- Large-scale integrating project (IP)
- Start date: 1 May 2008
- Duration: 48 months
- Total budget: 12 M€ (~17 M$)
- Total EC funding: 8.5 M€ (~12 M$)
- Consortium: 19 partners

Objectives of HELIOS project

- Build a complete design and fabrication chain enabling the integration of a photonic layer with a CMOS circuit, using microelectronics fabrication processes.
- Development of high performance generic building blocks that can be used for a broad range of applications:
  - WDM sources by III-V/Si heterogeneous integration
  - Fast modulators and detectors,
  - Passive circuits and packaging
- Building and optimization of the whole “food chain” to fabricate complex functional devices.
- Investigation of more promising but challenging alternative approaches for the next generation of devices (silicon source, new III-V source integration, a-Si modulators)
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

Consortium

- Different but complementary skills are requested to fulfill the project objectives:
  - Industrial end-users to drive the project, define the components architecture and specifications
  - III-V industrials to develop III-V on silicon approach, benchmarking
  - CMOS foundries and design tools experts to ensure technological relevance, photonic/electronic convergence and facilitate further exploitation
  - CMOS photonics institutes to develop processes and enable the transfer to foundries
  - Academic laboratories to optimize generic building blocks and develop innovative architectures