Silicon photonic devices

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http://silicon-photonics.ief.u-psud.fr/
Outline

- Motivations and rationales

- Photonic and opto-electronic building blocks:
  - Passive silicon photonic integrated circuits
    - Waveguides, 90°-turns, beam splitters, photonic circuits
  - Active devices:
    - Light sources
    - Optical modulators
    - Optical detectors

- Coupling to outside world

- Possible integration schemes of optics with CMOS

- Conclusion and perspectives
Increase of integrated circuit complexity
- Number of transistors
- Frequency operation
- Length and density of metallic interconnects

Metallic interconnect limitations
- RC delay
- Signal distortion
- Power consumption

Increase the number of cores

But what’s going on for intra and inter core communications?
Advantages of optics

- Negligible signal distortion even for high frequencies (>10GHz) and long distances (>1cm)
- Reduced latency, skew, and jitter
  - larger synchronous zones
  - better synchronization
- No repeaters
  - silicon area saving
  - lower power dissipation
  - reduced complexity
- Noise immunity
- Voltage insulation
Optical interconnects

Electronics/Photonics circuit

Source

Modulator

Driver

Photodetector
+ receiver circuit

90° turn

waveguide

splitter

Silicon seems to be a good material

Motivations and rationales
Silicon Pro’s and Cons

- Transparent in 1.3-1.6 µm region
- Take advantage of CMOS platform
  - Mature technology
  - High production volume
- Low cost
- Silicon On Insulator (SOI) wafer
  - Natural optical waveguide
- High-index contrast ($n_{\text{Si}}=3.5 - n_{\text{SiO}_2}=1.5$)
  - Strong light confinement
    - Small footprint (Sub-micron area)
- Electronic/photonic integration

- Indirect bandgap material
  - No electro-optic effect
  - Lacks efficient light emission
- No detection in 1.3-1.6 µm region
- High-index contrast for coupling

Strong interest for silicon photonics in the recent years
Hybrid CMOS chip merging optics and electronics??

**Motivations and rationales**

- **InP-on-Si integrated laser**
- **Silicon optical modulator**
- **ONoC Optical Network On Chip**
- **Slot waveguide for NL operation**
- **Ge-on-Si integrated photodetector**
- **MUX & DEMUX**
- **Silicon-On-Insulator waveguide**
- **Grating coupler**
- **Inverted taper**
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Passive silicon photonic integrated circuits

SOI microwaveguides: the basic device

- **Strip waveguides**
  - Mode size $\sim 0.1\mu m^2$
  - Propagation loss $\sim 1dB/cm$

- **Rib waveguides**
  - Mode size $\sim 0.2\mu m^2$
  - Propagation loss $\sim 0.2dB/cm$

SOI wafer = Optical planar waveguide
Light bending using strip wgs

- Increase for narrower waveguides:
  - Weaker confinement: bend radiation
  - More sensitive to roughness
- Increase for smaller bend radii

<table>
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<tr>
<th>Bend radius [µm]</th>
<th>Excess bend loss [dB/90°]</th>
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<tr>
<td>1</td>
<td>0.09 dB/90°</td>
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<tr>
<td>2</td>
<td>0.027 dB/90°</td>
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<tr>
<td>3</td>
<td>0.01 dB/90°</td>
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<tr>
<td>4</td>
<td>0.004 dB/90°</td>
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(FDTD simulation)

Testing device:

(IMEC)
(strip width: 540nm)
Other devices for light distribution:

Off-resonance

On-resonance

Integrated wavelength filter

Strip waveguides

Low-loss crossing

Spiral waveguide

and so on …

Results from Ghent Univ. (Belgium)
Compact star couplers:

Rib waveguides

90°-turns:

Measured loss < 0.5 dB

Other devices for light distribution:

Almost arbitrary optical paths and passive functions within SOI photonics

Other devices for light distribution: conclusion

**Strip waveguides**

- Mode size $\sim 0.1\mu m^2$
- Propagation loss $\sim 1dB/cm$

**Rib waveguides**

- Mode size $\sim 0.2\mu m^2$
- Propagation loss $\sim 0.2dB/cm$
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Overview of the optical source issue

Indirect bandgap of silicon make the source issue difficult!

Two main strategies:
• use III/V laser diodes on silicon
• develop silicon compatible optical sources using group-IV materials (e.g. Ge rich materials)

Questions to be adressed:
• Integration of optical sources on silicon: device bonding, wafer bonding, heteroepitaxial groth, heterogenous integration, …:
  ➢ several possible strategies with advantages and drawbacks: easiness, cost, thermal budget management
  ➢ injection optical waveguides: coupling issue (tolerances and misalignments, efficiency due to compatibility between optical modes)
Some proposed strategies for III/V source on Si:

**Micro-disk lasers**
- InP-based micro-disk lasers
- Die-to-wafer molecular bonding


**Fabry-Perot lasers**
- strong confinement of SOI waveguides
- optical amplification in the III/V layer

D. Liang et al., Optics Express **17**, 20355-20364 (2009).

~10-100 µW output powers

elocity
Electroluminescence properties of Germanium-rich materials (Ge/Si, GeSi quantum wells)

**Aim**: monolithic integration of optical source within CMOS

The direct bandgap can be exploited \( \lambda = 1.55 \mu m \)


Rapid progress in this field => Ge-on-Si optical source likely to appear in a near future
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Optical modulation within CMOS photonics?

Modulating the free carrier concentrations:

\[ \Delta n = -8.8 \times 10^{-22} \Delta N - 8.5 \times 10^{-18} \Delta P^{0.8} \]
\[ \Delta \alpha = 8.5 \times 10^{-18} \Delta N + 6.0 \times 10^{-18} \Delta P \]

at \( \lambda = 1.55 \mu m \)

Electro-refraction by free carrier concentration variations in silicon:

- Accumulation
- Injection
- Depletion

example:

MOS capacitances
PN, PIN, PIPIN junctions
Carrier injection

Q. Xu et al., Optics Express 15, 430-436 (2007).
Carrier depletion

Active devices: optical modulators

Hole concentration variation

Refractive index variation

Effective index variation
Carrier depletion

Insertion loss = 5 dB
Contrast ratio up to 14 dB
VπLπ = 5 V.cm

DC experimental results:

I = -2 μA at -10 V

λ ~ 1.55 μm
TE polarization

Mach-Zehnder interferometer

G. Rasigade et al.,
Optics Express, vol. 19,
n°7, pp. 5827-5832, 2011.
Carrier depletion

PN diode


Fig. 4. Normalized optical response as a function of frequency.

19 GHz small-signal bandwidth
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A material is needed for light absorption around $\lambda=1.55\mu m$
Strong absorption:

\[ \alpha \approx 9000 \text{ cm}^{-1} \text{ at } \lambda = 1.3 \mu\text{m} \]

\[ \Rightarrow L_{\text{ABS}}^{95\%} \approx 3.3 \mu\text{m} \]

\[ \Rightarrow \text{Low capacitance devices} \]

\[ \Rightarrow \text{High frequency operation} \]

Lattice misfit with Si of about 4.2%

\[ \Rightarrow \text{Specific growth strategies required} \]

2-step Ge growth on Si

\[ \Rightarrow \text{annealing to reduce threading dislocations} \]

Germanium photodetectors

**UHV-CVD (IEF)**

M. Halbwax & al., Optical Materials 27, 822-826 (2005)


**RP-CVD (LETI)**

HT Ge (~800°C, ~300-500nm)

LT Ge (~400°C, ~50nm)

Si substrate (001)
Vertical coupling

Vertical coupling

SOI waveguide

Ge

Si

SiO₂

Input optical mode

Waveguide height: 380 nm
Waveguide width: 700 nm
Etching depth: 110 nm

Active devices: detectors

Ge

Vertical coupling

Butt coupling

SOI waveguide

Ge

Si

SiO₂

→ Shorter absorption length (few microns)
→ Light absorption is independent of Ge film thickness
  (if Ge layer is thick enough: >350 nm)
Active devices: detectors

**Vertical diode**

- √ 3 µm wide mesa
- √ **i-Ge thickness**: ~300 nm
- √ **Ge length**: 15 µm

**Lateral diode**

- √ **i-Ge width**: from 1 µm to 0.5 µm
- √ **Ge length**: 10 µm

Both Ge PIN diodes theoretically lead to low dark current, high responsivity and high bandwidth.
Vertical pin diode views

Active devices: detectors
Vertical diode: DC characteristics

- 18 nA dark current at 1V reverse bias
  → Dark current density: 60 mA/cm²
- $C_{\text{measured}} \sim 12$ fF
- Under -0.5 V:
  → $\sim 1$ A/W at 1520 nm
  → $\sim 0.2$ A/W at 1600 nm
Vertical diode: RF characteristics

-3 dB bandwidth:
- 12 GHz at 0 V
- ~30 GHz at -2 V
- > 40 GHz at -4 V

Data transmission:
- 40 GBit/s at -4 V
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Coupling to outside world

The waveguide mode mismatch

... and the light polarization issue.

Direction of incoming electric field

Single-mode fiber

SOI wire

1 μm
3D adiabatic taper

- Thick silicon layer required (~10µm)
- Multilevel grey scale lithography required
- Manual polishing a the edge
- Antireflection coating is necessary

The most obvious idea is not the best one.
- Broad wavelength range
- Single mode
- Easy to fabricate (if you can do the tips)
- Low facet reflections

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<td>220</td>
<td>445</td>
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<td>75.0</td>
<td>Polymer</td>
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<td>Cornell</td>
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<td>470</td>
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<td>SiO₂</td>
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<td>&lt; 4dB</td>
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<tr>
<td>NTT</td>
<td>300</td>
<td>300</td>
<td>200.0</td>
<td>60.0</td>
<td>Polymer/Si₃N₄</td>
<td>3x3</td>
<td>0.8</td>
</tr>
</tbody>
</table>
Improved design allows the fabrication of high-efficiency and polarization-insensitive inversed tapers:

1D grating coupler

Injecting light anywhere on the surface

$\eta_{\text{injection}} = 68\%$ at $\lambda = 1.55\mu m$

D. Vermeulen et al., The 22nd Annual Meeting of the IEEE Photonics Society, USA, p. FPd1 (2009).
Coupling to outside world

Luxtera company, USA
Coupling to outside world

From Ghent University / Belgium

Polarisation diversity approach

light in

single-mode fiber

light out

2-D grating

TE-polarization

split polarisations

identical circuits

combine polarisations

2-D grating

From Ghent University / Belgium

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split polarisations

identical circuits

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2-D grating

From Ghent University / Belgium

Polarisation diversity approach
Next step: fiber pigtailing

Luxtera company, USA

… already at the commercial stage in some companies
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The integration of photonic devices in a CMOS chip can be envisioned by at least three means:

**Option 1**
Photonic layer at the last levels of metallizations with back-end fabrication

**Option 2**
Combined front-end fabrication

**Option 3**
Backside fabrication
Possible integration schemes

Option 3:

- Independance of the fabrication of the two electronic and photonic circuits.
- **But**: limitation in bandwidth due to long metallic vias
Possible integration schemes

Option 1: « Back-end integration of photonics with electronics »

- Fabrication of electronic and photonic wafers separately
- Test of each of them
- Aligned and bonding of the photonic wafer on the electronic one (accuracy<2µm)
- Removal of the photonic substrate down to the SOI buried oxide layer

The wire bonding technology is the most flexible way to connect two chips in a package.
Possible integration schemes

Option 2: « Front-end integration of CMOS photonics with electronics »

- Specific design libraries
- Separate areas for electronics and photonics
- Requirements of thermal budgets

...but this is the most ambitious approach for the development of future High Performance Computers (HPCs).

Generalization of optical interconnects to satisfy:
- Decrease of power consumption/bit,
- Increase of bandwidth.

=> Massively parallel Terabit/s optical transceivers on a single CMOS die.

IBM, Optical Fiber Conference (OFC), 2011.
**Possible integration schemes**

Silicon 10G Modulators
- driven with on-chip circuitry
- highest quality signal
- low loss, low power consumption

Flip-chip bonded lasers
- wavelength 1550nm
- passive alignment
- non-modulated = low cost/reliable

Silicon Optical Filters - DWDM
- electrically tunable
- integrated w/ control circuitry
- enables >100Gb in single mode fiber

Complete 10G Receive Path
- Ge photodetectors
- trans-impedance amplifiers
- output driver circuitry

Fiber cable plugs here

Ceramic Package

The Toolkit is Complete
- ✓10Gb modulators and receivers
- ✓Integration with CMOS electronics
- ✓Cost effective, reliable light source
- ✓Standard packaging technology

The Toolkit is Complete
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Silicon photonics has received a growing interest in the last years, and most of the basic building functionalities are now available, except the optical source.

Integration of optics within CMOS has not yet reached a mature stage => several options are still possible for on-chip optical interconnects.

Conclusion and perspectives

The silicon photonics into CMOS chips is likely to have a bright future.
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• Laurent VIVIEN
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[HELIOS FP7 IP project]

[ANR]
[CNRS]
[SILVER]
Thank you for questions

Silicon photonics group
IEF laboratory, Paris-Sud laboratory
http://silicon-photonics.ief.u-psud.fr

European Community's Seventh Framework Programme (FP7)
“pHotonics ELeクトronics functional Integration on CMOS”
Basic information about HELIOS

pHotonics ELectronics functional Integration on CMOS

www.helios-project.eu

- Large-scale integrating project (IP)
- Start date: 1 May 2008
- Duration: 48 months
- Total budget: 12 M€ (~17 M$)
- Total EC funding: 8.5 M€ (~12 M$)
- Consortium: 19 partners
Objectives of HELIOS project

- Build a complete design and fabrication chain enabling the integration of a photonic layer with a CMOS circuit, using microelectronics fabrication processes.
- Development of high performance generic building blocks that can be used for a broad range of applications:
  - WDM sources by III-V/Si heterogeneous integration
  - Fast modulators and detectors,
  - Passive circuits and packaging
- Building and optimization of the whole “food chain” to fabricate complex functional devices.
- Investigation of more promising but challenging alternative approaches for the next generation of devices (silicon source, new III-V source integration, a-Si modulators)
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.
Different but complementary skills are requested to fulfill the project objectives:

- Industrial end-users to drive the project, define the components architecture and specifications
- III-V industrials to develop III-V on silicon approach, benchmarking
- CMOS foundries and design tools experts to ensure technological relevance, photonic/electronic convergence and facilitate further exploitation
- CMOS photonics institutes to develop processes and enable the transfer to foundries
- Academic laboratories to optimize generic building blocks and develop innovative architectures