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Tests of ATLAS SCT Front-end Amplifier's ASIC Susceptibility to Beam Loss Scenario

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The Semi-Conductor Tracker in the ATLAS experiment at the Large Hadron Collider is potentially subject to various beam loss scenarios. It is important to understand what the effect of such an event would be on the operation of the SCT detector. Previous tests have shown the ABCD ASIC to be the weak point of the SCT modules when exposed to the intense radiation of a beam loss incident. According to the system specification, ABCD is expected to survive a 5nC charge over 25ns. In this study, we validate the 5nC threshold and test the ABCD's survival at greater charge dosages.

Summary 500 words

In previous tests of the ABCD fatal charge dosage, the test was done using a charged capacitor discharged by a mechanical switch. This results in an irreproducible jagged signal entering the chip. The charge deposited is well-defined; however, the time in which the charge is deposited, as well as the signal shape, varies with each flip of the switch. Our test uses a silicon switch, resulting in a clean signal that is reproducible between different trials. The high voltage step generator uses FET power transistors as a fast switch. The FET gates are driven with commercial high-side gate driver ICs, with a series gate resistor to control the step shape.

Our study consists of three tests. The first simulates a beam loss situation where the silicon detector survives the large amount of charge deposited by the beam. The charge is then transferred to the front-end amplifier. In the spirit of existing system specification, we modeled a deposition of 5nC in 25ns. This corresponds to an average current of 200mA. To complete this test, we created a circuit that can apply up to 80V to a 200pF coupling capacitor, with a rise time of about 40ns. This results in a maximum charge deposited of 16nC in a pulse 40ns in length, which is an average of 400mA throughout the pulse, doubling the system specification.

The second test simulates a more realistic scenario based on our detector studies with a charge injected by a laser beam. The large charge, of the order of 10ˆ6 MIPS, causes a local field breakdown between the backplane of the sensor, held at 450V, and the strips. The charge screening effects result in a long signal rise time, about 1 μs. We have tested ABCD chips with up to 90nC charge deposition over 1μs, resulting in a 90mA average current.

The third test is an extension of the second test. The strip AC-coupling capacitor can fail when the potential across it exceeds 100V. This can happen due to the readout electrode being held to ground by the front-end amplifier and the implant strip having high voltage due to the field breakdown outlined above. While the channel will not be usable after the breakdown of the capacitor, there is a possibility that the neighboring channel amplifiers or even the entire ASIC would be damaged in this case. Therefore, in this test we applied 450V to a 10KΩ resistor in series with the ABCD to model the bulk silicon resistivity in the field breakdown region.

For each test, pulses are applied to a single channel, and then the entire chip is tested using the ASIC built-in charge injection system with the SCT-standard module control and readout system (SCTDAQ). In this way, several channels on two chips were tested. We expected the first test with 80V applied to be the most strenuous for the chip, and there were no failures observed.

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